Allwinner Technology

A31

User Manual

Version 1.3

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Revision History

Version	Date	Author	Description
1.0	Nov 12, 2012		Initial version
1.1	June 30, 2013		Revise the video output spec
1.2	September 20, 2013		Add CPUs Port Controller register description
1.3	April 15,2015		Add the programming guide of the security system

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1 OVERVIEW

A31 is a highly integrated mobile application processor designed to provide high performance solutions for tablets, handsets, and smart TVs, etc.

It comes with a Quad-core Cortex-A7 CPU architecture that allows outstanding computing capability with less power consumption, a powerful SGX544MP2 GPU with eight logic cores, and a robust multimedia processing system that capable of 4Kx2K video decoding, Blu-ray 3D and perfect compatibility for stream media, etc.

A31 also features dual-channel 32bitx2 DRAM bus to provide wider bandwidth, and dual-channel NAND flash to speed up Read/Write operations.

Besides, A31 provides a board range of peripheral interfaces. For example, it comes with display interfaces such as HDMI, LCD RGB, MIPI DSI, and LVDS, image input interfaces such as CSI and MIPI CSI, and data interfaces such as USB DRD, USB EHCI/OHCI, GB Ethernet, SDC, SDIO, etc.

When it comes to power efficiency, A31 features smart Power Consumption Management System to dynamically adjust CPU frequency and voltage, DRAM Dynamic Frequency Scaling technology to dynamically adjust DRAM frequency based on bandwidth requirements, and also supports SuperStandby Mode to lower the power consumption during system standby.

2 FEATURE

CORTEX-A7 SUBSYSTEM

- Quad CPU
  - ARM v7 ISA Standard ARM instruction set plus Thumb-2, Jazeller RCT
  - 32KB instruction and 32KB data L1 cache for each CPU
  - NEON SIMD Coprocessor and VFPV4 for each CPU
  - TrustZone security technology
  - Hardware Virtualization support
  - Large Physical Address Extensions(LPAE)
  - Debug and trace features
  - One general timer for each CPU
- Shared 1MB L2 cache

GRAPHIC ENGINE

- **3D**
  - SGX544MP2 GPU
  - Support Open GL ES 2.0/Open VG 1.1 / Open CL 1.1 / DX 9.3 standard
  - Polygon ability up to 100M/s, pixel ability up to 3G/s
- **2D**
  - Support BLT / ROP2/3/4, scaling function with 4x4 taps and 32 phases
  - Support 90/180/270 rotation degree, mirror/alpha (plane and pixel alpha)/ color key
  - Any format conversion：ARGB 8888/4444/ 1555, RGB565, Mono 1/2/4/8 bpp, Palette 1/2/4/8 bpp (input only), YUV 444/422/420
  - Support command queue

SYSTEM RESOURCES

- **Timer**
  - 6 timers：clock source can be switched over 24M/32K for all timers, and external signals can function as clock source for timer4/5
  - 33-bit AVS counter
  - 4 watchdogs to generate reset signal or interrupts
- **GIC**
  - Support 16 SGIs, 16 PPIs, and 128 SPIs
  - Support ARM architecture security extensions
  - Support ARM architecture virtualization extensions
  - Uni-processor and multiprocessor environments
- **HS-Timer**
  - 4 channels
  - Clock source fixed to AHB, and pre-scale ranges from 1 to 16
  - 56-bit counter, can be separated to 24-bit Hi-reg and 32-bit Low-reg
- **DMA**
  - 16 channels
  - Support data width of 8/16/32 bits
  - Support linear and IO address modes
  - DMA channels can be paused during data transfer if necessary
- **RTC**
  - Real time registers for second, minute, hour, day, month and year

- Two alarms based on seconds and weeks
- 16 general purpose registers

- **CCU**
  - 11 programmable PLLs

MEMORY SUBSYSTEM

- **Internal Boot ROM**
  - 32KB in size
  - Support system boot from 8-bit NAND Flash, SPI Nor Flash (SPI0) and SD/TF/8-bit eMMC (SDC0/2)
  - Support system code download via USB DRD (USB0)

- **External SDRAM**
  - Dual Channels SDRAM Controller
  - Support memory capacity up to 16G bits
  - Support LPDDR1/2, DDR2, DDR3 SDRAM
  - Support 8/16/32 bits bus width per DRAM chip
  - 16 address lines and 3 bank address lines per channel

- **NAND FLASH**
  - Comply with ONFI 2.3 & toggle 1.0
  - Support up to 2 channels
  - Support up to 64 bits ECC per 512 bytes or
  - 1024 bytes
  - Support 8bits/16bits data bus width
  - Support 1K/2K/4K/8K/16K page size
  - Support up to 4 CE and 2 RB
  - Support hardware randomize engine
  - Support system boot from NAND flash
  - Support SLC/MLC/TLC NAND and EF-NAND
  - Support SDR/DDR NAND interface
  - Two 256x32-bit RAM for pipeline procession

- **SD/MMC**
  - Comply with eMMC standard specification v4.5
  - Comply with SD physical layer specification v3.0
  - Comply with SDIO card specification v2.0
  - Up to 1/4/8bits bus width
  - Support HS/DS/SDR12/SDR25/SDR50 /HS200/ DDR50 bus mode
  - Support eMMC mandatory and alternative boot operations
  - Support transmit clock up to100MHz
  - Support four independent SD/MMC/SDIO controllers
  - Support SDSC/SDHC/SDXC/UHS-I/MMC/ RS-MMC card
  - Support eMMC/iNand Flash
  - Support 1GB/2GB/4GB/8GB/16GB/32GB /64GB /128GB SD/MMC card
  - Support SDIO interrupt detection
  - Support build-in 64-byte FIFO for buffered read or write operations
  - Support descriptor-based internal DMA controller for efficient scatter and gather operations

IMAGE SIGNAL PROCESSOR

- Support multiple input formats, including 8/10/12 bits RAM RGB, 8/10 bits YCbCr
- Support multiple output formats, includingYCbCr 420 semi-planar, YCrCb 420 semi-planar, YCbCr 422 semi-planar, YCrCb 422 semi-planar, YUV 420 planar, YUV 422 planar
- Support image mirror flip and rotation;
- Support thumb image generation;
- Support two channels output;
- Support valid picture size up to 4096x4096;
- Support speed up to 250Mpixel/s;
- ISP for YCbCr input:
  - YCbCr gain and offset control
  - DRC(dynamic range compression)
  - Anti-flick detection statistics
  - Histogram statistics
- ISP for RAW RGB input
  - Black clamp with horizontal/vertical offset compensation
  - Window capture
  - Static/dynamic defect pixel correction

- Super lens shading correction
- Super lens flare correction
- Color dependent gain and offset control
- Anisotropic non-linear bayer interpolation with false color suppression
- Programmable color correction
- Programmable gamma correction
- DRC(dynamic range compression)
- RGB2YCbCr
- Non-linear 2D sharpening
- Advanced contrast enhancement
- Advanced spatial (2D) de-noise filter
- Zone-based AE/AF/AWB statistics
- Anti-flick detection statistics
- Histogram statistics

VIDEO ENGINE

- Decoder and encoder can work at the same time
- Video decoding
  - Picture size up to 4096x2304
  - Decoding speed up to 1920x1080@60fps
  - Support multiple video formats, including Mpeg1, Mpeg2, Mpeg4 SP/ASP GMC , H.263 including Sorenson Spark, H.264 BP/MP/HP, VP6/8, AVS jizun, JPEG/MJPEG
  - Support tiled/YUV/YUV output format
- Video encoding
  - H.264 HP: picture size up to 3840x2160
  - H.264 HP: speed up to 1920x1080@60fps
  - H.264 HP: cyclic intra refresh
  - H.264 HP: ROI windows
  - JPEG baseline: picture size up to 8192x8192
  - Alpha blending
  - Thumb generation
  - 4x2 scaling ratio: from 1/16 to 64 arbitrary non-integer ratio

DISPLAY ENGINE

- Support dual display paths
  - Each path supports 4 movable and size-adjustable layers
  - Layer size up to 8192x8192 pixels
- Ultra-scaling Engine
  - 8 taps in horizontal and 4 taps in vertical
  - Source image size from 8x4 to 8192x8192
  - Destination image size from 8x4 to 8192x8192
- Support multiple image input formats
  - Mono 1/2/4/8 bpp
  - Palette 1/2/4/8 bpp
  - 16/24/32 bpp color
  - YUV444/420/422/411
- Support alpha blending, color key, gamma, hardware cursor
- Support powerful video post processing
  - De-interlacing
  - Detail enhancement
  - Dynamic range control
  - Color management
- 3D content input/output format conversion and display (with HDMI)

VIDEO INPUT

- Support 4 lanes MIPI CSI, 1G bps per lane (up to 12M pixels still image or 1080p@60fps video)
- Support parallel 12bits CSI

VIDEO OUTPUT

- Support HDMI 1.4, speed up to 3G bps per channel, resolution up to 1080p@60fps
- Dual flexible sync RGB/CPU/LVDS LCD interface, up to 1080p@60fps
- Support 4 lanes MIPI DSI, 1G bps per lane, resolution up to 1920x1200/1080p@60fps
- Support dual display devices processing

ANALOG AUDIO INPUT

- Support two audio ADC channels
  - 96dBA SNR for ADC recording
  - 8KHz~ 48KHz ADC sample rate
- Analog low-power loop from line-in/mic-in/ phone-in to headphone/speaker/ receiver

outputs
- Accessory button press detection
- Five analog audio inputs
  - Three differential microphone inputs
  - Differential phone-in input
  - Stereo line-in input
- Support low-noise digital MIC interface
- Flexible digital audio process for ADC
  - High pass filter and low latency decimation filter for class voice
  - Automatic gain control (AGC)

ANALOG AUDIO OUTPUT

- Two audio DAC channels
- Stereo capless headphone drivers
  - Up to 100dBA SNR for DAC playback
  - 8KHz~192KHz DAC sample rate
- Support analog/digital volume control
- Two low-noise analog microphone bias
- Dedicated headphone/speaker/receiver outputs, single-ended or differential
- Support differential phone-out
- Support two mixers for different applications
  - Output mixer for LINEINL/R, PHONEP/N, MIC1P/N, MIC2P/N and stereo DAC output
  - ADC record mixer for LINEINL/R, PHONEP/N, MIC1P/N, MIC2P/N, MIC3P/N and stereo DAC output
- Flexible digital audio process for DAC
  - Pop suppression control
  - Individual high pass filter/De-emphasis filter
  - Support EQ equalization
  - Soft volume control and soft mute

GPADC

- Support 12-bit resolution
- Conversion rate up to 1MSPS
- 3V power supply
- Analog input range 0V~3V
- On-chip sample-and-hold function
- Single or multiple input channel select mode
- Median and averaging filter to reduce noise

CONNECTIVITY

- **USB2.0 DRD**
  - Support High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps), and Low-Speed (LS, 1.5-Mbps) in Host mode
  - Support High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps) in Device mode
  - 8K SRAM for EP Buffer
  - Support up to 10 user-configurable endpoints for bulk , isochronous**,** control and interrupt bi-directional transfers

- **USB EHCI/OHCI**
  - Two EHCI/OHCI-compliant hosts
  - One OHCI only FS Host

- **Digital Audio Interface**
  - Comply with industry standard I2S/PCM specification
  - Two sets of I2S/PCM interfaces for baseband and Bluetooth
  - Support Master/Slave mode and full-duplex operation
  - Support 8KHz~192KHz audio sample rate
  - Support MCLK output for CODEC chips
  - Support standard I2S, left-justified, right-justified, 8/16-bit linear sample, 8-bit u-law and a-law companded sample

- **LRADC**
  - 6-bit resolution
  - Support 0V ~2V voltage input

- **CIR**
  - A flexible receiver for IR remote controller

- **Transport Stream**
  - Support both SPI and SSI
  - Support 64 channels PID filter
  - Support hardware PCR packet detection
  - Speed up to 150Mbps for both SPI and SSI interface

- **EMAC**
  - Comply with IEEE 802.3-2002 standard

- controllable on a per-frame basis
- Options for automatic Pad/CRC stripping on receive frames
- Programmable frame length to support standard or Jumbo Ethernet frames with size up to 16KB
- Support 10/100/1000-Mbps transfer rates
- IEEE 802.3-compliant GMII/MII interface to communicate with an external Gigabit/Fast Ethernet PHY
- Support 10/100/1000-Mbps data transfer rates RGMII interface to communicate with an external Giga bit PHY

- **UART**
  - Comply with industry-standard 16450/16550 UARTS specification
  - Support fully AMBA APB CPU interface programmable operation
  - Support 16-bit programmable baud rate and dynamic modification
  - Support 2-wire serial communication
  - Support 4-wire auto data flow communication
  - Support 8-wire modem(data carrier equipment, DCE) or data set
  - Support up to 7 UART controllers

- **TWI**
  - Up to 5 TWIs compliant with I2C protocol
  - Support SCCB protocol

- **P2WI (Push-Pull TWI)**
  - Support speed up to 2MHz

- **SPI**
  - Master/Slave configurable
  - Up to 4 independent SPI controllers, SPI0 with only one CS signal for system boot, and SPI1/2/3 with two CS signals
  - Support dual-input and dual-output operation

- **One Wire Interface**
  - Support both standard One Wire protocol and simple HDQ protocol

- **PWM**
  - 4 PWM outputs
  - Support cycle mode and pulse mode
  - The pre-scale ranges from 1 to 64

SECURITY SYSTEM

- Support AES, DES, 3DES, SHA-1, MD5
- Support ECB, CBC, modes for AES/DES/3DES 128-bit, 192-bit and 256-bit key size for AES
- 160-bit hardware PRNG with 192-bit seed
- Security JTAG

POWER MANAGEMENT

- Flexible PLL clock generator and 32768Hz OSC
- Flexible clock gate and module reset
- Support DVFS for CPU frequency and voltage adjustment
- Support dynamic frequency adjustment for external DRAM controller
- Support standby mode

PROCESS & PACKAGE

- FBGA 609-balls, 0.65-mm ball pitch, 18 x 18 x 1.4-mm

3 SYSTEM

This chapter introduces the overall system architecture of A31 from following perspectives:

- BLOCK DIAGRAM,
- MEMORY MAPPING
- BOOT SYSTEM
- CCU
- CPU
- TRUSTZONE
- SYSTEM CONTROL
- PRCM
- TIMER
- HIGH SPEED TIMER
- PWM
- DMA
- GIC
- RTC
- SECURITY SYSTEM
- GPADC
- LRADC
- AUDIO CODEC
- PORT CONTROLLER

3.1. BLOCK DIAGRAM

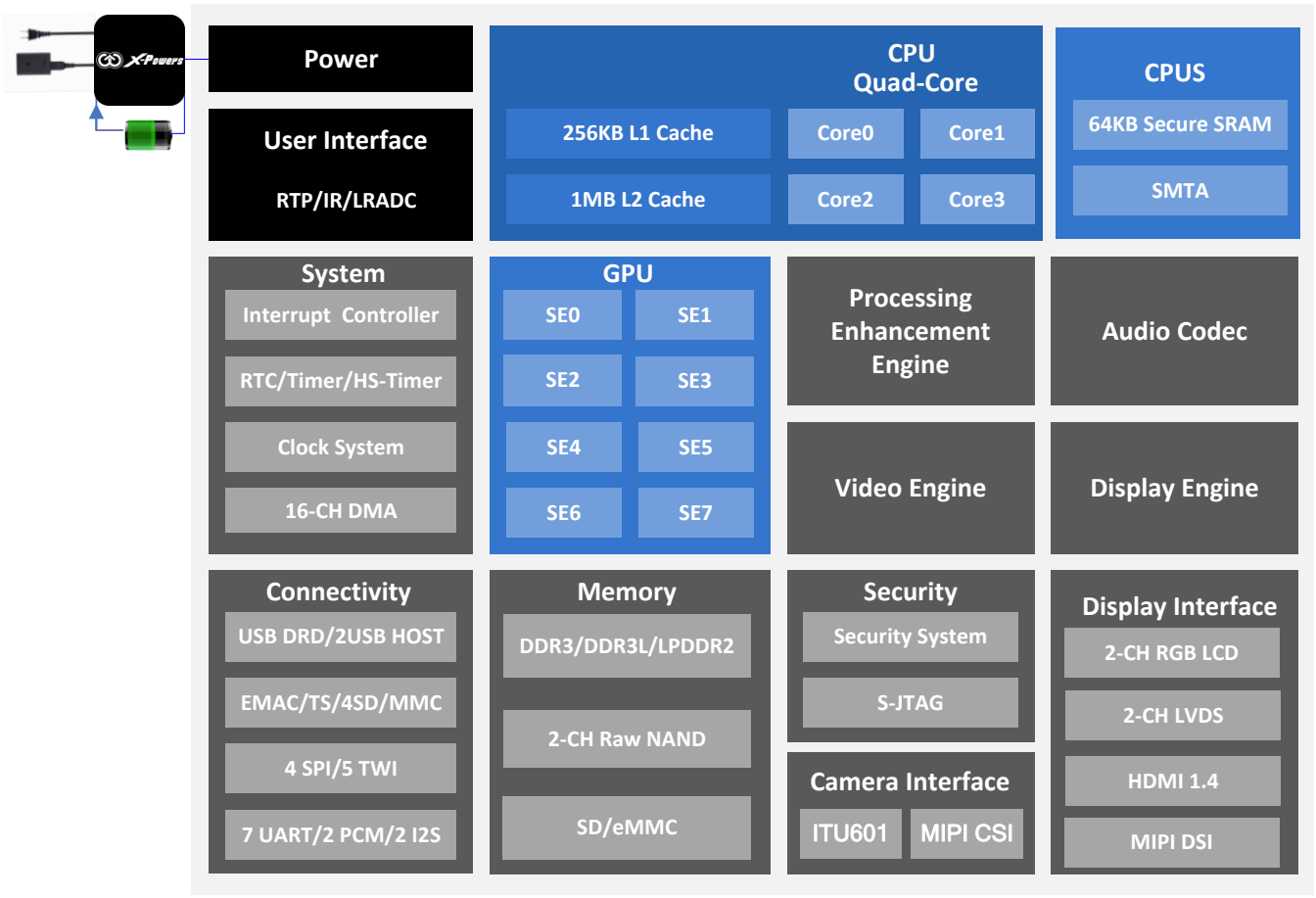


Figure 3-1 A31 Block Diagram

3.2. MEMORY MAPPING

Module	CPUX Address	Size(Bytes)
SRAM A1	0x0000 0000---0x0000 7FFF	32K
SRAM A2	/	64K
SRAM Nand	/	2K
SRAM B(Secure)	0x0002 0000---0x0002 FFFF	64K
SRAM Controller	0x01C0 0000---0x01C0 0FFF	4K
/	0x01C0 1000---0x01C0 1FFF	4K
DMA	0x01C0 2000---0x01C0 2FFF	4K
NFC0	0x01C0 3000---0x01C0 3FFF	4K
TS	0x01C0 4000---0x01C0 4FFF	4K
NFC1	0x01C0 5000---0x01C0 5FFF	4K
/	0x01C0 6000---0x01C0 6FFF	4K
/	0x01C0 7000---0x01C0 7FFF	4K
/	0x01C0 8000---0x01C0 8FFF	4K
/	0x01C0 9000---0x01C0 9FFF	4K
/	0x01C0 A000---0x01C0 AFFF	4K
/	0x01C0 B000---0x01C0 BFFF	4K
LCD 0	0x01C0 C000---0x01C0 CFFF	4K
LCD 1	0x01C0 D000---0x01C0 DFFF	4K
VE	0x01C0 E000---0x01C0 EFFF	4K
SD/MMC 0	0x01C0 F000---0x01C0 FFFF	4K
SD/MMC 1	0x01C1 0000---0x01C1 0FFF	4K
SD/MMC 2	0x01C1 1000---0x01C1 1FFF	4K
SD/MMC 3	0x01C1 2000---0x01C1 2FFF	4K
/	0x01C1 3000---0x01C1 3FFF	4K

/	0x01C1 4000---0x01C1 4FFF	4K
SS	0x01C1 5000---0x01C1 5FFF	4K
HDMI	0x01C1 6000---0x01C1 6FFF	4K
/	0x01C1 7000---0x01C1 7FFF	4K
/	0x01C1 8000---0x01C1 8FFF	4K
USB-DRD	0x01C1 9000---0x01C1 9FFF	4K
USB-EHCI0/OHCI0	0x01C1 A000---0x01C1 AFFF	4K
USB-EHCI1/OHCI1	0x01C1 B000---0x01C1 BFFF	4K
USB-OHCI2	0x01C1 C000---0x01C1 CFFF	4K
/	0x01C1 D000---0x01C1 DFFF	4K
TZASC	0x01C1 E000---0x01C1 EFFF	4K
/	0x01C1 F000---0x01C1 FFFF	4K
CCU	0x01C2 0000---0x01C2 03FF	1K
/	0x01C2 0400---0x01C2 07FF	1K
PIO	0x01C2 0800---0x01C2 0BFF	1K
TIMER0_5	0x01C2 0C00---0x01C2 0FFF	1K
/	0x01C2 1000---0x01C2 13FF	1K
PWM0_3	0x01C2 1400---0x01C2 17FF	1K
/	0x01C2 1800---0x01C2 1BFF	1K
/	0x01C2 1C00---0x01C2 1FFF	1K
DAUDIO-0	0x01C2 2000---0x01C2 23FF	1K
DAUDIO-1	0x01C2 2400---0x01C2 27FF	1K
LRADC 0/1	0x01C2 2800---0x01C2 2BFF	1K
AudioCodec	0x01C2 2C00---0x01C2 2FFF	1K
/	0x01C2 3000---0x01C2 33FF	1K
TZPC	0x01C2 3400---0x01C2 37FF	1K
SID	0x01C2 3800---0x01C2 3BFF	1K
SJTAG	0x01C2 3C00---0x01C2 3FFF	1K
/	0x01C2 4000---0x01C2 43FF	1K

/	0x01C2 4400---0x01C2 47FF	1K
/	0x01C2 4800---0x01C2 4BFF	1K
/	0x01C2 4C00---0x01C2 4FFF	1K
TP	0x01C2 5000---0x01C2 53FF	1K
DMIC	0x01C2 5400---0x01C2 57FF	1K
/	0x01C2 5800---0x01C2 5BFF	1K
/	0x01C2 5C00---0x01C2 5FFF	1K
/	0x01C2 6000---0x01C2 63FF	1K
/	0x01C2 6400---0x01C2 67FF	1K
/	0x01C2 6800---0x01C2 6BFF	1K
/	0x01C2 6C00---0x01C2 6FFF	1K
/	0x01C2 7000---0x01C2 73FF	1K
/	0x01C2 7400---0x01C2 77FF	1K
/	0x01C2 7800---0x01C2 7BFF	1K
/	0x01C2 7C00---0x01C2 7FFF	1K
UART 0	0x01C2 8000---0x01C2 83FF	1K
UART 1	0x01C2 8400---0x01C2 87FF	1K
UART 2	0x01C2 8800---0x01C2 8BFF	1K
UART 3	0x01C2 8C00---0x01C2 8FFF	1K
UART 4	0x01C2 9000---0x01C2 93FF	1K
UART 5	0x01C2 9400---0x01C2 97FF	1K
	0x01C2 9800---0x01C2 9BFF	1K
/	0x01C2 9C00---0x01C2 9FFF	1K
/	0x01C2 A000---0x01C2 A3FF	1K
/	0x01C2 A400---0x01C2 A7FF	1K
/	0x01C2 A800---0x01C2 ABFF	1K
TWI 0	0x01C2 AC00---0x01C2 AFFF	1K
TWI 1	0x01C2 B000---0x01C2 B3FF	1K
TWI 2	0x01C2 B400---0x01C2 B7FF	1K

TWI 3	0x01C2 B800---0x01C2 BBFF	1K
/	0x01C2 BC00---0x01C2 BFFF	1K
/	0x01C2 C400---0x01C2 C7FF	1K
/	0x01C2 C800---0x01C2 CBFF	1K
/	0x01C2 CC00---0x01C2 CFFF	1K
EMAC	0x01C3 0000---0x01C3 FFFF	64K
GPU	0x01C4 0000---0x01C4 FFFF	64K
HSTMR0_3	0x01C6 0000---0x01C6 0FFF	4K
/	0x01C6 1000---0x01C6 1FFF	4K
DRAMCOM	0x01C6 2000---0x01C6 2FFF	4K
DRAMCTL0	0x01C6 3000---0x01C6 3FFF	4K
DRAMCTL1	0x01C6 4000---0x01C6 4FFF	4K
DRAMPHY0	0x01C6 5000---0x01C6 5FFF	4K
DRAMPHY1	0x01C6 6000---0x01C6 6FFF	4K
/	0x01C6 7000---0x01C6 7FFF	
SPI0	0x01C6 8000---0x01C6 8FFF	4K
SPI1	0x01C6 9000---0x01C6 9FFF	4K
SPI2	0x01C6 A000---0x01C6 AFFF	4K
SPI3	0x01C6 B000---0x01C6 BFFF	4K
/	0x01C8 0000	
MIPI DSI0	0x01CA 0000---0x01CA 0FFF	4K
MIPI DSI0-PHY	0x01CA 1000---0x01CA 1FFF	4K
CSI0	0x01CB 0000---0x01CB 0FFF	4K
MIPI CSI0	0x01CB 1000---0x01CB 1FFF	4K
MIPI CSI0-PHY	0x01CB 2000---0x01CB 2FFF	4K
CSI1	0x01CB 3000---0x01CB 3FFF	4K
ISP	0x01CB 8000---0x01CB 8FFF	4K
ISP-Memory	0x01CC 0000---0x01CF FFFF	256K
SRAM Area C	0x01D0 0000---0x01DF FFFF	Module sram

DE_FE0	0x01E0 0000---0x01E1 FFFF	128K
DE_FE1	0x01E2 0000---0x01E3 FFFF	128K
DRC1	0x01E5 0000---0x01E5 FFFF	64K
DE_BE0	0x01E6 0000---0x01E6 FFFF	64K
DRC0	0x01E7 0000---0x01E7 FFFF	64K
DE_BE1	0x01E4 0000---0x01E4 FFFF	64K
MP	0x01E8 0000---0x01E9 FFFF	128K
DEU1	0x01EA 0000---0x01EA FFFF	64K
DEU0	0x01EB 0000---0x01EB FFFF	64K
PS	0x01EF 0000---0x01EF FFFF	64K
RTC	0x01F0 0000---0x01F0 03FF	1K
/	0x01F0 0400---0x01F0 07FF	1K
/	0x01F0 0800---0x01F0 0BFF	1K
/	0x01F0 0C00---0x01F0 0FFF	1K
/	0x01F0 1000---0x01F0 13FF	1K
/	0x01F0 1400---0x01F0 17FF	1K
/	0x01F0 1800---0x01F0 1BFF	1K
/	0x01F0 1C00---0x01F0 1FFF	1K
/	0x01F0 2000---0x01F0 23FF	1K
/	0x01F0 2400---0x01F0 27FF	1K
/	0x01F0 2800---0x01F0 2BFF	1K
/	0x01F0 2C00---0x01F0 2FFF	1K
/	0x01F0 3000---0x01F0 33FF	1K
/	0x01F0 3400---0x01F0 37FF	1K
/	0x01F0 3800---0x01F0 3BFF	1K
/	0x01F2 0000---0x01F2 0FFF	4K
/	0x01F2 1000---0x01F2 1FFF	4K
/	0x01F2 2000---0x01F2 2FFF	4K
/	0x01F2 3000---0x01F2 3FFF	4K

/	0x01F2 4000---0x01F2 4FFF	4K
DDR-II/DDR-III/LPDDR-II	0x4000 0000---0xBFFF FFFF	2G
BROM	0xFFFF 0000—0xFFFF 7FFF	32K

3.3. BOOT SYSTEM

3.3.1. OVERVIEW

A31 supports five boot methods. Based on the status of UBOOT_SEL pin and two BOOT_SEL pins, the system can boot from NAND Flash, SPI NOR Flash (SPI0), eMMC, SD Card (SDC0/2), and USB.

In normal state, UBOOT_SEL pin is pulled up by an internal 50K resistor, and if it is checked to be in Low level state after system power on, the system will choose to boot from USB;

The BOOT_SEL pins are pulled up by internal 50K resistors as well, and they can be used to determine from which media the system should be booted firstly.

3.3.2. BOOT DIAGRAM

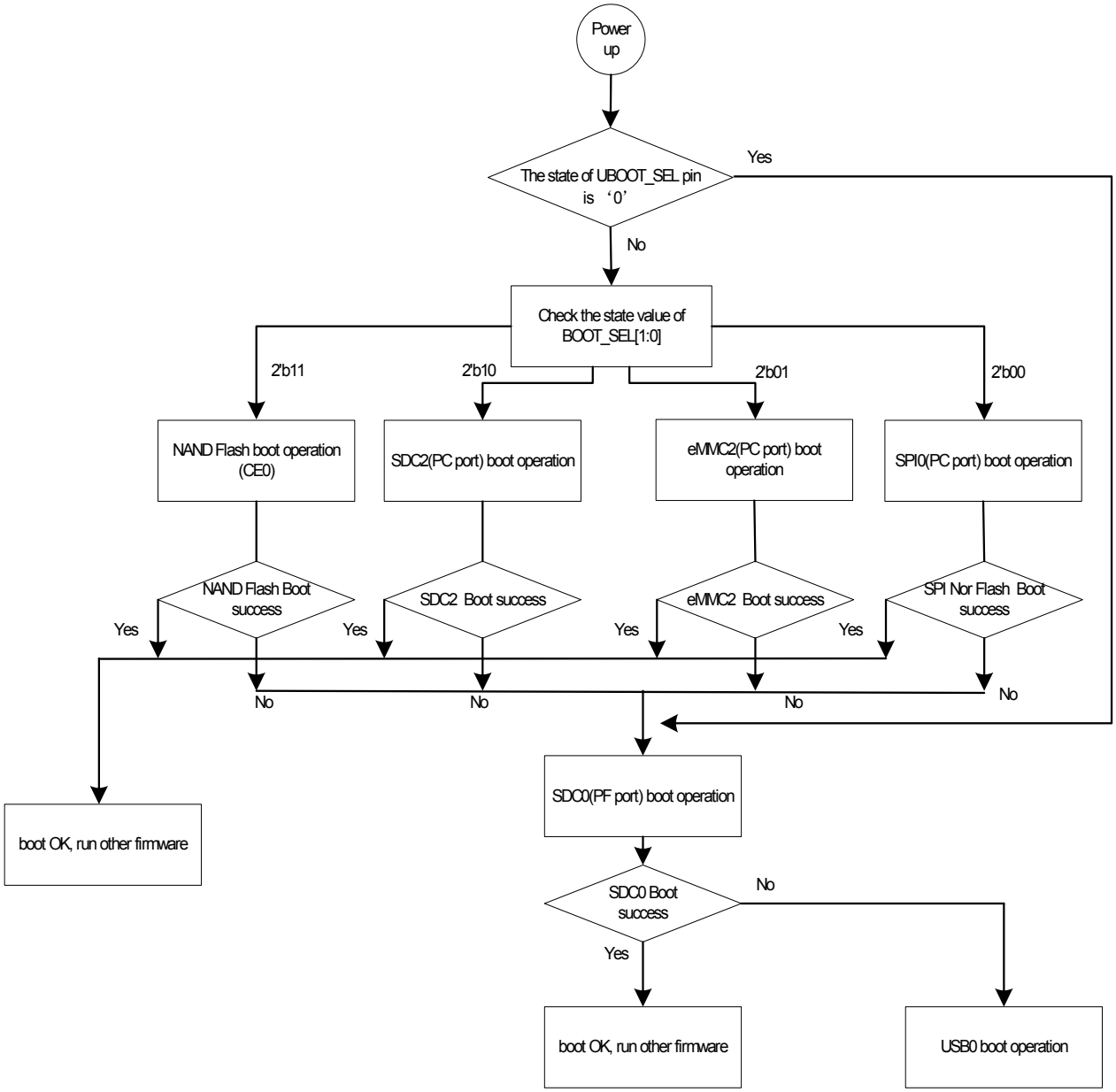


Figure 3-2 Boot Diagram

3.4. CCU

3.4.1. OVERVIEW

The CCU (Clock Control Unit) is made up of 11 PLLs, a main oscillator, an on-chip RC oscillator (466.9KHz ~ 867.1KHz), and a 32768Hz low-power oscillator.

It integrates two crystal oscillators: *a 24MHz crystal* is mandatory, which provides clock source for PLL and main digital blocks, and a *32768Hz oscillator*, which is only used to provide a low power, accurate reference for RTC.

The CCU features:

- 11 PLLs, a Main Oscillator, an on-chip RC Oscillator and a 32768Hz low-power Oscillator
- PLL1 is the main clock of CPU0/1/2/3
- Support clock configuration for corresponding module
- Support software-controlled clock gating
- Support software-controlled reset for corresponding module
- Support 3 clock output channels

3.4.2. A31 CPU CLOCK DIAGRAM

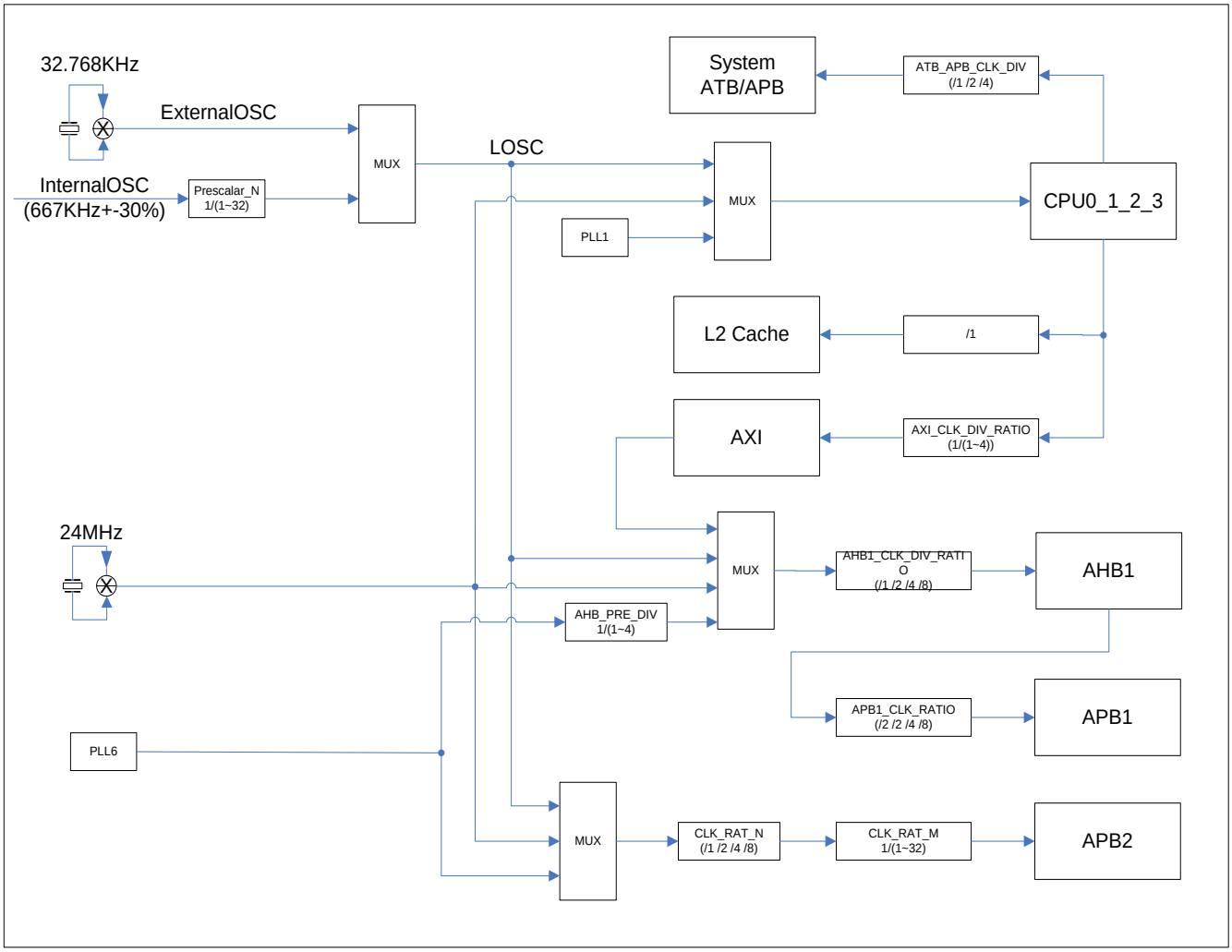


Figure 3-3 CPU Clock Diagram

3.4.3. CCU REGISTER LIST

Module Name	Base Address
CCU	0x01c20000

Register Name	Offset	Description
PLL1_CFG_REG	0x0000	PLL1 control register(CPU0_1_2 _3 PLL)
PLL2_CFG_REG	0x0008	PLL2 control register (Audio PLL)

PLL3_CFG_REG	0x0010	PLL3 control register (Video 0 PLL)
PLL4_CFG_REG	0x0018	PLL4 control register (VE PLL)
PLL5_CFG_REG	0x0020	PLL5 control register (DDR PLL)
PLL6_CFG_REG	0x0028	PLL6 control register (Peripheral PLL)
PLL7_CFG_REG	0x0030	PLL7 control register (Video 1 PLL)
PLL8_CFG_REG	0x0038	PLL8 control register (GPU PLL)
MIPI_PLL_CFG_REG	0x0040	MIPI_PLL control register
PLL9_CFG_REG	0x0044	PLL9 control register
PLL10_CFG_REG	0x0048	PLL10 control register
CPU_AXI_CFG_REG	0x0050	CPU /AXI CLK ratio register
AHB1_APB1_CFG_REG	0x0054	AHB1/APB1 CLK ratio register
APB2_CLK_DIV_REG	0x0058	APB2 clock divider register
AHB1_GATING_REG0	0x0060	AHB1 module clock gating register 0
AHB1_GATING_REG1	0x0064	AHB1 module clock gating register 1
APB1_GATING_REG	0x0068	APB1 module clock gating register
APB2_GATING_REG	0x006C	APB2 module clock gating register
NAND0_SCLK_CFG_REG	0x0080	NAND0 SCLK configuration register
NAND1_SCLK_CFG_REG	0x0084	NAND1 SCLK configuration register
SD0_CLK_REG	0x0088	SD/MMC 0 Clock Register
SD1_CLK_REG	0x008C	SD/MMC 1 Clock Register
SD2_CLK_REG	0x0090	SD/MMC 2 Clock Register
SD3_CLK_REG	0x0094	SD/MMC 3 Clock Register
TS_CLK_REG	0x0098	Transport Stream Clock Register
SS_CLK_REG	0x009C	Security System Clock Register
SPI0_CLK_REG	0x00A0	SPI0 Clock Register
SPI1_CLK_REG	0x00A4	SPI1 Clock Register
SPI2_CLK_REG	0x00A8	SPI2 Clock Register
SPI3_CLK_REG	0x00AC	SPI3 Clock Register
DAUDIO0_CLK_REG	0x00B0	DAUDIO0 Clock Register

DAUDIO1_CLK_REG	0x00B4	DAUDIO1 Clock Register
/	0x00C0	/
USBPHY_CFG_REG	0x00CC	USBPHY Configuration Register
EMAC_CLK_REG	0x00D0	EMAC Clock Register
MDFS_CLK_REG	0x00F0	MDFS Clock Register
DRAM_CFG_REG	0x00F4	DRAM Configuration Register
DRAM_GATING_REG	0x0100	DRAM Clock Gating Register
BE0_SCLK_CFG_REG	0x0104	Display Backend Channel0 Clock Configuration Register
BE1_SCLK_CFG_REG	0x0108	Display Backend Channel1 Clock Configuration Register
FE0_CLK_REG	0x010C	Display Frontend Channel0 Clock Configuration Register
FE1_CLK_REG	0x0110	Display Frontend Channel1 Clock Configuration Register
MP_CLK_REG	0x0114	Mixer Processor Clock Register
LCD0_CH0_CLK_REG	0x0118	LCD0 Channel0 Clock Register
LCD1_CH0_CLK_REG	0x011C	LCD1 Channel0 Clock Register
LCD0_CH1_CLK_REG	0x012C	LCD0 Channel1 Clock Register
LCD1_CH1_CLK_REG	0x0130	LCD1 Channel1 Clock Register
CSI0_CLK_REG	0x0134	CSI Channel0 Clock Register
CSI1_CLK_REG	0x0138	CSI Channel1 Clock Register
VE_CLK_REG	0x013C	Video Engine Clock Register
AUDIO_CODEC_CLK_REG	0x0140	Audio Codec Clock Register
AVS_CLK_REG	0x0144	AVS Clock Register
DIGITAL_MIC_CLK_REG	0x0148	Digital Mic Clock Register
HDMI_CLK_REG.	0x0150	HDMI Clock Register
PS_CLK_REG	0x0154	PS Clock Register
/	0x0158	/
MBUS_SCLK_CFG0_REG	0x015C	MBUS Clock Control 0 register
MBUS_SCLK_CFG1_REG	0x0160	MBUS Clock Control 1 register
MIPI_DSI_CLK_REG	0x0168	MIPI_DSI Clock Register
MIPI_CSI0_CLK_REG	0x016C	MIPI_CSI 0 Clock Register

DRC0_SCLK_CFG_REG	0x0180	DRC0 Special Clock Configuration Register
DRC1_SCLK_CFG_REG	0x0184	DRC1 Special Clock Configuration Register
DEU0_SCLK_CFG_REG	0x0188	DEU0 Special Clock Configuration Register
DEU1_SCLK_CFG_REG	0x018C	DEU1 Special Clock Configuration Register
GPU_CORE_CLK_REG	0x01A0	GPU Core Clock Register
GPU_MEM_CLK_REG	0x01A4	GPU Memory Clock Register
GPU_HYD_CLK_REG	0x01A8	GPU HYD Clock Register
ATS_CLK_REG	0x01B0	ATS Clock Register
TRACE_CLK_REG	0x01B4	Trace Clock Register
PLL_LOCK_CFG_REG	0x0200	PLL(Except PLL1) Lock Time Control Register
PLL1_LOCK_CFG_REG	0x0204	PLL1 Lock Time Control Register
PLL1_BIAS_REG	0x0220	PLL1 BIAS Register
PLL2_BIAS_REG	0x0224	PLL2 BIAS Register
PLL3_BIAS_REG	0x0228	PLL3 BIAS Register
PLL4_BIAS_REG	0x022C	PLL4 BIAS Register
PLL5_BIAS_REG	0x0230	PLL5 BIAS Register
PLL6_BIAS_REG	0x0234	PLL6 BIAS Register
PLL7_BIAS_REG	0x0238	PLL7 BIAS Register
PLL8_BIAS_REG	0x023C	PLL8 BIAS Register
MIPI_PLL_BIAS_REG	0x0240	MIPI PLL BIAS Register
PLL9_BIAS_REG	0x0244	PLL9 BIAS Register
PLL10_BIAS_REG	0x0248	PLL10 BIAS Register
PLL1_PAT_CFG_REG	0x0280	PLL1-PATTERN Control Register
PLL2_PAT_CFG_REG	0x0284	PLL2-PATTERN Control Register
PLL3_PAT_CFG_REG	0x0288	PLL3-PATTERN Control Register
PLL4_PAT_CFG_REG	0x028C	PLL4-PATTERN Control Register
PLL5_PAT_CFG_REG	0x0290	PLL5-PATTERN Control Register
PLL7_PAT_CFG_REG	0x0298	PLL7-PATTERN Control Register
PLL8_PAT_CFG_REG	0x029C	PLL8-PATTERN Control Register

MIPI_PLL_PAT_CFG_REG	0x02A0	MIPI_PLL PATTERN Control Register
PLL9_PAT_CFG_REG	0x02A4	PLL9-PATTERN Control Register
PLL10_PAT_CFG_REG	0x02A8	PLL10-PATTERN Control Register
AHB1_RST_REG0	0x02C0	AHB1 Module Software Reset Register0
AHB1_RST_REG1	0x02C4	AHB1 Module Software Reset Register1
AHB1_RST_REG2	0x02C8	AHB1 Module Software Reset Register2
APB1_RST_REG	0x02D0	APB1 Module Software Reset Register
APB2_RST_REG	0x02D8	APB2 Module Software Reset Register
CLK_OUTA_REG	0x0300	Clock OUTA Register
CLK_OUTB_REG	0x0304	Clock OUTB Register
CLK_OUTC_REG	0x0308	Clock OUTC Register

3.4.4. CCU REGISTER DESCRIPTION

3.4.4.1. PLL1_CFG REGISTER (DEFAULT: 0X00001000)

Offset: 0x00			Register Name: PLL1_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL1_ENABLE. 0: Disable, 1: Enable. The PLL1 output= (24MHz*N*K)/(M). The PLL1 output is for the CPU0_1_2_3 CLK. Note: the PLL output clock must be in the range of 200MHz~2.6GHz, Its default is 408MHz.
30:29	/	/	/
28	R	0x0	LOCK 0: unlocked 1: locked (It indicates that the PLL has been stable.)

27:25	/	/	/
24	R/W	0x0	CPU_SIGMA_DELTA_EN. 0: disable. 1: enable.
23:13	/	/	/
12:8	R/W	0x10	PLL_FACTOR_N PLL Factor N. Factor=0, N=1; Factor=1, N=2; Factor=2, N=3; …… Factor=31,N=32
7:6	/	/	/
5:4	R/W	0x0	PLL_FACTOR_K. PLL Factor K.(K=Factor + 1) The range is from 1 to 4.
3:2	/	/	/
1:0	R/W	0x0	PLL_FACTOR_M. PLL Factor M. (M=Factor + 1) The range is from 1 to 4.

3.4.4.2. PLL2-AUDIO REGISTER (DEFAULT:0X00035514)

Offset: 0x08			**Register Name: PLL2_CFG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL2_ENABLE. 0: Disable, 1: Enable. The PLL2 is for Audio. The PLL2 Output = 24MHz*N/ (P*M). **Notes:** In the CCU, the PLL2(8X) Output = 24MHz*N*2/M.

			The PLL output clock must be in the range of 20MHz~200MHz, Its default is 24.571MHz.
30:29	/	/	/
28	R	0x0	LOCK. 0: unlocked 1: locked (It indicates that the PLL has been stable.)
27:25	/	/	/
24	R/W	0x0	PLL_SDM_EN. 0: Disable. 1: Enable, In this case, the PLL_FACTOR_N only low 4 bits are valid (N: The range is from 1 to 16).
23:20	/	/	/
19:16	R/W	0x3	PLL_POSTDIV_P. Post-div factor (P= Factor+1) The range is from 1 to 16.
15	/	/	/
14:8	R/W	0x55	PLL_FACTOR_N. PLL Factor N. Factor=0, N=1; Factor=1, N=2; …… Factor=127, N=128;
7:5	/	/	/
4:0	R/W	0x14	PLL_PREDIV_M. Pre-div factor(M = Factor+1). The range is from 1 to 32

3.4.4.3. PLL3-VIDEO 0 REGISTER (DEFAULT:0X03006207)

Offset: 0x10	Register Name: PLL3_CFG_REG

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL3_ENABLE. 0: Disable, 1: Enable. In the integer mode, The PLL3 output = (24MHz*N)/M. In the fractional mode, the PLL3 output is select by bit 25. Note: In the CCU, PLL3(1X) output=PLL3 while PLL3(2X) output=PLL3 * 2. the PLL output clock must be in the range of 30MHz~600MHz, Its default is 297MHz.
30	R/W	0x0	PLL_MODE. 0: Manual Mode. 1: Auto Mode (Controlled by DE).
29	/	/	/
28	R	0x0	LOCK. 0: unlocked. 1: locked (It indicates that the PLL has been stable.)
27:26	/	/	/
25	R/W	0x1	FRAC_CLK_OUT. PLL clock output when PLL_MODE_SEL=0; no meaning when PLL_MODE_SEL =1. 0: pllout=270MHz; 1: pllout=297MHz.
24	R/W	0x1	PLL_MODE_SEL. 0: Fractional mode. 1: Integer mode.
23:21	/	/	/
20	R/W	0x0	PLL_SDM_EN. 0: Disable, 1: Enable.

19:15	/	/	/
14:8	R/W	0x62	PLL_FACTOR_N. PLL Factor N. Factor=0, N=1; Factor=1, N=2; Factor=2, N=3; …… Factor=127,N=128
7:4	/	/	/
3:0	R/W	0x7	PLL_PREDIV_M. PLL pre-divider(M = Factor+1). The range is from 1 to 16.

3.4.4.4. PLL4-VE REGISTER (DEFAULT:0X03006207)

Offset: 0x18			Register Name: PLL4_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL4_ENABLE. 0: Disable, 1: Enable. In the integer mode, The PLL4 output = (24MHz*N)/M. In the fractional mode, the PLL4 output is select by bit 25. Note: The PLL output clock must be in the range of 30MHz~600MHz, Its default is 297MHz.
30:29	/	/	/
28	R	0x0	LOCK 0: unlocked 1: locked (It indicates that the PLL has been stable.)
27:26	/	/	/
25	R/W	0x1	FRAC_CLK_OUT. PLL clock output when PLL_MODE_SEL=0; no meaning when

			PLL_MODE_SEL =1. 0: pllout=270MHz; 1: pllout=297MHz.
24	R/W	1	PLL_MODE_SEL. 0: Fractional mode. 1: Integer mode.
23:21	/	/	/
20	R/W	0x0	PLL_SDM_EN. 0: Disable, 1: Enable.
19:15	/	/	/
14:8	R/W	0x62	PLL_FACTOR_N. PLL Factor N. Factor=0, N=1; Factor=1, N=2; Factor=2, N=3 …… Factor=31,N=32 … Factor=127,N=128
7:4	/	/	/.
3:0	R/W	0x7	PLL_PREDIV_M. PLL pre-divider (M = Factor+1). The range is from 1 to 16.

3.4.4.5. PLL5-DDR REGISTER (DEFAULT:0X00001000)

Offset: 0x20			**Register Name: PLL5_CFG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL5_ENABLE. 0: Disable, 1: Enable.

			Set bit20 to validate the PLL5 after this bit is set to 1. the PLL5 output for SDRAM = (24MHz*N*K)/M. Note: the PLL output clock must be in the range of 200MHz~2.6GHz, Its default is 408MHz.
30:29	/	/	/
28	R	0x0	LOCK 0: unlocked 1: locked (It indicates that the PLL has been stable.)
27:25	/	/	/
24	R/W	0x0	SDRAM_SIGMA_DELTA_EN. 0: Disable. 1: Enable.
23:21	/	/	/
20	R/W	0x0	SDRPLL_UPD. SDRPLL Configuration Update. Note: After the PLL5 enabled, this bit should be set to 1 to validate PLL5, otherwise the PLL5 is invalid. It will be auto cleared after the PLL5 is valid. 0: No effect. 1: To validate PLL5.
19:13	/	/	/
12:8	R/W	0x10	PLL_FACTOR_N. PLL Factor N. Factor=0, N=1; Factor=1, N=2; Factor=2, N=3; …… Factor=31,N=32

7:6	/	/	/
5:4	R/W	0x0	PLL_FACTOR_K. PLL Factor K.(K=Factor + 1) The range is from 1 to 4.
3:2	/	/	/
1:0	R/W	0x0	PLL_FACTOR_M. PLL Factor M.(M = Factor + 1) The range is from 1 to 4.

3.4.4.6. PLL6-PERIPHERAL REGISTER (DEFAULT:0X00041811)

Offset: 0x28			**Register Name: PLL6_CFG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL6_ENABLE. 0: Disable, 1: Enable. The PLL6 Output = 24MHz*N*K/2. Notes: The PLL6 output should be fixed to 600MHz, and is not recommended to be modified. In the CCU, PLL6(2X) output= PLL6*2 = 24MHz*N*K. The PLL output clock must be in the range of 200MHz~1.8GHz, and default to be 600MHz.
30:29	/	/	/
28	R	0x0	LOCK. 0: unlocked 1: locked (indicating that the PLL has been stable.)
27:26	/	/	/
25	R/W	0x0	PLL_BYPASS_EN. PLL Output Bypass Enable. 0: Disable, 1: Enable. If the bypass is enabled, the PLL output is 24MHz.

24	R/W	0x0	PLL_CLK_OUT_EN. PLL clock output enable.(Just for the SATA Phy) 0: Disable, 1: Enable.
23:19	/	/	/
18	R/W	0x1	PLL_24M_OUT_EN. PLL 24MHz output enable. 0: Disable, 1: Enable. When 25MHz crystal is used, this PLL can output 24MHz.
17:16	R/W	0x0	PLL_24M_POST_DIV. PLL 24M output clock post divider (when 25MHz crystal is used). 1/2/3/4.
15:13	/	/	/
12:8	R/W	0x18	PLL_FACTOR_N. PLL Factor N. Factor=0, N=1; Factor=1, N=2; Factor=2, N=3; …… Factor=31,N=32
7:6	/	/	/
5:4	R/W	0x1	PLL_FACTOR_K. PLL Factor K.(K=Factor + 1) The range is from 1 to 4.
3:2	/	/	/
1:0	R/W	0x1	/

3.4.4.7. PLL7-VIDEO 1 REGISTER (DEFAULT:0X03006207)

Offset: 0x30	Register Name: PLL7_CFG_REG

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL7_ENABLE. 0: Disable, 1: Enable. In the integer mode, The PLL7 output = (24MHz*N)/M. Note: In the fractional mode, the PLL7 output is select by bit 25. In the CCU, PLL7(1X) output=PLL7 while PLL7(2X) output =PLL7 * 2. The PLL output clock must be in the range of 30MHz~600MHz, and default to be 297MHz.
30	R/W	0x0	PLL_MODE. 0: Manual Mode. 1: Auto Mode (Controlled by DE).
29	/	/	/
28	R	0x0	LOCK. 0: unlocked 1: locked (It indicates that the PLL has been stable.)
27:26	/	/	/
25	R/W	0x1	FRAC_CLK_OUT. PLL clock output when PLL_MODE_SEL=0; no meaning when PLL_MODE_SEL =1. 0: pllout=270MHz; 1: pllout=297MHz.
24	R/W	0x1	PLL_MODE_SEL. 0: Fractional mode. 1: Integer mode.
23:21	/	/	/
20	R/W	0x0	PLL_SDM_EN. 0: Disable, 1: Enable.
19:15	/	/	/

14:8	R/W	0x62	PLL_FACTOR_N PLL Factor N. Factor=0, N=1; Factor=1, N=2; Factor=2, N=3; …… Factor=127,N=128
7:4	/	/	/
3:0	R/W	0x7	PLL_PRE_DIV_M. PLL pre-divider (M = Factor+1). The range is from 1 to 16.

3.4.4.8. PLL8-GPU REGISTER (DEFAULT:0X03006207)

Offset: 0x38			Register Name: PLL8_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL8_ENABLE. 0: Disable, 1: Enable. In the integer mode, PLL8 output= (24MHz*N)/M. In the fractional mode, PLL8 output is select by bit 25. Notes: The PLL output clock must be in the range of 30MHz~600MHz, and default to be 297MHz.
30:29	/	/	/
28	R	0x0	LOCK 0: unlocked 1: locked (It indicates that the PLL has been stable.)
27:26	/	/	/
25	R/W	0x1	FRAC_CLK_OUT. PLL clock output when PLL_MODE_SEL=0; no special meaning when PLL_MODE_SEL =1.

			0: pllout=270MHz; 1: pllout=297MHz.
24	R/W	0x1	PLL_MODE_SEL. 0: Fractional mode. 1: Integer mode.
23:21	/	/	/
20	R/W	0x0	PLL_SDM_EN. 0: Disable, 1: Enable.
19:15	/	/	/
14:8	R/W	0x62	PLL_FACTOR_N PLL Factor N. Factor=0, N=1; Factor=1, N=2; Factor=2, N=3 …… Factor=127,N=128
7:4	/	/	/
3:0	R/W	0x7	PLL_PRE_DIV_M. PLL pre-divider (M = Factor+1). The range is from 1 to 16.

3.4.4.9. MIPI_PLL CONTROL REGISTER (DEFAULT:0X00000502)

Offset: 0x40			Register Name: MIPI_PLL_CFG_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MIPI_PLL_ENABLE. 0: Disable, 1: Enable. When VFB_SEL=0 (MIPI mode), PLL output= (PLL_SRC*N*K)/M; When VFB_SEL=1, PLL output depends on these bits:

			sint_frac,sdiv2, s6p25_7p5 , pll_feedback_div.
30:29	/	/	/
28	R	0x0	LOCK. 0: unlocked 1: locked (It indicates that the PLL has been stable.)
27	R/W	0x0	SINT_FRAC. When VFB_SEL=1, PLL mode control, otherwise, it has no special meaning. 0: Integer mode 1: Fractional mode
26	R/W	0x0	SDIV2. PLL clock output when VFB_SEL=1; no meaning when VFB_SEL =0 0: PLL output 1: PLL output X2.
25	R/W	0x0	S6P25_7P5. PLL Output is selected by this bit when VFB_SEL=1 and SINT_FRAC=1, otherwise, it has no special meaning. 0: pllout=pllinput*6.25 1: pllout=pllinput*7.5.
24	/	/	/
23	R/W	0	LDO1_EN. On-chip LDO1 Enable.
22	R/W	0	LDO2_EN. On-chip LDO2 Enable.
21	R/W	0	PLL_SRC. PLL Source Select. 0: VIDEO PLL0 (PLL3) 1: VIDEO PLL1 (PLL7).

20	R/W	0x0	PLL_SDM_EN. 0: Disable, 1: Enable.
19:18	/	/	/
17	R/W	0x0	PLL_FEEDBACK_DIV. PLL feed-back divider control. PLL clock output when VFB_SEL=1; no meaning when VFB_SEL =0 0:divided by 5 1:divided by 7
16	R/W	0x0	VFB_SEL. 0: MIPI mode(N, K, M valid) 1:HDMI mode(sint_frac,sdiv2,s6p25_7p5 , pll_feedback_div valid)
15:12	/	/	/
11:8	R/W	0x5	PLL_FACTOR_N PLL Factor N. Factor=0, N=1; Factor=1, N=2; …… Factor=15,N=16
7:6	/	/	/
5:4	R/W	0x0	PLL_FACTOR_K. PLL Factor K.(K=Factor + 1) The range is from 1 to 4.
3:0	R/W	0x2	PLL_PRE_DIV_M. PLL Pre-divider Factor (M = Factor+1). The range is from 1 to 16.

3.4.4.10. PLL9 REGISTER (DEFAULT:0X03006207)

Offset: 0x44	Register Name: PLL9_CFG_REG

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL9_ENABLE. 0: Disable, 1: Enable. In the integer mode, The PLL9 output= (24MHz*N)/M. In the fractional mode, the PLL9 output is select by bit 25. Notes: The PLL output clock must be in the range of 30MHz~600MHz. Its default is 297MHz.
30:29	/	/	/
28	R	0x0	LOCK 0: unlocked 1: locked (It indicates that the PLL has been stable.)
27:26	/	/	/
25	R/W	0x1	FRAC_CLK_OUT. PLL clock output when PLL_MODE_SEL=0; no meaning when PLL_MODE_SEL =1. 0: pllout=270MHz; 1: pllout=297MHz.
24	R/W	0x1	PLL_MODE_SEL. 0: Fractional mode. 1: Integer mode.
23:21	/	/	/
20	R/W	0x0	PLL_SDM_EN. 0: Disable, 1: Enable.
19:15	/	/	/
14:8	R/W	0x62	PLL_FACTOR_N PLL Factor N. Factor=0, N=1; Factor=1, N=2; Factor=2, N=3

			…… Factor=0x7F,N=128
7:4	/	/	/
3:0	R/W	0x7	PLL_PRE_DIV_M. PLL pre-divider (M = Factor+1). The range is from 1 to 16.

3.4.4.11. PLL10 REGISTER (DEFAULT:0X03006207)

Offset: 0x48			Register Name: PLL10_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL10_ENABLE. 0: Disable, 1: Enable. In the integer mode, The PLL10 output= (24MHz*N)/M. In the fractional mode, the PLL10 output is select by bit 25. Note: The PLL output clock must be in the range of 30MHz~600MHz. Its default is 297MHz.
30:29	/	/	/
28	R	0x0	LOCK 0: unlocked 1: locked (It indicates that the PLL has been stable.)
27:26	/	/	/
25	R/W	0x1	FRAC_CLK_OUT. PLL clock output when PLL_MODE_SEL=0; no meaning when PLL_MODE_SEL =1. 0: pllout=270MHz; 1: pllout=297MHz.
24	R/W	0x1	PLL_MODE_SEL. 0: Fractional mode. 1: Integer mode.

23:21	/	/	/
20	R/W	0x0	PLL_SDM_EN. 0: Disable, 1: Enable.
19:15	/	/	/
14:8	R/W	0x62	PLL_FACTOR_N PLL Factor N. Factor=0, N=1; Factor=1, N=2; Factor=2, N=3 …… Factor=0x7F,N=128
7:4	/	/	/
3:0	R/W	0x7	PLL_PRE_DIV_M. PLL pre-divider (M = Factor+1). The range is from 1 to 16.

3.4.4.12. CPU /AXI CLOCK RATIO REGISTER (DEFAULT: 0X00010000)

Offset: 0x50			**Register Name: CPU_AXI_CFG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:16	R/W	0x1	CPU_CLK_SRC_SEL. CPU0/1/2/3 Clock Source Select. 00: LOSC 01: OSC24M 10: PLL1 11: PLL1 If the clock source is changed, wait for at most 8 present running clock cycles.
15:10	/	/	/

9:8	R/W	0x0	ATB_APB_CLK_DIV. 00: /1 01: /2 1x: /4 Note: System ATB/APB clock source is CPU clock source.
7:3	/	/	/
2:0	R/W	0x0	AXI_CLK_DIV_RATIO. AXI Clock divide ratio. AXI Clock source is CPU clock source. 000: /1 001: /2 010: /3 011: /4 1xx: /4

3.4.4.13. AHB1/APB1 CLOCK RATIO REGISTER (DEFAULT: 0X00001010)

Offset: 0x54			Register Name: AHB1_APB1_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x1	AHB1_CLK_SRC_SEL. 00: LOSC 01: OSC24M 10: AXI 11: PLL6/ AHB1_PRE_DIV.
11:10	/	/	/
9:8	R/W	0x0	APB1_CLK_RATIO. APB1 Clock divide ratio. APB1 clock source is AHB1 clock. 00: /2 01: /2

			10: /4 11: /8
7:6	R/W	0x0	AHB1_PRE_DIV AHB1 clock pre-divide ratio 00: /1 01: /2 10: /3 11: /4
5:4	R/W	0x1	AHB1_CLK_DIV_RATIO. AHB1 Clock divide ratio. 00: /1 01: /2 10: /4 11: /8
3:0	/	/	/

3.4.4.14. APB2 CLOCK DIVIDE RATIO REGISTER (DEFAULT: 0X01000000)

Offset: 0x58			Register Name: APB2_CLK_DIV_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x1	APB2_CLK_SRC_SEL. APB2 Clock Source Select 00: LOSC 01: OSC24M 10: PLL6 11: PLL6 This clock is used for some special module apbclk(UART,TWI), because these modules need special clock rate if the apb1clk has changed.

23:18	/	/	/
17:16	R/W	0x0	CLK_RAT_N Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:5	/	/	/
4:0	R/W	0x0	CLK_RAT_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider can be 1 to 32.

3.4.4.15. AHB1 MODULE CLOCK GATING REGISTER 0(DEFAULT: 0X00000000)

Offset: 0x60			Register Name: AHB1_GATING_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	Gating AHB Clock for USB OHCI2(0: mask, 1: pass).
30	R/W	0x0	Gating AHB Clock for USB OHCI1(0: mask, 1: pass).
29	R/W	0x0	Gating AHB Clock for USB OHCI0(0: mask, 1: pass).
28	/	/	/
27	R/W	0x0	Gating AHB Clock for USB EHCI1 (0: mask, 1: pass).
26	R/W	0x0	Gating AHB Clock for USB EHCI0 (0: mask, 1: pass).
25	/	/	/
24	R/W	0x0	Gating AHB Clock for USB-DRD(0: mask, 1: pass).
23	R/W	0x0	SPI3_AHB_GATING Gating AHB Clock for SPI3(0: mask, 1: pass).
22	R/W	0x0	SPI2_AHB_GATING. Gating AHB Clock for SPI2(0: mask, 1: pass).
21	R/W	0x0	SPI1_AHB_GATING. Gating AHB Clock for SPI1(0: mask, 1: pass).
20	R/W	0x0	SPI0_AHB_GATING.

			Gating AHB Clock for SPI0(0: mask, 1: pass).
19	R/W	0x0	HSTMR_AHB_GATING. Gating AHB Clock for High Speed Timer (0: mask, 1: pass).
18	R/W	0x0	TS_AHB_GATING. Gating AHB Clock for TS(0: mask, 1: pass).
17	R/W	0x0	EMAC_AHB_GATING. Gating AHB Clock for EMAC(0: mask, 1: pass).
16:15	/	/	/
14	R/W	0x0	SDRAM_AHB_GATING. Gating AHB Clock for SDRAM(0: mask, 1: pass).
13	R/W	0x0	NAND0_AHB_GATING. Gating AHB Clock for NAND0(0: mask, 1: pass).
12	R/W	0x0	NAND1_AHB_GATING. Gating AHB Clock for NAND1(0: mask, 1: pass).
11	R/W	0x0	SD3_AHB_GATING. Gating AHB Clock for SD/MMC3(0: mask, 1: pass).
10	R/W	0x0	SD2_AHB_GATING. Gating AHB Clock for SD/MMC2(0: mask, 1: pass).
9	R/W	0x0	SD1_AHB_GATING. Gating AHB Clock for SD/MMC1(0: mask, 1: pass).
8	R/W	0x0	SD0_AHB_GATING. Gating AHB Clock for SD/MMC0(0: mask, 1: pass).
7	/	/	/
6	R/W	0x0	DMA_AHB_GATING. Gating AHB Clock for DMA(0: mask, 1: pass).
5	R/W	0x0	SS_AHB_GATING. Gating AHB Clock for SS(0: mask, 1: pass).
4:2	/	/	/
1	R/W	0x0	MIPIDSI_AHB_GATING.

			Gating AHB Clock for MIPI DSI(0: mask, 1: pass).
0	/	/	/

3.4.4.16. AHB1 MODULE CLOCK GATING REGISTER 1(DEFAULT: 0X00000000)

Offset: 0x64			Register Name: AHB1_GATING_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26	R/W	0x0	DRC1_AHB_GATING. Gating AHB Clock for DRC1 (0: mask, 1: pass).
25	R/W	0x0	DRC0_AHB_GATING. Gating AHB Clock for DRC0 (0: mask, 1: pass).
24	R/W	0x0	DEU1_AHB_GATING. Gating AHB Clock for DEU1 (0: mask, 1: pass).
23	R/W	0x0	DEU0_AHB_GATING. Gating AHB Clock for DEU0 (0: mask, 1: pass).
22:21	R/W	0x0	/
20	R/W	0x0	GPU_AHB_GATING. Gating AHB Clock for GPU (0: mask, 1: pass).
19	/	/	/
18	R/W	0x0	MP_AHB_GATING. Gating AHB Clock for MP (0: mask, 1: pass).
17:16	/	/	/
15	R/W	0x0	FE1_AHB_GATING. Gating AHB Clock for DE-FE1 (0: mask, 1: pass).
14	R/W	0x0	FE0_AHB_GATING. Gating AHB Clock for DE-FE0 (0: mask, 1: pass).
13	R/W	0x0	BE1_AHB_GATING. Gating AHB Clock for DE-BE1 (0: mask, 1: pass).
12	R/W	0x0	BE0_AHB_GATING.

			Gating AHB Clock for DE-BE0 (0: mask, 1: pass).
11	R/W	0x0	HDMI_AHB_GATING. Gating AHB Clock for HDMI (0: mask, 1: pass).
10:9	/	/	/
8	R/W	0x0	CSI_AHB_GATING. Gating AHB Clock for CSI0/CSI1/MIPICSI0 (0: mask, 1: pass).
7:6	/	/	/
5	R/W	0x0	LCD1_AHB_GATING. Gating AHB Clock for LCD1 (0: mask, 1: pass).
4	R/W	0x0	LCD0_AHB_GATING. Gating AHB Clock for LCD0 (0: mask, 1: pass).
3:1	/	/	/
0	R/W	0x0	VE_AHB_GATING. Gating AHB Clock for VE (0: mask, 1: pass).

3.4.4.17. APB1 MODULE CLOCK GATING REGISTER (DEFAULT: 0X00000000)

Offset: 0x68			Register Name: APB1_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/.
13	R/W	0x0	DAUDIO1_APB_GATING. Gating APB Clock for DAUDIO1 (0: mask, 1: pass).
12	R/W	0x0	DAUDIO0_APB_GATING. Gating APB Clock for DAUDIO0 (0: mask, 1: pass).
11:6	/	/	/
5	R/W	0x0	PIO_APB_GATING. Gating APB Clock for PIO (0: mask, 1: pass).
4	R/W	0x0	DIGITAL_MIC_APB_GATING. Gating APB Clock for Digital MIC (0: mask, 1: pass).
3:2	/	/	/

1	R/W	0x0	/
0	R/W	0x0	AUDIO_CODEC_APB_GATING. Gating APB Clock for Audio CODEC (0: mask, 1: pass).

3.4.4.18. APB2 MODULE CLOCK GATING REGISTER (DEFAULT: 0X00000000)

Offset: 0x6C			Register Name: APB2_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/.
21	R/W	0x0	UART5_APB_GATING. Gating APB Clock for UART5(0: mask, 1: pass).
20	R/W	0x0	UART4_APB_GATING. Gating APB Clock for UART4(0: mask, 1: pass).
19	R/W	0x0	UART3_APB_GATING. Gating APB Clock for UART3(0: mask, 1: pass).
18	R/W	0x0	UART2_APB_GATING. Gating APB Clock for UART2(0: mask, 1: pass).
17	R/W	0x0	UART1_APB_GATING. Gating APB Clock for UART1(0: mask, 1: pass).
16	R/W	0x0	UART0_APB_GATING. Gating APB Clock for UART0(0: mask, 1: pass).
15:4	/	/	/
3	R/W	0x0	TWI3_APB_GATING. Gating APB Clock for TWI3(0: mask, 1: pass).
2	R/W	0x0	TWI2_APB_GATING. Gating APB Clock for TWI2(0: mask, 1: pass).
1	R/W	0x0	TWI1_APB_GATING. Gating APB Clock for TWI1(0: mask, 1: pass).
0	R/W	0x0	TWI0_APB_GATING. Gating APB Clock for TWI0(0: mask, 1: pass).

3.4.4.19. NAND0 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x80			Register Name: NAND0_SCLK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: / 11: /.
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

Notes: In practical application, the module clock frequency is always switched off.

3.4.4.20. NAND1 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x84			Register Name: NAND1_SCLK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: / 11: /.
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

Notes: In application, the module clock frequency is always switched off.

3.4.4.21. SD/MMC 0 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x88	Register Name: SD0_CLK_REG

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: / 11: /.
23	/	/	/
22:20	R/W	0x0	SAMPLE_CLK_PHASE_CTR. Sample Clock Phase Control. The sample clock phase delay is based on the number of source clock that is from 0 to 7.
19:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:11	/	/	/
10:8	R/W	0x0	OUTPUT_CLK_PHASE_CTR. Output Clock Phase Control. The output clock phase delay is based on the number of source clock that is from 0 to 7.
7:4	/	/	/

3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.22. SD/MMC 1 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x8C			Register Name: SD1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: / 11: /.
23	/	/	/
22:20	R/W	0x0	CLK_PHASE_CTR. Sample Clock Phase Control. The sample clock phase delay is based on the number of source clock that is from 0 to 7.
19:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is

			1/2/4/8.
15:11	/	/	/
10:8	R/W	0x0	OUTPUT_CLK_PHASE_CTR. Output Clock Phase Control. The output clock phase delay is based on the number of source clock that is from 0 to 7.
7:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.23. SD/MMC 2 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x90			Register Name: SD2_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: / 11: /.
23	/	/	/
22:20	R/W	0x0	CLK_PHASE_CTR.

			Sample Clock Phase Control. The sample clock phase delay is based on the number of source clock that is from 0 to 7.
19:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:11	/	/	/
10:8	R/W	0x0	OUTPUT_CLK_PHASE_CTR. Output Clock Phase Control. The output clock phase delay is based on the number of source clock that is from 0 to 7.
7:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.24. SD/MMC 3 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x94			Register Name: SD3_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL.

			Clock Source Select 00: OSC24M 01: PLL6 10: / 11: /
23	/	/	/
22:20	R/W	0x0	CLK_PHASE_CTR. Sample Clock Phase Control. The sample clock phase delay is based on the number of source clock that is from 0 to 7.
19:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:11	/	/	/
10:8	R/W	0x0	OUTPUT_CLK_PHASE_CTR. Output Clock Phase Control. The output clock phase delay is based on the number of source clock that is from 0 to 7.
7:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.25. TS CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x98			Register Name: TS_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: / 11: /
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.26. SS CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x9C			Register Name: SS_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF

			1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: / 11: /.
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.27. SPI0 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0xA0			Register Name: SPI0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/

25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: / 11: /.
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.28. SPI1 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0xA4			Register Name: SPI1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M

			01: PLL6 10: / 11: /.
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.29. SPI2 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0xA8			Register Name: SPI2_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: / 11: /.

23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.30. SPI3 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0xAC			Register Name: SPI3_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: / 11: /.
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n)

			The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.31. DAUDIO-0 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0xB0			Register Name: DAUDIO0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON
30:18	/	/	/
17:16	R/W	0x0	CLK_SRC_SEL. 00: PLL2 (8X) 01: PLL2(8X)/2 10: PLL2(8X)/4 11: PLL2(1X)
15:0	/	/	/.

3.4.4.32. DAUDIO-1 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0xB4			Register Name: DAUDIO1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF

			1: Clock is ON
30:18	/	/	/
17:16	R/W	0x0	CLK_SRC_SEL. 00: PLL2 (8X) 01: PLL2(8X)/2 10: PLL2(8X)/4 11: PLL2(1X)
15:0	/	/	/.

3.4.4.33. USBPHY CONFIGURATION REGISTER(DEFAULT: 0X00000000)

Offset: 0xCC			Register Name: USBPHY_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0x0	SCLK_GATING_OHCI2. Gating Special Clock for OHCI2 0: Clock is OFF 1: Clock is ON
17	R/W	0x0	SCLK_GATING_OHCI1. Gating Special Clock for OHCI1 0: Clock is OFF 1: Clock is ON
16	R/W	0x0	SCLK_GATING_OHCI0. Gating Special Clock for OHCI0 0: Clock is OFF 1: Clock is ON
15:11	/	/	/
10	R/W	0x0	SCLK_GATING_USBPHY2. Gating Special Clock for USB PHY2 0: Clock is OFF

			1: Clock is ON
9	R/W	0x0	SCLK_GATING_USBPHY1. Gating Special Clock for USB PHY1 0: Clock is OFF 1: Clock is ON
8	R/W	0x0	SCLK_GATING_USBPHY0. Gating Special Clock for USB PHY0 0: Clock is OFF 1: Clock is ON
7:3	/	/	/
2	R/W	0x0	USBPHY2_RST. USB PHY2 Reset Control 0: Assert 1: De-assert
1	R/W	0x0	USBPHY1_RST. USB PHY1 Reset Control 0: Assert 1: De-assert
0	R/W	0x0	USBPHY0_RST. USB PHY0 Reset Control 0: Assert 1: De-assert

3.4.4.34. EMAC CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0xD0			Register Name: EMAC_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:5	R/W	0	GRXDC Configure EMAC Receive Clock Delay Chian.

			000: 001: … 111:
4	R/W	0	GRXIE Enable EMAC Receive Clock Invertor. 0: Disable; 1: Enable;
3	R/W	0	GTXIE Enable EMAC Transmit Clock Invertor. 0: Disable; 1: Enable;
2	R/W	0	GPIT EMAC PHY Interface Type 0: GMII/MII; 1: RGMII;
1:0	R/W	0	GTCS EMAC Transmit Clock Source 00: Transmit clock source for MII; 01: External transmit clock source for GMII and RGMII; 10: Internal transmit clock source for GMII and RGMII; 11: Reserved;

3.4.4.35. MDFS CLK REGISTER (DEFAULT: 0X01000002)

Offset: 0xF0			Register Name: MDFS_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CLK_GATING. Gating Clock 0: Clock is OFF

			1: Clock is ON This clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x1	CLK_SRC_SEL. Clock Source Select 00: PLL5 01: PLL6 10: / 11: /.
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x2	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.36. DRAM CFG REGISTER (DEFAULT: 0X00000000)

Offset: 0xF4			Register Name: DRAM_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SDRAM_CTR_RST. Sdram Controller Reset. 0: assert, 1: de-assert.
30:17	/	/	/
16	R/W	0x0	SDRCLK_UPD. SDRCLK Configuration 0 update.

			0:Invalid 1:Valid. Note: Set this bit will validate Configuration 0. It will be auto cleared after the Configuration 0 is valid.
15:13	/	/	/
12	R/W	0x0	SDRCLK_SEL0. SDRCLK Source Select of Configuration 0 0: PLL5 1: PLL6
11:8	R/W	0x0	CLK_DIV0_M. SDRCLK Divider of Configuration 0 The clock is divided by (m+1). The divider is from 1 to 16.
7:5	/	/	/
4	R/W	0x0	SDRCLK_SEL1. SDRCLK Source Select of Configuration 1 0: PLL5 1: PLL6
3:0	R/W	0x0	CLK_DIV1_M. SDRCLK Divider of Configuration 1. The clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.37. DRAM CLK GATING REGISTER (DEFAULT: 0X00000000)

Offset: 0x100			Register Name: DRAM_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	DE_MP_DCLK_GATING. Gating DRAM Clock for DE_MP(0: mask, 1: pass).
27	R/W	0x0	BE1_DCLK_GATING. Gating DRAM Clock for DE_BE1(0: mask, 1: pass).

26	R/W	0x0	BE0_DCLK_GATING. Gating DRAM Clock for DE_BE0(0: mask, 1: pass).
25	R/W	0x0	FE1_DCLK_GATING. Gating DRAM Clock for DE_FE1 (0: mask, 1: pass).
24	R/W	0x0	FE0_DCLK_GATING. Gating DRAM Clock for DE_FE0 (0: mask, 1: pass).
23:20	/	/	/.
19	R/W	0x0	DEU1_DCLK_GATING. Gating DRAM Clock for IEP DEU1 (0: mask, 1: pass).
18	R/W	0x0	DEU0_DCLK_GATING. Gating DRAM Clock for IEP DEU0 (0: mask, 1: pass).
17	R/W	0x0	DRC1_DCLK_GATING. Gating DRAM Clock for IEP DRC1 (0: mask, 1: pass).
16	R/W	0x0	DRC0_DCLK_GATING. Gating DRAM Clock for IEP DRC0 (0: mask, 1: pass).
15:4	/	/	/
3	R/W	0x0	TS_DCLK_GATING. Gating DRAM Clock for TS(0: mask, 1: pass).
2	/	/	/
1	R/W	0x0	CSI_ISP_DCLK_GATING. Gating DRAM Clock for CSI0,CSI1,MIPI_CSI0, ISP(0: mask, 1: pass).
0	R/W	0x0	VE_DCLK_GATING. Gating DRAM Clock for VE(0: mask, 1: pass).

3.4.4.38. DE-BE 0 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x104			Register Name: BE0_SCLK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING.

			Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL3 001: PLL7 010: PLL6(2X) 011: PLL8 100:PLL9 101:PLL10 110/111:Reserved.
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.39. DE-BE 1 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x108			Register Name: BE1_SCLK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M.
30:27	/	/	/

26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL3 001: PLL7 010: PLL6(2X) 011: PLL8 100:PLL9 101:PLL10 110/111:Reserved.
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.40. DE-FE 0 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x10C			Register Name: FE0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL3 001: PLL7 010: PLL6(2X)

			011: PLL8 100:PLL9 101:PLL10 110/111: Reserved.
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.41. DE-FE 1 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x110			Register Name: FE1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL3 001: PLL7 010: PLL6(2X) 011: PLL8 100:PLL9 101:PLL10 110/111: Reserved.
23:4	/	/	/

3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.42. DE-MP CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x114			Register Name: MP_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: PLL3 01: PLL7 10: PLL9 11: PLL10.
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.43. LCD 0 CH0 CLOCK (DEFAULT: 0X00000000)

Offset: 0x118			Register Name: LCD0_CH0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/ Divider M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL3(1X) 001: PLL7(1X) 010: PLL3(2X) 011: PLL7(2X) 100: MIPI_PLL 101~111: /
23:0	/	/	/

3.4.4.44. LCD 1 CH0 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x11C			Register Name: LCD1_CH0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/ Divider M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL3(1X) 001: PLL7(1X)

			010: PLL3(2X) 011: PLL7(2X) 100: MIPI_PLL 101~111: /
23:0	/	/	/

3.4.4.45. LCD 0 CH1 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x12C			Register Name: LCD0_CH1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/ Divider M.
30:26	/	/	/
25:24	R/W	0x0	SCLK_SEL. Special Clock Source Select 00: PLL3(1X) 01: PLL7(1X) 10: PLL3(2X) 11: PLL7(2X)
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.46. LCD 1 CH1 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x130	Register Name: LCD1_CH1_CLK_REG

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock=Clock Source/ Divider M.
30:26	/	/	/
25:24	R/W	0x0	SCLK_SRC_SEL. Special Clock Source Select 00: PLL3(1X) 01: PLL7(1X) 10: PLL3(2X) 11: PLL7(2X)
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.47. CSI 0 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x134			Register Name: CSI0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CSI0_SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Special Clock Source/CSI0_SCLK_DIV_M.
30:27	/	/	/
26:24	R/W	0x0	SCLK_SRC_SEL.

			Special Clock Source Select 000: PLL3(1X) 001: PLL7(1X) 010: PLL9 011: PLL10 100: MIPI_PLL 101: PLL4 110~111:/
23:20	/	/	/
19:16	R/W	0x0	CSI0_SCLK_DIV_M. CSI0 Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.
15	R/W	0x0	CSI0_MCLK_GATING. Gating Master Clock 0: Clock is OFF 1: Clock is ON This clock =Master Clock Source/ CSI0_MCLK_DIV_M.
14:11	/	/	/
10:8	R/W	0x0	MCLK_SRC_SEL. Master Clock Source Select 000: PLL3(1X) 001: PLL7(1X) 010:/ 011:/ 100: / 101: OSC24M 110~111:/
7:4	/	/	/

3:0	R/W	0x0	CSI0_MCLK_DIV_M. CSI0 Master Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.48. CSI 1 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x138			Register Name: CSI1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	CSI1_MCLK_GATING. Gating Master Clock 0: Clock is OFF 1: Clock is ON This clock =Master Clock Source/ CSI1_MCLK_DIV_M.
14:11	/	/	/
10:8	R/W	0x0	MCLK_SRC_SEL. Master Clock Source Select 000: PLL3(1X) 001: PLL7(1X) 010:/ 011:/ 100:/ 101: OSC24M 110~111:/
7:4	/	/	/
3:0	R/W	0x0	CSI1_MCLK_DIV_M. CSI1 Master Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.49. VE CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x13C			Register Name: VE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating the Special clock for VE(0: mask, 1: pass). Its clock source is the PLL4 output. This special clock = Clock Source/Divider N.
30:19	/	/	/.
18:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (N) The select clock source is pre-divided by n+1. The divider is from 1 to 8.
15:0	/	/	/

3.4.4.50. AUDIO CODEC CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x140			Register Name: AUDIO_CODEC_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = PLL2 output.
30:0	/	/	/

3.4.4.51. AVS CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x144			Register Name: AVS_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING.

			Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = OSC24M.
30:0	/	/	/

3.4.4.52. DIGITAL MIC CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x148			Register Name: DIGITAL_MIC_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = PLL2 output.
30:0	/	/	/

3.4.4.53. HDMI CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x150			Register Name: HDMI_CLK_REG.
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/ Divider M
30	R/W	0x0	DDC_CLK_GATING. 0: Clock is OFF 1: Clock is ON This DDC clock = 24MHz
29:26	/	/	/

25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: PLL3(1X) 01: PLL7(1X) 10: PLL3(2X) 11: PLL7(2X)
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.54. PS CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x154			Register Name: PS_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON Note: The clock source is LCD1 CH1 Clock.
30:0	/	/	/

3.4.4.55. MBUS CLOCK CONTROL 0 REGISTER (DEFAULT: 0X00000000)

Offset: 0x15C			Register Name: MBUS_SCLK_CFG0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MBUS_SCLK_GATING. Gating Clock for MBUS0 (Max Clock = 300MHz) 0: Clock is OFF, 1: Clock is ON;

			MBUS_CLOCK = Clock Source/Divider N/Divider M
30:26	/	/	/
25:24	R/W	0x0	MBUS_SCLK_SRC Clock Source Select 00: OSC24M 01: PLL6 10: PLL5 11: Reserved
23:18	/	/	/
17:16	R/W	0x0	MBUS_SCLK_RATIO_N Clock Pre-divide Ratio (N) The select clock source is pre-divided by 2^N. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	MBUS_SCLK_RATIO_M Clock Divide Ratio (M) The divided clock is divided by (M+1). The divider is from 1 to 16.

3.4.4.56. MBUS CLOCK CONTROL 1 REGISTER (DEFAULT: 0X00000000)

Offset: 0x160			Register Name: MBUS_SCLK_CFG1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MBUS_SCLK_GATING. Gating Clock for MBUS1 (Max Clock = 300MHz) 0: Clock is OFF, 1: Clock is ON; MBUS_CLOCK = Clock Source/Divider N/Divider M
30:26	/	/	/
25:24	R/W	0x0	MBUS_SCLK_SRC Clock Source Select

			00: OSC24M 01: PLL6 10: PLL5 11: Reserved
23:18	/	/	/
17:16	R/W	0x0	MBUS_SCLK_RATIO_N Clock Pre-divide Ratio (N) The select clock source is pre-divided by 2^N. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	MBUS_SCLK_RATIO_M Clock Divide Ratio (M) The divided clock is divided by (M+1). The divider is from 1 to 16.

3.4.4.57. MIPI_DSI CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x168			Register Name: MIPI_DSI_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DSI_SCLK_GATING. Gating DSI Special Clock 0: Clock is OFF 1: Clock is ON DSI Special clock(test clock) = Clock Source/DSI_SCLK_DIV_M.
30:26	/	/	/
25:24	R/W	0x0	DSI_SCLK_SRC_SEL. DSI Special Clock Source Select 00: PLL3(1X) 01: PLL7(1X) 10: PLL3(2X) 11: PLL7(2X)

23:20	/	/	/
19:16	R/W	0x0	DSI_SCLK_DIV_M. DSI Special Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.
15	R/W	0x0	DSI_DPHY_GATING. Gating DSI DPHY Clock 0: Clock is OFF 1: Clock is ON This DSI DPHY clock =Clock Source/ DPHY_CLK_DIV_M.
14:10	/	/	/
9:8	R/W	0x0	DSI_DPHY_SRC_SEL. DSI DPHY Clock Source Select. 00: PLL3(1X) 01: PLL7(1X) 10: PLL3(2X) 11: PLL7(2X)
7:4	/	/	/.
3:0	R/W	0x0	DPHY_CLK_DIV_M. DSI DPHY Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.58. MIPI_CSI0 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x16C			Register Name: MIPI_CSI0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	CSI_DPHY_CLK_GATING. Gating CSI_DPHY Clock

			0: Clock is OFF 1: Clock is ON This clock = CSI_DPHY Clock Source/ CSI_DPHY_DIV_M.
14:10	/	/	/
9:8	R/W	0x0	CSI_DPHY_SRC_SEL. CSI_DPHY Clock Source Select 00: PLL3(1X) 01: PLL7(1X) 10: PLL3(2X) 11: PLL7(2X)
7:4	/	/	/
3:0	R/W	0x0	CSI_DPHY_DIV_M. CSI_DPHY Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.59. IEP-DRC0 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x180			Register Name: DRC0_SCLK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL3(1X) 001: PLL7(1X)

			010: PLL6(2X) 011: PLL8 100:PLL9 101:PLL10 110/111:Reserved.
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.60. IEP-DRC1 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x184			Register Name: DRC1_SCLK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL3(1X) 001: PLL7(1X) 010: PLL6(2X) 011: PLL8 100:PLL9 101:PLL10 110/111:Reserved.

23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.61. IEP-DEU0 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x188			Register Name: DEU0_SCLK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL3(1X) 001: PLL7(1X) 010: PLL6(2X) 011: PLL8 100:PLL9 101:PLL10 110/111:Reserved.
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.62. IEP-DEU1 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x18C			Register Name: DEU1_SCLK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL3(1X) 001: PLL7(1X) 010: PLL6(2X) 011: PLL8 100:PLL9 101:PLL10 110/111:Reserved.
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.4.4.63. GPU CORE CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x1A0			Register Name: GPU_CORE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING.

			Gating the Special clock for GPU core(0: mask, 1: pass). This special clock = Clock Source/Divider N.
30:27	/	/	/.
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select. 000:PLL8 001:PLL6(2X)/3 010:PLL3 011:PLL7 100:PLL9 101:PLL10 110/111:Reserved.
23:3	/	/	/.
2:0	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (N) The select clock source is pre-divided by n+1. The divider is from 1 to 8.

3.4.4.64. GPU MEMORY CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x1A4			Register Name: GPU_MEM_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating the Special clock for GPU mem (0: mask, 1: pass). This special clock = Clock Source/Divider N.
30:27	/	/	/.
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select. 000:PLL8 001:PLL6(2X)/3

			010:PLL3 011:PLL7 100:PLL9 101:PLL10 110/111:Reserved.
23:3	/	/	/.
2:0	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (N) The select clock source is pre-divided by n+1. The divider is from 1 to 8.

3.4.4.65. GPU HYD CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x1A8			Register Name: GPU_HYD_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating the Special clock for GPU hyd (0: mask, 1: pass). This special clock = Clock Source/Divider N.
30:27	/	/	/.
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select. 000:PLL8 001:PLL6(2X)/3 010:PLL3 011:PLL7 100:PLL9 101:PLL10 110/111:Reserved.
23:3	/	/	/.
2:0	R/W	0x0	CLK_DIV_RATIO_N.

			Clock pre-divide ratio (N) The select clock source is pre-divided by n+1. The divider is from 1 to 8.

3.4.4.66. ATS CLOCK REGISTER (DEFAULT: 0X80000000)

Offset: 0x1B0			Register Name: ATS_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source /Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: / 11: /.
23:3	/	/	/
2:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 8.

3.4.4.67. TRACE CLOCK REGISTER (DEFAULT: 0X80000000)

Offset: 0x1B4			Register Name: TRACE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	SCLK_GATING.

			Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source /Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: / 11: /.
23:3	/	/	/
2:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 8.

3.4.4.68. PLL LOCK TIME REGISTER (DEFAULT:0X000000FF)

Offset: 0x200			Register Name: PLL_LOCK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFF	PLL_LOCK_TIME PLL Lock Time (Unit: us). Note: When any PLL (except PLL1) is enabled or changed, the corresponding PLL lock bit will be set after the PLL Lock Time.

3.4.4.69. PLL1 LOCK TIME REGISTER (DEFAULT:0X000000FF)

Offset: 0x204			Register Name: PLL1_LOCK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:16	/	/	/
15:0	R/W	0xFF	PLL1_LOCK_TIME PLL1 Lock Time (Unit: us). Note: When PLL1 is enabled or changed, the PLL1 lock bit will be set after the PLL1 Lock Time.

3.4.4.70. PLL1 BIAS REGISTER (DEFAULT:0X08100200)

Offset: 0x220			Register Name: PLL1_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	VCO_RST. VCO reset in.
30:29	/	/	/
28	R/W	0x0	EXG_MODE. Exchange mode. Note: CPU PLL source will select PLL6 instead of PLL1
27:24	R/W	0x8	PLL_VCO_BIAS_CTRL. PLL VCO bias control[3:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CUR_CTRL. PLL Bias Current Control[4:0].
15:11	/	/	/
10:8	R/W	0x2	PLL_LOCK_CTRL. PLL lock time control[2:0].
7:4	/	/	/
3:0	R/W	0x0	PLL_DAMP_FACT_CTRL. PLL damping factor control[3:0].

3.4.4.71. PLL2 BIAS REGISTER (DEFAULT:0X10100000)

Offset: 0x224	Register Name: PLL2_BIAS_REG

Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS. PLL VCO Bias Current[4:0]
23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CUR. PLL Bias Current[4:0]
15:0	/	/	/

3.4.4.72. PLL3 BIAS REGISTER (DEFAULT:0X10100000)

Offset: 0x228			Register Name: PLL3_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CTRL. PLL Bias Control[4:0].
15:3	/	/	/
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL damping factor control[2:0].

3.4.4.73. PLL4 BIAS REGISTER (DEFAULT:10100000)

Offset: 0x22C			Register Name: PLL4_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0].
23:21	/	/	/

20:16	R/W	0x10	PLL_BIAS_CTRL. PLL Bias Control[4:0].
15:3	/	/	/
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL damping factor control[2:0].

3.4.4.74. PLL5 BIAS REGISTER (DEFAULT:0X81104000)

Offset: 0x230			Register Name: PLL5_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x8	PLL_VCO_BIAS. PLL VCO bias[3:0]
27:26	/	/	/
25	R/W	0x0	PLL_VCO_GAIN_CTRL_EN. PLL VCO gain control enable. 0: disable, 1: enable.
24	R/W	0x1	PLL_BANDW_CTRL. PLL band width control. 0: narrow, 1: wide.
23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CUR_CTRL. PLL Bias Current Control.
15	/	/	/
14:12	R/W	0x4	PLL_VCO_GAIN_CTRL. PLL VCO gain control bit[2:0].
11:4	/	/	/
3:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL damping factor control[3:0].

3.4.4.75. PLL6 BIAS REGISTER (DEFAULT:0X10100010)

Offset: 0x234			Register Name: PLL6_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS. PLL VCO bias[4:0]
23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CUR_CTRL. PLL Bias Current Control.
15:5	/	/	/
4	R/W	0x1	PLL_BANDW_CTRL. PLL band width control. 0: narrow, 1: wide.
3:2	/	/	/
1:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL damping factor control[1:0].

3.4.4.76. PLL7 BIAS REGISTER (DEFAULT:10100000)

Offset: 0x238			Register Name: PLL7_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/.
28:24	R/W	0X10	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0].
23:21	/	/	/.
20:16	R/W	0x10	PLL_BIAS_CTRL. PLL Bias Control[4:0].
15:3	/	/	/.
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL damping factor control[2:0].

3.4.4.77. PLL8 BIAS REGISTER (DEFAULT:0X10100000)

Offset: 0x23C			Register Name: PLL8_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/.
28:24	R/W	0X10	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0].
23:21	/	/	/.
20:16	R/W	0x10	PLL_BIAS_CTRL. PLL Bias Control[4:0].
15:3	/	/	/.
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL damping factor control[2:0].

3.4.4.78. MIPI_PLL BIAS REGISTER (DEFAULT: 0XA8100400)

Offset: 0x240			Register Name: MIPI_PLL_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	VCO_RST. VCO reset in.
30:28	R/W	0x2	PLLVDD_LDO_OUT_CTRL. PLLVDD LDO output control. 000:1.10v 001:1.15v 010:1.20v 011:1.25v 100: 1.30v 101:1.35v 110:1.40v 111:1.45v

27:24	R/W	0x8	PLL_VCO_BIAS_CTRL. PLL VCO bias control [3:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CUR_CTRL. PLL Bias Current Control[4:0].
15:11	/	/	/
10:8	R/W	0x4	PLL_LOCK_CTRL. PLL lock time control[2:0].
7:1	/	/	/
0	R/W	0x0	PLL_DAMP_FACT_CTRL. PLL damping factor control.

3.4.4.79. PLL9 BIAS REGISTER (DEFAULT:10100000)

Offset: 0x244			Register Name: PLL9_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/.
28:24	R/W	0X10	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0].
23:21	/	/	/.
20:16	R/W	0x10	PLL_BIAS_CTRL. PLL Bias Control[4:0].
15:3	/	/	/.
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL damping factor control[2:0].

3.4.4.80. PLL10 BIAS REGISTER (DEFAULT:10100000)

Offset: 0x248			Register Name: PLL10_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/.

28:24	R/W	0X10	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0].
23:21	/	/	/.
20:16	R/W	0x10	PLL_BIAS_CTRL. PLL Bias Control[4:0].
15:3	/	/	/.
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL damping factor control[2:0].

3.4.4.81. PLL1-PATTERN CONTROL REGISTER (DEFAULT: 0X00000000)

Offset: 0x280			Register Name: PLL1_PAT_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-delta pattern enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: awmode
28:20	R/W	0x0	WAVE_STEP. Wave step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz

16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.4.4.82. PLL2- PATTERN CONTROL REGISTER(DEFAULT:0X00000000)

Offset: 0x284			Register Name: PLL2_PAT_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-delta pattern enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: awmode
28:20	R/W	0x0	WAVE_STEP. Wave step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.4.4.83. PLL3- PATTERN CONTROL REGISTER (DEFAULT:0X00000000)

Offset: 0x288			Register Name: PLL3_PAT_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-delta pattern enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: awmode
28:20	R/W	0x0	WAVE_STEP. Wave step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.4.4.84. PLL4- PATTERN CONTROL REGISTER (DEFAULT:0X00000000)

Offset: 0x28C			Register Name: PLL4_PAT_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-delta pattern enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1

			10: Triangular 11: awmode
28:20	R/W	0x0	WAVE_STEP. Wave step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.4.4.85. PLL5- PATTERN CONTROL REGISTER (DEFAULT:0X00000000)

Offset: 0x290			Register Name: PLL5_PAT_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-delta pattern enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: awmode
28:20	R/W	0x0	WAVE_STEP. Wave step.
19	/	/	/
18:17	R/W	0x0	FREQ.

			Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.4.4.86. PLL7- PATTERN CONTROL REGISTER(DEFAULT:0X00000000)

Offset: 0x298			Register Name: PLL7_PAT_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-delta pattern enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: awmode
28:20	R/W	0x0	WAVE_STEP. Wave step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT.

			Wave Bottom.

3.4.4.87. PLL8- PATTERN CONTROL REGISTER (DEFAULT:0X00000000)

Offset: 0x29C			Register Name: PLL8_PAT_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-delta pattern enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: awmode
28:20	R/W	0x0	WAVE_STEP. Wave step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.4.4.88. MIPI_PLL- PATTERN CONTROL REGISTER (DEFAULT:0X00000000)

Offset: 0x2A0			Register Name: MIPI_PLL_PAT_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN.

			Sigma-delta pattern enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: awmode
28:20	R/W	0x0	WAVE_STEP. Wave step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.4.4.89. PLL9- PATTERN CONTROL REGISTER (DEFAULT:0X00000000)

Offset: 0x2A4			Register Name: PLL9_PAT_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-delta pattern enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular

			11: awmode
28:20	R/W	0x0	WAVE_STEP. Wave step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.4.4.90. PLL10- PATTERN CONTROL REGISTER (DEFAULT:0X00000000)

Offset: 0x2A8			Register Name: PLL10_PAT_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-delta pattern enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: awmode
28:20	R/W	0x0	WAVE_STEP. Wave step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency.

			00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.4.4.91. AHB1 MODULE SOFTWARE RESET REGISTER 0(DEFAULT: 0X00000000)

Offset: 0x2C0			Register Name: AHB1_RST_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	USBOHCI2_RST. USB OHCI2 Reset Control 0: Assert 1: De-assert
30	R/W	0x0	USBOHCI1_RST. USB OHCI1 Reset Control 0: Assert 1: De-assert
29	R/W	0x0	USBOHCI0_RST. USB OHCI0 Reset Control 0: Assert 1: De-assert
28	/	/	/
27	R/W	0x0	USBEHCI1_RST. USB EHCI1 Reset Control 0: Assert 1: De-assert
26	R/W	0x0	USBEHCI0_RST. USB EHCI0 Reset Control

			0: Assert 1: De-assert
25	/	/	/
24	R/W	0x0	USBDRD_RST. USB DRD Reset Control 0: Assert 1: De-assert
23	R/W	0x0	SPI3_RST. SPI3 reset. 0: assert, 1: de-assert.
22	R/W	0x0	SPI2_RST. SPI2 reset. 0: assert, 1: de-assert.
21	R/W	0x0	SPI1_RST. SPI1 reset. 0: assert, 1: de-assert.
20	R/W	0x0	SPI0_RST. SPI0 reset. 0: assert, 1: de-assert.
19	R/W	0x0	HSTMR_RST. HSTMR reset. 0: assert, 1: de-assert.
18	R/W	0x0	TS_RST. TS reset. 0: assert, 1: de-assert.
17	R/W	0x0	EMAC_RST. EMAC reset. 0: assert, 1: de-assert.
16:15	/	/	/

14	R/W	0x0	SDRAM_RST. SDRAM AHB reset. 0: assert, 1: de-assert.
13	R/W	0x0	NAND0_RST. NAND0 reset. 0: assert, 1: de-assert.
12	R/W	0x0	NAND1_RST. NAND1 reset. 0: assert, 1: de-assert.
11	R/W	0x0	SD3_RST. SD/MMC3 reset. 0: assert, 1: de-assert.
10	R/W	0x0	SD2_RST. SD/MMC2 reset. 0: assert, 1: de-assert.
9	R/W	0x0	SD1_RST. SD/MMC1 reset. 0: assert, 1: de-assert.
8	R/W	0x0	SD0_RST. SD/MMC0 reset. 0: assert, 1: de-assert.
7	/	/	/
6	R/W	0x0	DMA_RST. DMA reset. 0: assert, 1: de-assert.
5	R/W	0x0	SS_RST. SS reset. 0: assert, 1: de-assert.
4:2	/	/	/

1	R/W	0x0	MIPIDSI_RST. MIPI DSI reset. 0: assert, 1: de-assert.
0	/	/	/

3.4.4.92. AHB1 MODULE SOFTWARE RESET REGISTER 1(DEFAULT: 0X00000000)

Offset: 0x2C4			Register Name: AHB1_RST_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26	R/W	0x0	DRC1_RST. DRC1 reset. 0: assert, 1: de-assert.
25	R/W	0x0	DRC0_RST. DRC0 reset. 0: assert, 1: de-assert.
24	R/W	0x0	DEU1_RST. DEU1 reset. 0: assert, 1: de-assert.
23	R/W	0x0	DEU0_RST DEU0 reset. 0: assert, 1: de-assert.
22	R/W	0x0	/
21	R/W	0x0	/
20	R/W	0x0	GPU_RST. GPU reset. 0: assert, 1: de-assert.
19	/	/	/
18	R/W	0x0	MP_RST. MP reset.

			0: assert, 1: de-assert.
17:16	/	/	/
15	R/W	0x0	FE1_RST. DE-FE1 reset. 0: assert, 1: de-assert.
14	R/W	0x0	FE0_RST. DE-FE0 reset. 0: assert, 1: de-assert.
13	R/W	0x0	BE1_RST. DE-BE1 reset. 0: assert, 1: de-assert.
12	R/W	0x0	BE0_RST. DE-VE0 reset. 0: assert, 1: de-assert.
11	R/W	0x0	HDMI_RST. HDMI reset. 0: assert, 1: de-assert.
10:9	/	/	/
8	R/W	0x0	CSI_RST. CSI reset. 0: assert, 1: de-assert.
7:6	/	/	
5	R/W	0x0	LCD1_RST. LCD1 reset. 0: assert, 1: de-assert.
4	R/W	0x0	LCD0_RST. LCD0 reset. 0: assert, 1: de-assert.
3:1	/	/	/

0	R/W	0x0	VE_RST. VE reset. 0: assert, 1: de-assert.

3.4.4.93. AHB1 MODULE SOFTWARE RESET REGISTER2(DEFAULT:0X00000000)

Offset: 0x2C8			Register Name: AHB1_RST_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	LVDS_RST. LVDS reset. 0: assert, 1: de-assert.

3.4.4.94. APB1 MODULE SOFTWARE RESET REGISTER(DEFAULT: 0X00000000)

Offset: 0x2D0			Register Name: APB1_RST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/.
13	R/W	0x0	DAUDIO1_RST. DAUDIO1 reset. 0: assert, 1: de-assert.
12	R/W	0x0	DAUDIO0_RST. DAUDIO0 reset. 0: assert, 1: de-assert.
11:5	/	/	/
4	R/W	0x0	DIGITAL_MIC_RST. Digital MIC reset. 0: assert, 1: de-assert.
3:2	/	/	/
1	R/W	0x0	/
0	R/W	0x0	AUDIO_CODEC_RST.

			Audio codec reset. 0: assert, 1: de-assert.

3.4.4.95. APB2 MODULE SOFTWARE RESET REGISTER(DEFAULT: 0X00000000)

Offset: 0x2D8			Register Name: APB2_RST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/.
21	R/W	0x0	UART5_RST. UART5 reset. 0: assert, 1: de-assert.
20	R/W	0x0	UART4_RST. UART4 reset. 0: assert, 1: de-assert.
19	R/W	0x0	UART3_RST. UART3 reset. 0: assert, 1: de-assert.
18	R/W	0x0	UART2_RST. UART2 reset. 0: assert, 1: de-assert.
17	R/W	0x0	UART1_RST. UART1 reset. 0: assert, 1: de-assert.
16	R/W	0x0	UART0_RST. UART0 reset. 0: assert, 1: de-assert.
15:4	/	/	/
3	R/W	0x0	TWI3_RST. TWI3 reset. 0: assert, 1: de-assert.

2	R/W	0x0	TWI2_RST. TWI2 reset. 0: assert, 1: de-assert.
1	R/W	0x0	TWI1_RST. TWI1 reset. 0: assert, 1: de-assert.
0	R/W	0x0	TWI0_RST. TWI0 reset. 0: assert, 1: de-assert.

3.4.4.96. CLK_OUTA_REG (DEFAULT: 0X00000000)

Offset: 0x300			Register Name: CLK_OUTA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CLK_OUT_EN Clock Output Enable 0: disable 1: Clock Output Enable OutputA = Clock Source / DIVIDOR-N / DIVIDOR-M.
30:28	/	/	/
27:24	R/W	0x0	CLK_OUT_SRC_SEL 0000: OSC24MHz/750=32KHz 0001: LOSC 0010: OSC24MHz 0011: / 0100: / 0101: / 0110: / 0111: / 1000: /

			1001: / 1010: / 1011: AXICLK/4 1100: / 1101: AHB1CLK/4 1110: / 1111: /
23:22	/	/	/
21:20	R/W	0x0	DIVIDOR_N Clock Output Divide Factor N 00: /1 01: /2 10: /4 11: /8
19:13	/	/	/
12:8	R/W	0x0	DIVIDOR_M Clock Output Divide Factor M 00000: /1 00001: /2 00010: /3 …… 11111: /32
7:0	/	/	/

3.4.4.97. CLK_OUTB_REG (DEFAULT: 0X00000000)

Offset: 0x304			Register Name: CLK_OUTB_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CLK_OUT_EN Clock Output Enable

			0: disable 1: Clock Output Enable OutputB = Clock Source / DIVIDOR-N / DIVIDOR-M.
30:28	/	/	/
27:24	R/W	0x0	CLK_OUT_SRC_SEL 0000: OSC24MHz/750=32KHz 0001: LOSC 0010: OSC24MHz 0011: / 0100: / 0101: / 0110: / 0111: / 1000: / 1001: / 1010: / 1011: AXICLK/4 1100: / 1101: AHB1CLK/4 1110: / 1111: /
23:22	/	/	/
21:20	R/W	0x0	DIVIDOR_N Clock Output Divide Factor N 00: /1 01: /2 10: /4 11: /8
19:13	/	/	/

12:8	R/W	0x0	DIVIDOR_M Clock Output Divide Factor M 00000: /1 00001: /2 00010: /3 …… 11111: /32
7:0	/	/	/

3.4.4.98. CLK_OUTC_REG (DEFAULT: 0X00000000)

Offset: 0x308			Register Name: CLK_OUTC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CLK_OUT_EN Clock Output Enable 0: disable 1: Clock Output Enable Output C= Clock Source / DIVIDOR-N / DIVIDOR-M.
30:28	/	/	/
27:24	R/W	0x0	CLK_OUT_SRC_SEL 0000: OSC24MHz/750=32KHz 0001: LOSC 0010: OSC24MHz 0011: / 0100: / 0101: / 0110: / 0111: / 1000: / 1001: /

			1010: / 1011: AXICLK/4 1100:/ 1101: AHB1CLK/4 1110: / 1111: /
23:22	/	/	/
21:20	R/W	0x0	DIVIDOR_N Clock Output Divide Factor N 00: /1 01: /2 10: /4 11: /8
19:13	/	/	/
12:8	R/W	0x0	DIVIDOR_M Clock Output Divide Factor M 00000: /1 00001: /2 00010: /3 …… 11111: /32
7:0	/	/	/

3.5. CPU

3.5.1. OVERVIEW

The CPU configuration module features:

- Support software reset control for each CPU.
- Support CPU configuration for each CPU
- Integrate five 64-bit idle counters and a 64-bit common counter

3.5.2. CPU CONFIGURATION REGISTER LIST

Module Name	Base Address
CPUCFG	0x01F01C00

Register Name	Offset	Description
CPU0_RST_CTRL	0x0040	CPU0 Reset Control
CPU0_CTRL_REG	0x0044	CPU0 Control Register
CPU0_STATUS_REG	0x0048	CPU0 Status Register
CPU1_RST_CTRL	0x0080	CPU1 Reset Control
CPU1_CTRL_REG	0x0084	CPU1 Control Register
CPU1_STATUS_REG	0x0088	CPU1 Status Register
CPU2_RST_CTRL	0x00C0	CPU2 Reset Control
CPU2_CTRL_REG	0x00C4	CPU2 Control Register
CPU2_STATUS_REG	0x00C8	CPU2 Status Register
CPU3_RST_CTRL	0x0100	CPU3 Reset Control
CPU3_CTRL_REG	0x0104	CPU3 Control Register
CPU3_STATUS_REG	0x0108	CPU3 Status Register

GENER_CTRL_REG	0x0184	General Control Register
L2_STATUS_REG	0x0188	L2 Status Register
EVENT_IN	0x0190	Event Input Register
SUP_STAN_FLAG_REG	0x01A0	Super Standby Flag Register
PRIVATE_REG0	0x01A4	Private Register0
PRIVATE_REG1	0x01A8	Private Register1
IDLE_CNT0_LOW_REG	0x0200	Idle Counter 0 Low Register
IDLE_CNT0_HIGH_REG	0x0204	Idle Counter 0 High Register
IDLE_CNT0_CTRL_REG	0x0208	Idle Counter 0 Control Register
IDLE_CNT1_LOW_REG	0x0210	Idle Counter 1 Low Register
IDLE_CNT1_HIGH_REG	0x0214	Idle Counter 1 High Register
IDLE_CNT1_CTRL_REG	0x0218	Idle Counter 1 Control Register
IDLE_CNT2_LOW_REG	0x0220	Idle Counter 2 Low Register
IDLE_CNT2_HIGH_REG	0x0224	Idle Counter 2 High Register
IDLE_CNT2_CTRL_REG	0x0228	Idle Counter 2 Control Register
IDLE_CNT3_LOW_REG	0x0230	Idle Counter 3 Low Register
IDLE_CNT3_HIGH_REG	0x0234	Idle Counter 3 High Register
IDLE_CNT3_CTRL_REG	0x0238	Idle Counter 3 Control Register
IDLE_CNT4_LOW_REG	0x0240	Idle Counter 4 Low Register
IDLE_CNT4_HIGH_REG	0x0244	Idle Counter4 High Register
IDLE_CNT4_CTRL_REG	0x0248	Idle Counter 4 Control Register
CNT64_CTRL_REG	0x0280	64-Bit Counter Control Register
CNT64_LOW_REG	0x0284	64-Bit Counter Low Register
CNT64_HIGH_REG	0x0288	64-Bit Counter High Register

3.5.3. CPU CONFIGURATION REGISTER DESCRIPTION

3.5.3.1. CPU0 RESET CONTROL(DEFAULT: 0X00000003)

Offset: 0x40			Register Name: CPU0_RST_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/.
1	R/W	0x1	CPU0_CORE_REST. These are the primary reset signals which initialize the processor logic in the processor power domains, not including the debug, breakpoint and watchpoint logic. 0: assert 1: de-assert.
0	R/W	0x1	CPU0_RESET. CPU0 Reset Assert. These power-on reset signals initialize all the processor logic, including CPU Debug, and breakpoint and watch point logic in the processor power domains. They do not reset debug logic in the debug power domain. 0: assert 1: de-assert.

3.5.3.2. CPU0 CONTROL REGISTER(DEFAULT :0X00000000)

Offset: 0x44			Register Name: CPU0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	CPU0_CP15_WRITE_DISABLE. Disable write access to certain CP15 registers. 0: enable 1: disable

3.5.3.3. CPU0 STATUS REGISTER(DEFAULT : 0X00000000)

Offset: 0x48			Register Name: CPU0_ STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/.
2	R	0x0	STANDBYWFI. Indicates if the processor is in WFI standby mode: 0: Processor not in WFI standby mode. 1: Processor in WFI standby mode
1	R	0x0	STANDBYWFE. Indicates if the processor is in the WFE standby mode: 0: Processor not in WFE standby mode 1: Processor in WFE standby mode
0	R	0x0	SMP_AMP 0: AMP mode 1: SMP mode

3.5.3.4. CPU1 RESET CONTROL(DEFAULT: 0X00000000)

Offset: 0x80			Register Name: CPU1_RST_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/.
1	R/W	0x0	CPU1_CORE_REST. These are the primary reset signals which initialize the processor logic in the processor power domains, not including the debug, breakpoint and watchpoint logic. 0: assert 1: de-assert.
0	R/W	0x0	CPU1_RESET. CPU1 Reset Assert.

			These power-on reset signals initialize all the processor logic, including CPU Debug, and breakpoint and watch point logic in the processor power domains. They do not reset debug logic in the debug power domain. 0: assert 1: de-assert.

3.5.3.5. CPU1 CONTROL REGISTER(DEFAULT :0X00000000)

Offset: 0x84			Register Name: CPU1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	CPU1_CP15_WRITE_DISABLE. Disable write access to certain CP15 registers. 0: enable 1: disable

3.5.3.6. CPU1 STATUS REGISTER(DEFAULT : 0X00000000)

Offset: 0x88			Register Name: CPU1_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/.
2	R	0x0	STANDBYWFI. Indicates if the processor is in WFI standby mode: 0: Processor not in WFI standby mode. 1: Processor in WFI standby mode
1	R	0x0	STANDBYWFE. Indicates if the processor is in the WFE standby mode: 0: Processor not in WFE standby mode 1: Processor in WFE standby mode
0	R	0x0	SMP_AMP

			0: AMP mode 1: SMP mode

3.5.3.7. CPU2 RESET CONTROL(DEFAULT: 0X00000000)

Offset: 0xC0			Register Name: CPU2_RST_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/.
1	R/W	0x0	CPU2_CORE_REST. These are the primary reset signals which initialize the processor logic in the processor power domains, not including the debug, breakpoint and watchpoint logic. 0: assert 1: de-assert.
0	R/W	0x0	CPU2_RESET. CPU2 Reset Assert. These power-on reset signals initialize all the processor logic, including CPU Debug, and breakpoint and watch point logic in the processor power domains. They do not reset debug logic in the debug power domain. 0: assert 1: de-assert.

3.5.3.8. CPU2 CONTROL REGISTER(DEFAULT :0X00000000)

Offset: 0xC4			Register Name: CPU2_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	CPU2_CP15_WRITE_DISABLE. Disable write access to certain CP15 registers. 0: enable

			1: disable

3.5.3.9. CPU2 STATUS REGISTER(DEFAULT : 0X00000000)

Offset: 0xC8			Register Name: CPU2_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/.
2	R	0x0	STANDBYWFI. Indicates if the processor is in WFI standby mode: 0: Processor not in WFI standby mode. 1: Processor in WFI standby mode
1	R	0x0	STANDBYWFE. Indicates if the processor is in the WFE standby mode: 0: Processor not in WFE standby mode 1: Processor in WFE standby mode
0	R	0x0	SMP_AMP 0: AMP mode 1: SMP mode

3.5.3.10. CPU3 RESET CONTROL(DEFAULT: 0X00000000)

Offset: 0x100			Register Name: CPU3_RST_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/.
1	R/W	0x0	CPU3_CORE_REST. These are the primary reset signals which initialize the processor logic in the processor power domains, not including the debug, breakpoint and watchpoint logic. 0: assert 1: de-assert.
0	R/W	0x0	CPU3_RESET.

			CPU3 Reset Assert. These power-on reset signals initialize all the processor logic, including CPU Debug, and breakpoint and watch point logic in the processor power domains. They do not reset debug logic in the debug power domain. 0: assert 1: de-assert.

3.5.3.11. CPU3 CONTROL REGISTER(DEFAULT :0X00000000)

Offset: 0x104			Register Name: CPU3_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	CPU3_CP15_WRITE_DISABLE. Disable write access to certain CP15 registers. 0: enable 1: disable

3.5.3.12. CPU3 STATUS REGISTER(DEFAULT : 0X00000000)

Offset: 0x108			Register Name: CPU3_ STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/.
2	R	0x0	STANDBYWFI. Indicates if the processor is in WFI standby mode: 0: Processor not in WFI standby mode. 1: Processor in WFI standby mode
1	R	0x0	STANDBYWFE. Indicates if the processor is in the WFE standby mode: 0: Processor not in WFE standby mode 1: Processor in WFE standby mode

0	R	0x0	SMP_AMP 0: AMP mode 1: SMP mode

3.5.3.13. GENERAL CONTROL REGISTER(DEFAULT :0X00000020)

Offset: 0x184			Register Name: GENER_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/.
8	R/W	0x0	CFGSDISABLE. Disables write access to some secure GIC registers.
7	R/W	0x0	TSCLKCHANGE When trace clk changes, this bit should set 1 to valid the trace clk
6	R/W	0x0	ACINACTM. Snoop interface is inactive and no longer accepting requests.
5	R/W	0x1	L2_RST. L2 Reset.(SCU global reset) 0: Apply reset to shared L2 memory system controller. 1: Do not apply reset to shared L2 memory system controller.
4	R/W	0x0	L2_RST_DISABLE. Disable automatic L2 cache invalidate at reset: 0: L2 cache is reset by hardware. 1: L2 cache is not reset by haredware.
3:0	R/W	0x0	L1_RST_DISABLE. L1 Reset Disable[3:0]. 0: L1 cache is reset by hardware. 1: L1 cache is not reset by hardware.

3.5.3.14. L2 STATUS REGISTER(DEFAULT :0X00000000)

Offset: 0x188			Register Name: L2_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/.
0	R	0x0	STANDBYWFIL2. Indicates if the L2 memory system is in WFI standby mode. 0:active 1:idle

3.5.3.15. EVENT INPUT REGISTER(DEFAULT : 0X00000000)

Offset: 0x190			Register Name: EVENT_IN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	EVENT_IN. Event input that can wake-up CPU0/1/2/3 from WFE standby mode.

3.5.3.16. SUPER STANDBY FLAG REGISTER (DEFAULT: 0X00000000)

Offset: 0x1A0			Register Name: SUP_STAN_FLAG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	SUP_STANDBY_FLAG.
15:0	R/W	0x0	SUP_STANBY_FLAG_DATA.

Notes:

When system is turned on, Super Standby Flag Register low 16 bits should be 0x0. If you want to write correct super standby flag ID in low 16 bits, the high 16 bits should be written 0x16AA at first, and then write 0xAA16XXXX in the Super Standby Flag Register ('XXXX' stands for the correct super standby flag ID). Refer to the Diagram section for details.

3.5.3.17. PRIVATE REGISTER0 (DEFAULT: 0X00000000)

Offset: 0x1A4			Register Name: PRIVATE_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	/

3.5.3.18. PRIVATE REGISTER1 (DEFAULT: 0X00000000)

Offset: 0x1A8			Register Name: PRIVATE_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	/

3.5.3.19. IDLE COUNTER 0 LOW REGISTER (DEFAULT: 0X00000000)

Offset: 0x200			Register Name: IDLE_CNT0_LOW_REG.
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	IDLE_CNT0_LO. Idle Counter 0 [31:0]. This counter clock source is 24MHz. If the CPU is in idle state, the counter will count up in the clock of 24MHz. Any write to this register will clear this register and the idle counter 0 high register.

3.5.3.20. IDLE COUNTER 0 HIGH REGISTER (DEFAULT: 0X00000000)

Offset: 0x204			Register Name: IDLE_CNT0_HIGH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	IDLE_CNT0_HI. Idle Counter 0 [63:32]. Any write to this register will clear this register and the idle counter 0 low register.

3.5.3.21. IDLE COUNTER 0 CONTROL REGISTER (DEFAULT: 0X00000000)

Offset: 0x208	Register Name: IDLE_CNT0_CTRL_REG

Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	IDLE_CNT_EN. Idle counter enable. 0: disable 1: enable. Note: Idle Counter 0 is used for CPU0
1	R/W	0x0	IDLE_RL_EN. Idle Counter Read Latch Enable. 0: no effect, 1: to latch the idle Counter to the Low/Hi registers and it will change to zero after the registers are latched.
0	R/W	0x0	IDLE_CNT_CLR_EN. Idle Counter Clear Enable. 0: no effect, 1: to clear the idle Counter Low/Hi registers and it will change to zero after the registers are cleared.

3.5.3.22. IDLE COUNTER 1 LOW REGISTER (DEFAULT: 0X00000000)

Offset: 0x210			Register Name: IDLE_CNT1_LOW_REG.
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	IDLE_CNT1_LO. Idle Counter 1 [31:0]. This counter clock source is 24MHz. If the CPU is in idle state, the counter will count up in the clock of 24MHz. Any write to this register will clear this register and the idle counter 1 high register.

3.5.3.23. IDLE COUNTER 1 HIGH REGISTER (DEFAULT: 0X00000000)

Offset: 0x214			Register Name: IDLE_CNT1_HIGH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:0	R/W	0x0	IDLE_CNT1_HI. Idle Counter 1[63:32]. Any write to this register will clear this register and the idle counter 1 low register.

3.5.3.24. IDLE COUNTER 1 CONTROL REGISTER (DEFAULT: 0X00000000)

Offset: 0x218			Register Name: IDLE_CNT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	IDLE_CNT_EN. Idle counter enable. 0: disable 1: enable. Note: Idle Counter 1 is used for CPU1
1	R/W	0x0	IDLE_RL_EN. Idle Counter Read Latch Enable. 0: no effect, 1: to latch the idle Counter to the Low/Hi registers and it will change to zero after the registers are latched.
0	R/W	0x0	IDLE_CNT_CLR_EN. Idle Counter Clear Enable. 0: no effect, 1: to clear the idle Counter Low/Hi registers and it will change to zero after the registers are cleared.

3.5.3.25. IDLE COUNTER 2 LOW REGISTER (DEFAULT: 0X00000000)

Offset: 0x220			Register Name: IDLE_CNT2_LOW_REG.
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	IDLE_CNT2_LO. Idle Counter 2 [31:0]. This counter clock source is 24MHz. If the CPU is in idle state,

			the counter will count up in the clock of 24MHz. Any write to this register will clear this register and the idle counter 2 high register.

3.5.3.26. IDLE COUNTER 2 HIGH REGISTER (DEFAULT: 0X00000000)

Offset: 0x224			Register Name: IDLE_CNT2_HIGH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	IDLE_CNT2_HI. Idle Counter 2 [63:32]. Any write to this register will clear this register and the idle counter 2 low register.

3.5.3.27. IDLE COUNTER 2 CONTROL REGISTER (DEFAULT: 0X00000000)

Offset: 0x228			Register Name: IDLE_CNT2_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	IDLE_CNT_EN. Idle counter enable. 0: disable 1: enable. Note: Idle Counter 2 is used for CPU2
1	R/W	0x0	IDLE_RL_EN. Idle Counter Read Latch Enable. 0: no effect, 1: to latch the idle Counter to the Low/Hi registers and it will change to zero after the registers are latched.
0	R/W	0x0	IDLE_CNT_CLR_EN. Idle Counter Clear Enable. 0: no effect, 1: to clear the idle Counter Low/Hi registers and it will change to zero after the registers are cleared.

3.5.3.28. IDLE COUNTER 3 LOW REGISTER (DEFAULT: 0X00000000)

Offset: 0x230			Register Name: IDLE_CNT3_LOW_REG.
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	IDLE_CNT3_LO. Idle Counter 3 [31:0]. This counter clock source is 24MHz. If the CPU is in idle state, the counter will count up in the clock of 24MHz. Any write to this register will clear this register and the idle counter 3 high register.

3.5.3.29. IDLE COUNTER 3 HIGH REGISTER (DEFAULT: 0X00000000)

Offset: 0x234			Register Name: IDLE_CNT3_HIGH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	IDLE_CNT3_HI. Idle Counter 3 [63:32]. Any write to this register will clear this register and the idle counter 3 low register.

3.5.3.30. IDLE COUNTER 3 CONTROL REGISTER (DEFAULT: 0X00000000)

Offset: 0x238			Register Name: IDLE_CNT3_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	IDLE_CNT_EN. Idle counter enable. 0: disable 1: enable. Note: Idle Counter 3 is used for CPU3
1	R/W	0x0	IDLE_RL_EN.

			Idle Counter Read Latch Enable. 0: no effect, 1: to latch the idle Counter to the Low/Hi registers and it will change to zero after the registers are latched.
0	R/W	0x0	IDLE_CNT_CLR_EN. Idle Counter Clear Enable. 0: no effect, 1: to clear the idle Counter Low/Hi registers and it will change to zero after the registers are cleared.

3.5.3.31. IDLE COUNTER 4 LOW REGISTER (DEFAULT: 0X00000000)

Offset: 0x240			Register Name: IDLE_CNT4_LOW_REG.
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	IDLE_CNT4_LO. Idle Counter 4 [31:0]. This counter clock source is 24MHz. If the L2 cache is in idle state, the counter will count up in the clock of 24MHz. Any write to this register will clear this register and the idle counter 4 high register.

3.5.3.32. IDLE COUNTER 4 HIGH REGISTER (DEFAULT: 0X00000000)

Offset: 0x244			Register Name: IDLE_CNT4_HIGH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	IDLE_CNT4_HI. Idle Counter 4 [63:32]. Any write to this register will clear this register and the idle counter 4 low register.

3.5.3.33. IDLE COUNTER 4 CONTROL REGISTER (DEFAULT: 0X00000000)

Offset: 0x248			Register Name: IDLE_CNT4_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:3	/	/	/
2	R/W	0x0	IDLE_CNT_EN. Idle counter enable. 0: disable 1: enable. Note: Idle Counter 4 is used for L2 Cache.
1	R/W	0x0	IDLE_RL_EN. Idle Counter Read Latch Enable. 0: no effect, 1: to latch the idle Counter to the Low/Hi registers and it will change to zero after the registers are latched.
0	R/W	0x0	IDLE_CNT_CLR_EN. Idle Counter Clear Enable. 0: no effect, 1: to clear the idle Counter Low/Hi registers and it will change to zero after the registers are cleared.

3.5.3.34. 64-BIT COUNTER CONTROL REGISTER (DEFAULT: 0X00000000)

Offset: 0x280			Register Name: CNT64_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/.
2	R/W	0x0	CNT64_CLK_SRC_SEL. 64-bit Counter Clock Source Select. 0: OSC24M 1: /
1	R/W	0x0	CNT64_RL_EN. 64-bit Counter Read Latch Enable. 0: no effect, 1: to latch the 64-bit Counter to the Low/Hi registers and it will change to zero after the registers are latched.
0	R/W	0x0	CNT64_CLR_EN.

			64-bit Counter Clear Enable. 0: no effect, 1: to clear the 64-bit Counter Low/Hi registers and it will change to zero after the registers are cleared.

Notes:

This 64-bit counter will start to count as soon as the System Power On finishes.

3.5.3.35. 64-BIT COUNTER LOW REGISTER (DEFAULT: 0X00000000)

Offset: 0x284			Register Name: CNT64_LOW_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CNT64_LO. 64-bit Counter [31:0].

3.5.3.36. 64-BIT COUNTER HIGH REGISTER (DEFAULT: 0X00000000)

Offset: 0x288			Register Name: CNT64_HIGH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CNT64_HI. 64-bit Counter [63:32].

3.6. TRUSTZONE

3.6.1. TRUSTZONE ADDRESS SPACE CONTROLLER

The TZASC is an advanced microcontroller bus architecture compliant System-on-Chip peripheral. As a high-performance, area-optimized address space controller with on-chip AMBA bus interfaces that conform to the AMBA Advanced eXtensible Interface protocol and the AMBA Advanced Peripheral Bus protocol, it can be configured to provide optimum security address region control functions required for intended application.

MASTER	ID	MASTER	ID
CPU(AXI)	0	M00(DMAC)	16
GPU	1	M01(VE)	17
/	2	M02(MP)	18
/	3	M03(NAND0)	19
/	4	M04(IEP0)	20
H01(ATH)	5	M05(IEP1)	21
H02(EMAC)	6	M06(DEU0)	22
H03(SD0)	7	M07(DEU1)	23
H04(SD1)	8	R00(BE0)	24
H05(SD2)	9	R01(FE0)	25
H06(SD3)	10	R02(BE1)	26
H07(USB)	11	R03(FE1)	27
/	12	R04(CSI0)	28
/	13	R05(CSI1)	29
/	14	R06(TS)	30
M08(NAND1)	15	/	31

Table 3-1 Master and Master ID

SPN Field	Secure Read	Secure Write	Non-Secure Read	Non-Secure Write
4b0000	No	No	No	No
4b0100	No	Yes	No	No
4b0001,4b0101	No	Yes	No	Yes
4b1000	Yes	No	No	No
4b0010,4b1010	Yes	No	Yes	No
4b1100	Yes	Yes	No	No
4b1001,4b1101	Yes	Yes	No	Yes
4b0110,4b1110	Yes	Yes	Yes	No
4b0011,4b0111,4b1011,4b1111	Yes	Yes	Yes	Yes

Table 3-2 Region Security Permissions (when security inversion is disabled)

Notes: *SPN field* controls whether access to following AXI transactions is permitted by TZASC. See Region attributes n Register for more information.

SPN Field	Secure Read	Secure Write	Non-Secure Read	Non-Secure Write
4b0000	No	No	No	No
4b0001	No	No	No	Yes
4b0010	No	No	Yes	No
4b0011	No	No	Yes	Yes
4b0100	No	Yes	No	No
4b0101	No	Yes	No	Yes
4b0110	No	Yes	Yes	No
4b0111	No	Yes	Yes	Yes
4b1000	Yes	No	No	No
4b1001	Yes	No	No	Yes
4b1010	Yes	No	Yes	No
4b1011	Yes	No	Yes	Yes

4b1100	Yes	Yes	No	No
4b1101	Yes	Yes	No	Yes
4b1110	Yes	Yes	Yes	No
4b1111	Yes	Yes	Yes	Yes

Table 3-3 Region Security Permissions (when security inversion is enabled)

Size<n>	Size of region<n>	Base address constraints
b000000-b001101	Reserved	-
b001110	32KB	-
b001111	64KB	Bit [15] must be zero
b010000	128KB	Bits [16:15] must be zero
b010001	256KB	Bits [17:15] must be zero
b010010	512KB	Bits [18:15] must be zero
b010011	1MB	Bits [19:15] must be zero
b010100	2MB	Bits [20:15] must be zero
b010101	4MB	Bits [21:15] must be zero
b010110	8MB	Bits [22:15] must be zero
b010111	16MB	Bits [23:15] must be zero
b011000	32MB	Bits [24:15] must be zero
b011001	64MB	Bits [25:15] must be zero
b011010	128MB	Bits [26:15] must be zero
b011011	256MB	Bits [27:15] must be zero
b011100	512MB	Bits [28:15] must be zero
b011101	1GB	Bits [29:15] must be zero
b011110	2GB	Bits [30:15] must be zero

Table 3-4 Region Size

The TZASC features:

- Enable you to program security access permissions each address region;

- Permit data transfer between master and slave only if the security status of the AXI transaction matches the security settings of the memory region it addresses;

3.6.2. SPECULATIVE ACCESS

By default, TZASC performs read or write speculative, that means it forwards an AXI transaction address to a slave before it verifies that the AXI transaction is permitted to read address or write address respectively.

Since TZASC only permits data transfer between its AXI bus interfaces after verifying that the read or write access is permitted respectively, so when the verification fails, TZASC prevents data transfer between the master and slave as Denied AXI transactions.

When the speculative accesses are disabled, TZASC verifies the permissions of the access before it forwards the access to the salve. If the TZASC:

- permits the access, it commences an AXI transaction to the slave, and it adds one clock latency.
- denies the access, it prevents the transfer of data between the master and slave. In this situation, the slave is unaware when the TZASC prevents the master from accessing the slave.

3.6.3. TZASC REGISTER LIST

Module Name	Base Address
TZASC	0x01C1E000

Register Name	Offset	Description
TZASC_CONFIG_REG	0x0000	Configuration Register
TZASC_ACTION_REG	0x0004	Action Register
TZASC_LOCKDOWN_RANGE_REG	0x0008	Lock Down Range Register
TZASC_LOCKDOWN_SELECT_REG	0x000C	Lock Down Select Register
TZASC_INT_STATUS_REG	0x0010	Interrupt Status Register
TZASC_INT_CLEAR_REG	0x0014	Interrupt Clear Register
TZASC_MASTER_BYP_REG	0x0018	Master Bypass Register

TZASC_MASTER_SEC_REG	0x001C	Master Secure Register
TZASC_FAIL_ADDR_REG	0x0020	Fail Address Register
TZASC_FAIL_CTRL_REG	0x0028	Fail Control Register
TZASC_FAIL_ID_REG	0x002C	Fail ID Register
TZASC_SPECU_CTRL_REG	0x0030	Speculation Control Register
TZASC_SEC_INV_EN_REG	0x0034	Security Inversion Enable Register
TZASC_REGION_SETUP_REG	0x0100+N*0x10	Region Setup Register N(N=0~15)
TZASC_REGION_ATTR_REG	0x0108+N*0x10	Region Attribute Register N(N=0~15)

3.6.4. TZASC REGISTER DESCRIPTION

3.6.4.1. TZASC CONFIGURATION REGISTER(DEFAULT: 0X00001F0F)

Offset: 0x00			Register Name: TZASC_CONFIG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/.
13:8	R	0x1F	ADDR_WIDTH_RTN. Address width. Return the width of the AXI address bus. 6’b 000000-6’b011110 reserved. 6’b 011111 = 32-bit …… 6’b 111111 = 64-bit
7:4	/	/	/.
3:0	R	0xF	REGIONS_RTN. Returns the number of the regions that the TZASC provides. 4’b0000 = reserved 4’b0001 = 2 regions …… 4’b1111 = 16 regions.

3.6.4.2. TZASC ACTION REGISTER(DEFAULT: 0X00000001)

Offset: 0x04			Register Name: TZASC_ACTION_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/.
1:0	R/W	0x1	TZASC_INT_RESP. Control how the TZASC uses the bresps[1:0], rresps[1:0], and tzasc_int signals when a region permission failure occurs: 2'b00 = sets tzasc_int LOW and issues an OKEY response 2'b01 = sets tzasc_int LOW and issues a DECERR response 2'b10 = sets tzasc_int HIGH and issues an OKEY response 2'b11 = sets tzasc_int HIGH and issues a DECERR response

Notes：This action is only valid for CPU access, not for MBUS and DMA access.

3.6.4.3. TZASC LOCKDOWN_RANGE REGISTER(DEFAULT: 0X00000000)

Offset: 0x08			Register Name: TZASC_LOCKDOWN_RANGE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LOCKDOWN_EN. When set to 1, it enables the lockdown_regions field to control the regions that are to be locked.
30:4	/	/	/.
3:0	R/W	0x0	NO_REGIONS_LOCKDOWN. Control the number of regions to lockdown when the enable bit is set to 1. 4'b0000 = region no_of_regions-1 is locked 4'b0001 = region no_of_regions-1 to region no_of_regions-2 are locked

			…… 4'b1111 = region no_of_regions-1 to region no_of_regions-16 are locked

Notes:

1) no_of_regions is the value of the no_of_regions field in the configuration register.

2) The value programmed in lockdown_range register must be no larger than no_of_regions-1, or all regions are locked.

3.6.4.4. TZASC LOCKDOWN SELECT REGISTER(DEFAULT: 0X00000000)

Offset: 0x0C			Register Name: TZASC_LOCKDOWN_SELECT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/.
2	R/W	0x0	ACCESS_TYPE_SPECU. Modify the access type of the speculation_control register: 0: no effect. The speculation register remains RW. 1:speculation_control register is RO
1	R/W	0x0	ACCESS_TYPE_SEC_INV_EN. Modify the access type of the security_inversion_en register. 0:no effect. Security_inversion_en register remains RW. 1:security_inversion_en register is RO
0	R/W	0x0	ACCESS_TYPE_LOCKDOWN_RANGE. Modify the access type of the lockdown_range register. 0:no effect. Lockdown_range register remains RW 1:lockdown_range register is RO.

3.6.4.5. TZASC INTERRUPT STATUS REGISTER(DEFAULT: 0X00000000)

Offset: 0x10			Register Name: TZASC_INT_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:2	/	/	/
1	R	0x0	OVERRUN. When set to 1, it indicates the occurrence of two or more region permission failure since the interrupt was last cleared.
0	R	0x0	STATUS.. Return the status of the interrupt. 0: interrupt is inactive 1: interrupt is active.

3.6.4.6. TZASC INTERRUPT CLEAR REGISTER(DEFAULT: 0X00000000)

Offset: 0x14			Register Name: TZASC_INT_CLEAR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TZASC_CLR_REG. Write any value to the int_clear register sets the : Status bit to 0 in the int_status register Overrun bit to 0 in the int_status register. Note: It will be auto clear after the write operation.

3.6.4.7. TZASC MASTER BYPASS REGISTER (DEFAULT: 0XFFFFFFFF)

Offset: 0x18			Register Name: TZASC_MASTER_BYP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0xFFFF0FFF	TZASC_MASTER_BYPASS_EN. TZASC Master n Bypass Enable.(n = 0~31, see the Table 3-1. MASTER and MASTER ID for detail.) Note: Bit[31:0] stand for Master ID [31:0] If the master n bypass enable is set to 0, the master n access must be through the TZASC. 0: Bypass Disable

			1: Bypass Enable.

3.6.4.8. TZASC MASTER SECURE REGISTER (DEFAULT: 0X00000000)

Offset: 0x1C			Register Name: TZASC_MASTER_SEC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TZASC_MASTER_SEC. TZASC Master n (except CPU(AXI)) Secure Configuration. (n = 0~31，see the Table 3-1 for detail.) 0: secure 1: non-secure.

3.6.4.9. TZASC FAIL ADDRESS REGISTER (DEFAULT: 0X00000000)

Offset: 0x20			Register Name: TZASC_FAIL_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	FIRST_ACCESS_FAIL. Return the address bits[31:0] of the first access to fail a region permission check after the interrupt was cleared. For external 16-bit DDR2, the address[2:0] are fixed to zero. For external 32-bit DDR2 and 16-bit DDR3, the address[3:0] are fixed to zero. For external 32-bit DDR3, the address[4:0] are fixed to zero.

Notes: If the master ID=”SRAM” and the register value is within the range 0x800000 ~ 0xBFFFF, the real address should be divided by 4.

3.6.4.10. TZASC FAIL CONTROL REGISTER (DEFAULT: 0X00000000)

Offset: 0x28			Register Name: TZASC_FAIL_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R	0x0	READ_WRITE.

			Write. This bit indicates whether the first access to fail a region permission check was a write or read as: 0 = read access 1 = write access.
23:22	/	/	/
21	R	0x0	NON_SECURE. Nonsecure. After clearing the interrupt status, this bit indicates whether the first access to fail a region permission check was non-secure. Read as: 0 = secure access 1 = non-secure access
20	R	0x0	PRIVILEGED. Privileged. After clearing the interrupt status, this bit indicates whether the first access to fail a region permission check was privileged. Read as: 0 = unprivileged access. 1 = privileged access
19:0	/	/	/

3.6.4.11. TZASC FAIL ID REGISTER (DEFAULT: 0X00001F00)

Offset: 0x2C			Register Name: TZASC_FAIL_ID_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R	0x0	FAIL_BST_LEN. Fail burst length. 0 = 1 word length …… 0xf =16 words length
15:13	/	/	/

12:8	R	0x1F	FAIL_MASTER_ID. Fail Master ID. The value stands for master id, see the Table 3- 1 MASTER and MASTER ID for details.
7:4	/	/	/
3:0	R	0x0	AXI_ID_RTN. Return the master AXI ID of the first access to fail a region permission check after the interrupt was cleared.

3.6.4.12. TZASC SPECULATION CONTROL REGISTER (DEFAULT: 0X00000000)

Offset: 0x30			Register Name: TZASC_SPECU_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	WRITE_SPECU. Write_speculation. Control the write access speculation: 0 = write access speculation is enabled 1 = write access speculation is disabled.
0	R/W	0x0	READ_SPECU. Read_speculation. Control the read access speculation: 0 = read access speculation is enabled 1 = read access speculation is disabled.

3.6.4.13. TZASC SECURITY INVERSION ENABLE REGISTER (DEFAULT: 0X00000000)

Offset: 0x34			Register Name: TZASC_SEC_INV_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	SEC_INV_EN. Security_inversion_en. Controls whether the TZASC permits security inversion to occur.

			0 = security inversion is not permitted. 1 = security inversion is permitted. This enables a region to be accessible to masters in Non-secure state but not accessible to masters in Secure state.

3.6.4.14. TZASC REGION SETUP N(N=0 TO 15)(DEFAULT: 0X00000000)

Offset:0x100+N*0x10 (N=0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15)			**Register Name: TZASC_REGION_SETUP_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	R/W	0x0	BASE_ADDRESS. Controls the base address[31:15] of region<n>. The TZASC only permits a region to start at address 0x0, or at a multiple of its region size. For example, if the size of a region is 512MB, and it is not at address 0x0, the only valid settings for this field are: 17'b00100000000000000 17'b01000000000000000 17'b01100000000000000 17'b10000000000000000 17'b10100000000000000 17'b11000000000000000 17'b11100000000000000
14:0	/	/	/

Notes :

1) For region 0, this field is Read Only (RO). The TZASC sets the base address of region 0 to 0x0.

2) The base address should equal to the DRAM absolute address.

3.6.4.15. TZASC REGION ATTRIBUTES N (N=0 TO 15)(DEFAULT: 0X00000000)

Offset:0x108+N*0x10	**Register Name: TZASC_REGION_ATTR_REG**

(N=0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15)			
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	SPN. SP<n>. Permission setting for region <n>. if an AXI transaction occurs to region n, the value in the sp<n> field controls whether the TZASC permits the transaction to proceed.
27:16	/	/	/.
15:8	R/W	0x0	SUB_REGION_DISABLE. Subregion_disable. Regions are split into eight equal-sized sub-regions, and each bit enables the corresponding subregion to be disabled. Bit[15] = 1 subregion 7 is disabled. Bit[14] = 1 subregion 6 is disabled. Bit[13] = 1 subregion 5 is disabled. Bit[12] = 1 subregion 4 is disabled. Bit[11] = 1 subregion 3 is disabled. Bit[10] = 1 subregion 2 is disabled. Bit[9] = 1 subregion 1 is disabled. Bit[8] = 1 subregion 0 is disabled.
7	/	/	/
6:1	R/W	0x0	SIZE. Size<n>. size of region<n>
0	R/W	0x0	EN. EN<n>. Enable for region<n>. 0 = region < n> is disabled. 1 = region < n> is enabled.

Notes:

For region 0, this filed is reserved except SPN field.

3.6.5. TRUSTZONE PROTECTION CONTROLLER

The TrustZone Protection Controller (TZPC) provides a software interface to the protection bits in a secure system in a TruztZone design. It provides system flexibility that enables users to configure different areas of memory as secure or non-secure.

The TZPC features:

- Provide protection bits that enable you to define some memory areas as secure or non-secure;
- Support secure RAM;
- Support secure RTC;

3.6.6. TZPC CONFIGURATION TABLE

Following table shows the configurable region of TZPC.

Register	Bit	TZPC0	TZPC1	TZPC2
		Module Name	**Module Name**	**Module Name**
TZPCDECPORTx (x=0,1,2)	[0]	/	/	/
	[1]	RTC&ALARM	/	/
	[2]	/	/	/
	[3]	/	/	/
	[4]	/	/	/
	[5]	/	/	/
	[6]	/	/	/
	[7]	/	/	/

Table 3-5 TZPC Configuration Table

3.6.7. TZPC REGISTER LIST

Module Name	Base Address
TZPC	0x01c23400

Register Name	Offset	Description
TZPC_R0SIZE_REG	0x0000	TZPC R0SIZE register
TZPC_DECPORT0_STA_REG	0x0004	TZPC Decode Port0 Status
TZPC_DECPORT0_SET_REG	0x0008	TZPC Decode Port0 Set
TZPC_DECPORT0_CLR_REG	0x000C	TZPC Decode Port0 Clear

3.6.8. TZPC REGISTER DESCRIPTION

3.6.8.1. TZPC R0SIZE REGISTER(DEFAULT : 0X00000010)

Offset: 0x00			Register Name: TZPC_R0SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/.
9:0	R	0x10	SEC_RAM_SIZE. Secure RAM region size in 4KB step. 0x000: = no secure region 0x001: = 4KB secure region 0x002: = 8KB secure region 0x003: = 12KB secure region 0x004: = 16KB secure region 0x005: = 20KB secure region ……. 0x010: = 64KB secure region ……. 0x1FF: = 2044KB secure region

			0x200 or above sets the entire RAM to secure regardless of size.

3.6.8.2. TZPC DECPORT0STATUS REGISTER(DEFAULT : 0X00000000)

Offset: 0x04			Register Name: TZPC_DECPORT0_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/.
7:0	R	0x0	STA_DEC_PROT_OUT. Show the status of the decode protection output: 0: = Decode region corresponding to the bit is secure 1: = Decode region corresponding to the bit is non-secure. There is one bit of the register for each protection output (See the TZPC Configuration Table for details).

3.6.8.3. TZPC DECPORT0SET REGISTER(DEFAULT : 0X00000000)

Offset: 0x08			Register Name: TZPC_DECPORT0_SET_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/.
7:0	W	0x0	SET_DEC_PORT_OUT. Sets the corresponding decode protection output: 0: = No effect 1: = Set decode region to non-secure. There is one bit of the register for each protection output (See the TZPC Configuration Table for details).

3.6.8.4. TZPC DECPORT0CLEAR REGISTER(DEFAULT : 0X00000000)

Offset: 0x0C			Register Name: TZPC_DECPORT0_CLR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/.

7:0	W	0x0	CLR_DEC_PROT_OUT. Clears the corresponding decode protection output: 0: = No effect 1: = Set decode region to secure. There is one bit of the register for each protection output (See the TZPC Configuration Table for details).

3.7. SYSTEM CONTROL

3.7.1. OVERVIEW

A31 embeds a high speed SRAM.

Detailed memory mapping is shown below.

Area	Address	Size(Bytes)
A1	0x00000000--0x00007FFF	32K
A2	0x00044000--0x00053FFF	64K
C1		VE
C2		ACE
C3		ISP
NAND		2K
B(Secure RAM)	0x00020000--0x0002FFFF	64K
CPU0 I-Cache		32K
CPU0 D-Cache		32K
CPU1 I-Cache		32K
CPU1 D-Cache		32K
CPU2 I-Cache		32K
CPU2 D-Cache		32K
CPU3 I-Cache		32K
CPU3 D-Cache		32K
CPU L2 Cache		1024K
Total		**1442K**

Table 3-6 System Memory Mapping

3.7.2. SYSTEM CONTROL REGISTER LIST

Module Name	Base Address
SRAM	0x01C00000

Register Name	Offset	Description
SRAM_CTRL_REG0	0x0	SRAM Control Register 0
SRAM_CTRL_REG1	0x4	SRAM Control Register 1
GPU_DXT_BC_EN_REG	0x50	GPU DXT BC Enable Register
GPU_SW_CLK_GATING_REG	0x54	GPU SW Clock Gating Register
GPU_IDLE_STATUS_REG	0x58	GPU Idle Status Register
GPU_POWER_STATUS_REG	0x60	GPU Power Status Register

3.7.3. SYSTEM CONTROL REGISTER DESCRIPTION

3.7.3.1. SRAM CONTROL REGISTER 0 (DEFAULT: 0X7FFFFFFF)

Offset:0x0			Register Name: SRAM_CTRL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:0	R/W	0x7fffffff	SRAM_C1_MAP. SRAM Area C1 50K Bytes Configuration by AHB. 0: map to CPU/DMA 1: map to VE

3.7.3.2. SRAM CONTROL REGISTER 1 (DEFAULT: 0X00001300)

Offset:0x4			Register Name: SRAM_CTRL_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	BIST_DMA_CTRL_SEL. Bist and DMA control select.

			0: DMA, 1: Bist.
30:0	/	/	/.

3.7.3.3. GPU DXT BC ENABLE REGISTER (DEFAULT: 0X00000000)

Offset:0x50			Register Name: GPU_DXT_BC_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	DXT_BC_EN. 0:dxt texture compression disable 1:dxt texture compression enable

3.7.3.4. GPU SW CLOCK GATING REGISTER(DEFAULT: 0X00000001)

Offset:0x54			Register Name: GPU_SW_CLK_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11	R/W	0x0	SW_HYD_CLK_CTRL 0:no effect 1:enable hyd_clk
10	R/W	0x0	SW_CORE_CLK_CTRL 0:no effect 1:enable core_clk
9	R/W	0x0	SW_SYS_CLK_CTRL 0:no effect 1:enable sys_clk
8	R/W	0x0	SW_MEM_CLK_CTRL 0:no effect 1:enable mem_clk
7:6	/	/	/
5	R/W	0x0	POST_RST_CLK_CTRL

			0:no effect 1:enable all clks
4	R/W	0x0	SW_GLOBAL_CLK_CTRL 0: no effect; 1: enable all clocks
3:1	/	/	/
0	R/W	0x1	SW_IDLE_GATE 0: disable GPU idle signal 1: enable GPU idle signal

3.7.3.5. GPU IDLE STATUS REGISTER(DEFAULT: 0X00000001)

Offset:0x58			Register Name: GPU_IDLE_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x1	GPU_IDLE_STA. 0:gpu is busy 1:gpu is idle

3.7.3.6. GPU POWER STATUS REGISTER(DEFAULT: 0X00000000)

Offset:0x60			Register Name: GPU_POWER_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	GPU_PWR_STATUS. 0: power on(power is stable) 1: power off

3.8. PRCM

3.8.1. OVERVIEW

The PRCM (Power/Reset/Clock Management) module features:

- CPU power clamp control
- One clock output channel

3.8.2. PRCM REGISTER LIST

Module Name	Base Address
PRCM	0x01F01400

Register Name	Offset	Description
PLL_CTRL_REG0	0x0040	PLL Control Register0
PLL_CTRL_REG1	0x0044	PLL Control Register1
CLK_OUTD_REG	0x00F0	RTC CLKD OUT
CPU_PWROFF_GATING	0x0100	CPU Power Off Gating Register
VDD_SYS_PWROFF_GATING	0x0110	VDD_SYS Power Off Gating Register
GPU_PWROFF_GATING	0x0118	GPU Power Off Gating Register
VDD_SYS_PWR_RST	0x0120	VDD_SYS Power Domain Reset Register.
CPU1_PWR_CLAMP	0x0144	CPU1 Power Clamp Control
CPU2_PWR_CLAMP	0x0148	CPU2 Power Clamp Control
CPU3_PWR_CLAMP	0x014C	CPU3 Power Clamp Control

3.8.3. PRCM REGISTER DESCRIPTION

3.8.3.1. PLL CONTROL REGISTER0 (DEFAULT: 0X00101013)

Offset: 0x40			Register Name: PLL_CTRL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0	/
23:22	/	/	/
21:20	R/W	0x1	OSC24M_CLK_SEL. 24MHz clock source select.
19:14	/	/	/
13:12	R/W	0x1	INTERNALPLL_INPUT_SEL. Internal PLL input select.
11:6	/	/	/
5:4	R/W	1	USB_24M_CLK_SEL. USB 24MHz clock source select.
3:2	/	/	/
1	R/W	0x1	OSC24M_GAIN_ENHANCE.
0	R/W	0x1	PLL_BIAS_EN. PLL Bias Enable. 0: disable 1: enable

3.8.3.2. PLL CONTROL REGISTER1 (DEFAULT: 00028007)

Offset: 0x44			Register Name: PLL_CTRL_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	KEY_FIELD. Key Field for LDO Enable bit. If the key field value is 0xA7, the bit[23:0] can be modified.

23:19	/	/	/
18:16	R/W	0x2	PLLVDD_LDO_OUT_CTRL. PLLVDD LDO (both LDO and LDO1) output control. PLL_IN_PWR_SEL= 0 PLL_IN_PWR_SEL= 1 000: 1.16v 000: 1.00v 001: 1.19v 001: 1.02v 010: 1.22v 010: 1.04v 011: 1.25v 011: 1.06v 100: 1.28v 100: 1.08v 101: 1.31v 101: 1.10v 110: 1.34v 110: 1.12v 111: 1.37v 111: 1.14v **Note:** Before enable PLL, PLLVDD LDO should be set to 1.37v
15	R/W	0x1	PLL_IN_PWR_SEL. PLL Input Power Select. 0: 2.5v, 1: 3.3v
14:3	/	/	/
2	R/W	1	CRYSTAL_EN. External crystal enable.
1	R/W	1	LDO1_EN. 0: disable; 1: enable. Note: All PLL Analog Power enable (power source from pll_vdd).
0	R/W	1	LDO_EN. 0: disable; 1: enable. Note: All PLL Digital Power enable (power source from pll_vdd).

3.8.3.3. CLK_OUTD_REG (DEFAULT: 0X00000000)

Offset: 0xF0			Register Name: CLK_OUTD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CLK_OUTD_EN Clock OutputD Enable

			0: disable 1: Output Enable CLK OutputD = CLK Source / DIVIDOR-N / DIVIDOR-M.
30:26	/	/	/
25:24	R/W	0x0	CLK_OUT_SRC_SEL. 0x: LOSC 10:OSC24MHz 11:/
23:22	/	/	/
21:20	R/W	0x0	DIVIDOR_N Output Divide Factor N 00: /1 01: /2 10: /4 11: /8
19:11	/	/	/
10:8	R/W	0x0	DIVIDOR_M Output Divide Factor M 000: /1 001: /2 010: /3 …… 111: /8
7:0	/	/	/

3.8.3.4. CPU POWER OFF GATING REGISTER (DEFAULT: 0X00000000)

Offset: 0x100			Register Name:CPU_PWROFF_GATING
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/

3	R/W	0x0	PWROFF_GATING Gating the corresponding modules when CPU3 power off. 0: Invalid 1: Valid Note: This bit should be set to 1 before CPU3 power off while it should be set to 0 after the CPU3 power on.
2	R/W	0x0	PWROFF_GATING Gating the corresponding modules when CPU2 power off. 0: Invalid 1: Valid Note: This bit should be set to 1 before CPU2 power off while it should be set to 0 after the CPU2 power on.
1	R/W	0x0	PWROFF_GATING Gating the corresponding modules when CPU1 power off. 0: Invalid 1: Valid Note: This bit should be set to 1 before CPU1 power off while it should be set to 0 after the CPU1 power on.
0	R/W	0x0	PWROFF_GATING Gating the corresponding modules when CPU0 power off. 0: Invalid 1: Valid Note: This bit should be set to 1 before CPU0 power off while it should be set to 0 after the CPU0 power on.

3.8.3.5. VDD_SYS POWER OFF GATING REGISTER (DEFAULT: 0X00000000)

Offset: 0x110			Register Name: VDD_SYS_PWROFF_GATING
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/

2	R/W	0x0	AVCC_A_GATING Gating the corresponding modules to the AVCC_A Power Domain when VDD_SYS power off. 0: Invalid 1: Valid Note: This bit should be set to 1 before VDD_SYS power off while it should be set to 0 after the VDD_SYS power on.
1	R/W	0x0	DRAM_CH1_PAD_HOLD. Hold the pad of DRAM channel 1 0:Not hold 1:Hold DRAM Pad. Note: This bit should be set to 1 before VDD_SYS power off while it should be set to 0 after the VDD_SYS power on.
0	R/W	0x0	DRAM_CH0_PAD_HOLD. Hold the pad of DRAM channel 0 0:Not hold 1:Hold DRAM Pad. Note: This bit should be set to 1 before VDD_SYS power off while it should be set to 0 after the VDD_SYS power on.

3.8.3.6. GPU POWER OFF GATING REGISTER (DEFAULT: 0X00000000)

Offset: 0x118			Register Name: GPU_PWROFF_GATING
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	PWROFF_GATING Gating the corresponding modules when GPU power off. 0: Invalid 1: Valid Note: This bit should be set to 1 before GPU power off, while it should be

			set to 0 after the GPU power on.

3.8.3.7. VDD_SYS POWER DOMAIN RESET REGISTER (DEFAULT: 0X00000001)

Offset: 0x120			Register Name: VDD_SYS_PWR_RST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x1	MODULE_RST VDD_SYS Power Domain Modules should be reset before VDD_SYS power on. 0: Assert 1: De-assert

3.8.3.8. CPU1 POWER CLAMP CONTROL REGISTER (DEFAULT: 0X00000000)

Offset: 0x144			Register Name: CPU1_PWR_CLAMP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	CPU1_PWR_CLAMP. CPU1 Power Clamp Control.

3.8.3.9. CPU2 POWER CLAMP CONTROL REGISTER (DEFAULT: 0X00000000)

Offset: 0x148			Register Name: CPU2_PWR_CLAMP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	CPU2_PWR_CLAMP. CPU2 Power Clamp Control.

3.8.3.10. CPU3 POWER CLAMP CONTROL REGISTER (DEFAULT: 0X00000000)

Offset: 0x14C			Register Name: CPU3_PWR_CLAMP
Bit	**Read/Write**	**Default/Hex**	**Description**

31:8	/	/	/
7:0	R/W	0x0	CPU3_PWR_CLAMP. CPU3 Power Clamp Control.

3.9. TIMER

3.9.1. OVERVIEW

A31 supports up to 6 timers.

Timer 0/1/2/3 take inputs from internal RC oscillator, external 32768Hz crystal or OSC24M. They provide scheduler interrupt for OS to offer maximum accuracy and efficient management for systems with long or short response time. A 24-bit programmable overflow counter is supported, which can work in auto-reload mode or no-reload mode. When the current value in *Current Value Register* is counting down to zero, they will generate interrupts if interrupt enable bit is set.

Timer 4 and timer 5 can also take inputs from external CLKIN. They can be used to calculate external devices frequency.

Up to four watchdogs are supported on A31 platform to generate reset signals or interrupts.They feature a down counter that allows a watchdog period of up to 16 seconds (512000 cycles). The *Watchdog Reset Pulse Width Register* is a counter register that indicates the pulse width when the watchdog generates a reset signal, and its clock source is the watchdog clock source.

Moreover, two 32-bit AVS counters are used to synchronize video and audio in players.

3.9.2. TIMER BLOCK DIAGRAM

Figure 3-4 Timer Block Diagram

3.9.3. TIMER REGISTER LIST

Module Name	Base Address
Timer	0x01C20C00

Register Name	Offset	Description
TMR_IRQ_EN_REG	0x0	Timer IRQ Enable Register
TMR_IRQ_STA_REG	0x4	Timer Status Register
TMR0_CTRL_REG	0x10	Timer 0 Control
TMR0_INTV_VALUE_REG	0x14	Timer 0 Interval Value Register
TMR0_CUR_VALUE_REG	0x18	Timer 0 Current Value Register
TMR1_CTRL_REG	0x20	Timer 1 Control Register
TMR1_INTV_VALUE_REG	0x24	Timer 1 Interval Value Register
TMR1_CUR_VALUE_REG	0x28	Timer 1 Current Value Register
TMR2_CTRL_REG	0x30	Timer 2 Control Register
TMR2_INTV_VALUE_REG	0x34	Timer 2 Interval Value Register
TMR2_CUR_VALUE_REG	0x38	Timer 2 Current Value Register
TMR3_CTRL_REG	0x40	Timer 3 Control Register
TMR3_INTV_VALUE_REG	0x44	Timer 3 Interval Value Register
TMR3_CUR_VALUE_REG	0x48	Timer 3 Current Value Register
TMR4_CTRL_REG	0x50	Timer 4 Control Register
TMR4_INTV_VALUE_REG	0x54	Timer 4 Interval Value Register
TMR4_CUR_VALUE_REG	0x58	Timer 4 Current Value Register
TMR5_CTRL_REG	0x60	Timer 5 Control Register
TMR5_INTV_VALUE_REG	0x64	Timer 5 Interval Value Register
TMR5_CUR_VALUE_REG	0x68	Timer 5 Current Value Register
AVS_CNT_CTL_REG	0x80	AVS Control Register

AVS_CNT0_REG	0x84	AVS Counter 0 Register
AVS_CNT1_REG	0x88	AVS Counter 1 Register
AVS_CNT_DIV_REG	0x8C	AVS Divisor
WDOG1_IRQ_EN_REG	0xA0	Watchdog 1 IRQ Enable Register
WDOG1_IRQ_STA_REG	0xA4	Watchdog 1 Status Register
WDOG1_CTRL_REG	0xB0	Watchdog 1 Control Register
WDOG1_CFG_REG	0xB4	Watchdog 1 Configuration Register
WDOG1_MODE_REG	0xB8	Watchdog 1 Mode Register
WDOG2_IRQ_EN_REG	0xC0	Watchdog 2 IRQ Enable Register
WDOG2_IRQ_STA_REG	0xC4	Watchdog 2 Status Register
WDOG2_CTRL_REG	0xD0	Watchdog 2 Control Register
WDOG2_CFG_REG	0xD4	Watchdog 2 Configuration Register
WDOG2_MODE_REG	0xD8	Watchdog 2 Mode Register
WDOG3_IRQ_EN_REG	0xE0	Watchdog 3 IRQ Enable Register
WDOG3_IRQ_STA_REG	0xE4	Watchdog 3 Status Register
WDOG3_CTRL_REG	0xF0	Watchdog 3 Control Register
WDOG3_CFG_REG	0xF4	Watchdog 3 Configuration Register
WDOG3_MODE_REG	0xF8	Watchdog 3 Mode Register
WDOG4_IRQ_EN_REG	0x100	Watchdog 4 IRQ Enable Register
WDOG4_IRQ_STA_REG	0x104	Watchdog 4 Status Register
WDOG4_CTRL_REG	0x110	Watchdog 4 Control Register
WDOG4_CFG_REG	0x114	Watchdog 4 Configuration Register
WDOG4_MODE_REG	0x118	Watchdog 4 Mode Register

3.9.4. TIMER REGISTER DESCRIPTION

3.9.4.1. TIMER IRQ ENABLE REGISTER (DEFAULT: 0X00000000)

Offset:0x0	Register Name: TMR_IRQ_EN_REG

Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	TMR5_IRQ_EN. Timer 5 Interrupt Enable. 0: No effect; 1: Timer 5 Interval Value reached interrupt enable.
4	R/W	0x0	TMR4_IRQ_EN. Timer 4 Interrupt Enable. 0: No effect; 1: Timer 4 Interval Value reached interrupt enable.
3	R/W	0x0	TMR3_IRQ_EN. Timer 3 Interrupt Enable. 0: No effect; 1: Timer 3 Interval Value reached interrupt enable.
2	R/W	0x0	TMR2_IRQ_EN. Timer 2 Interrupt Enable. 0: No effect; 1: Timer 2 Interval Value reached interrupt enable.
1	R/W	0x0	TMR1_IRQ_EN. Timer 1 Interrupt Enable. 0: No effect; 1: Timer 1 Interval Value reached interrupt enable.
0	R/W	0x0	TMR0_IRQ_EN. Timer 0 Interrupt Enable. 0: No effect; 1: Timer 0 Interval Value reached interrupt enable.

3.9.4.2. TIMER IRQ STATUS REGISTER (DEFAULT: 0X00000000)

Offset:0x04	Register Name: TMR_IRQ_STA_REG

Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	TMR5_IRQ_PEND. Timer 5 IRQ Pending. Set 1 to the bit will clear it. 0: No effect; 1: Pending, timer 5 counter value is reached.
4	R/W	0x0	TMR4_IRQ_PEND. Timer 4 IRQ Pending. Set 1 to the bit will clear it. 0: No effect; 1: Pending, timer 4 counter value is reached.
3	R/W	0x0	TMR3_IRQ_PEND. Timer 3 IRQ Pending. Set 1 to the bit will clear it. 0: No effect; 1: Pending, timer 3 counter value is reached.
2	R/W	0x0	TMR2_IRQ_PEND. Timer 2 IRQ Pending. Set 1 to the bit will clear it. 0: No effect; 1: Pending, timer 2 counter value is reached.
1	R/W	0x0	TMR1_IRQ_PEND. Timer 1 IRQ Pending. Set 1 to the bit will clear it. 0: No effect; 1: Pending, timer 1 interval value is reached.
0	R/W	0x0	TMR0_IRQ_PEND. Timer 0 IRQ Pending. Set 1 to the bit will clear it. 0: No effect; 1: Pending, timer 0 interval value is reached.

3.9.4.3. TIMER 0 CONTROL REGISTER (DEFAULT: 0X00000004)

Offset:0x10	Register Name: TMR0_CTRL_REG

Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TMR0_MODE. Timer 0 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR0_CLK_PRES. Select the pre-scale of timer 0 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR0_CLK_SRC. Timer 0 Clock Source. 'N' is the value of Internal OSC Clock Prescalar register. 00: InternalOSC / N 01: OSC24M. 10: / 11: /
1	R/W	0x0	TMR0_RELOAD. Timer 0 Reload. 0: No effect, 1: Reload timer 0 Interval value. After the bit is set, it can not be written again before it's cleared

			automatically.
0	R/W	0x0	TMR0_EN. Timer 0 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.9.4.4. TIMER 0 INTERVAL VALUE REGISTER

Offset:0x14			Register Name: TMR0_INTV_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR0_INTV_VALUE. Timer 0 Interval Value.

Notes: The value setting should consider the system clock and the timer clock source.

3.9.4.5. TIMER 0 CURRENT VALUE REGISTER

Offset:0x18			Register Name: TMR0_CUR_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR0_CUR_VALUE. Timer 0 Current Value.

Notes:

Timer 0 current value is a 32-bit down-counter (from interval value to 0).

3.9.4.6. TIMER 1 CONTROL REGISTER (DEFAULT: 0X00000004)

Offset:0x20			Register Name: TMR1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TMR1_MODE. Timer 1 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR1_CLK_PRES. Select the pre-scale of timer 1 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR1_CLK_SRC. Timer 1 Clock Source. ‘N’ is the value of Internal OSC Clock Prescalar register. 00: InternalOSC / N 01: OSC24M. 10: / 11: /.

1	R/W	0x0	TMR1_RELOAD. Timer 1 Reload. 0: No effect, 1: Reload timer 1 Interval value. After the bit is set, it can not be written again before it's cleared automatically.
0	R/W	0x0	TMR1_EN. Timer 1 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.9.4.7. TIMER 1 INTERVAL VALUE REGISTER

Offset:0x24			Register Name: TMR1_INTV_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR1_INTV_VALUE. Timer 1 Interval Value.

Notes: The value setting should consider the system clock and the timer clock source.

3.9.4.8. TIMER 1 CURRENT VALUE REGISTER

Offset:0x28	Register Name: TMR1_CUR_VALUE_REG

Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TMR1_CUR_VALUE. Timer 1 Current Value.

Notes: Timer 1 current value is a 32-bit down-counter (from interval value to 0).

3.9.4.9. TIMER 2 CONTROL REGISTER (DEFAULT: 0X00000004)

Offset:0x30			Register Name: TMR2_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TMR2_MODE. Timer 2 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR2_CLK_PRES. Select the pre-scale of timer 2 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR2_CLK_SRC. Timer 2 Clock Source. ‘N’ is the value of Internal OSC Clock Prescalar register. 00: InternalOSC / N

			01: OSC24M. 1x: /.
1	R/W	0x0	TMR2_RELOAD. Timer 2 Reload. 0: No effect, 1: Reload timer 2 Interval value. After the bit is set, it can not be written again before it's cleared automatically.
0	R/W	0x0	TMR2_EN. Timer 2 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.9.4.10. TIMER 2 INTERVAL VALUE REGISTER

Offset:0x34			Register Name: TMR2_INTV_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR2_INTV_VALUE. Timer 2 Interval Value.

Notes: When set the value, you should take into consideration the system clock and the timer clock source.

3.9.4.11. TIMER 2 CURRENT VALUE REGISTER

Offset:0x38			Register Name: TMR2_CUR_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR2_CUR_VALUE. Timer 2 Current Value.

Notes: Timer current value is a 32-bit down-counter (from interval value to 0).

3.9.4.12. TIMER 3 CONTROL REGISTER (DEFAULT: 0X00000004)

Offset:0x40			Register Name: TMR3_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TMR3_MODE. Timer 3 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR3_CLK_PRES. Select the pre-scale of timer 3 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR3_CLK_SRC. Timer 3 Clock Source. ‘N’ is the value of Internal OSC Clock

			Prescalar register. 00: InternalOSC / N 01: OSC24M. 1x: /
1	R/W	0x0	TMR3_RELOAD. Timer 3 Reload. 0: No effect, 1: Reload timer 3 Interval value. After the bit is set, it can not be written again before it's cleared automatically.
0	R/W	0x0	TMR3_EN. Timer 3 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 3 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.9.4.13. TIMER 3 INTERVAL VALUE REGISTER

Offset:0x44			Register Name: TMR3_INTV_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR3_INTV_VALUE. Timer 3 Interval Value.

Notes: When set the values, you should take into consideration the system clock and the timer clock source.

3.9.4.14. TIMER 3 CURRENT VALUE REGISTER

Offset:0x48			Register Name: TMR3_CUR_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR3_CUR_VALUE. Timer 3 Current Value.

Notes: Timer current value is a 32-bit down-counter (from interval value to 0).

3.9.4.15. TIMER 4 CONTROL REGISTER (DEFAULT: 0X00000004)

Offset:0x50			Register Name: TMR4_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/.
7	R/W	0x0	TMR4_MODE. Timer 4 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR4_CLK_PRES. Select the pre-scale of timer 4 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128

3:2	R/W	0x1	TMR4_CLK_SRC. Timer 4 Clock Source. 'N' is the value of Internal OSC Clock Prescalar register. 00: InternalOSC / N 01: OSC24M. 10: External CLKIN0 11: /
1	R/W	0x0	TMR4_RELOAD. Timer 4 Reload. 0: No effect, 1: Reload timer 4 Interval value. After the bit is set, it can not be written again before it's cleared automatically.
0	R/W	0x0	TMR4_EN. Timer 4 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

Notes：If the clock source is External CLKIN, the interval value register is not used, the current value register is an up counter that counting from 0.

3.9.4.16. TIMER 4 INTERVAL VALUE REGISTER

Offset:0x54			Register Name: TMR4_INTV_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR4_INTV_VALUE. Timer 4 Interval Value.

Notes: When set the value, you should take into consideration the system clock and the timer clock source.

3.9.4.17. TIMER 4 CURRENT VALUE REGISTER

Offset:0x58			Register Name: TMR4_CUR_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR4_CUR_VALUE. Timer 4 Current Value.

Notes: Timer current value is a 32-bit down-counter (from interval value to 0).

3.9.4.18. TIMER 5 CONTROL REGISTER (DEFAULT: 0X00000004)

Offset:0x60			Register Name: TMR5_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TMR5_MODE. Timer 5 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR5_CLK_PRES. Select the pre-scale of timer 5 clock source. 000: /1 001: /2 010: /4

			011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR5_CLK_SRC. Timer 5 Clock Source. 'N' is the value of Internal OSC Clock Prescalar register. 00: InternalOSC / N 01: OSC24M. 10: External CLKIN1 11: /.
1	R/W	0x0	TMR5_RELOAD. Timer 5 Reload. 0: No effect, 1: Reload timer 5 Interval value. After the bit is set, it can not be written again before it's cleared automatically.
0	R/W	0x0	TMR5_EN. Timer 5 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the

			reload bit and the enable bit should be set to 1 at the same time.

Notes：If the clock source is External CLKIN, the interval value register is not used, the current value register is an up counter that counting from 0.

3.9.4.19. TIMER 5 INTERVAL VALUE REGISTER

Offset:0x64			Register Name: TMR5_INTV_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR5_INTV_VALUE. Timer 5 Interval Value.

Notes: the value setting should consider the system clock and the timer clock source.

3.9.4.20. TIMER 5 CURRENT VALUE REGISTER

Offset:0x68			Register Name: TMR5_CUR_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR5_CUR_VALUE. Timer 5 Current Value.

Notes: Timer 5 current value is a 32-bit down-counter (from interval value to 0).

3.9.4.21. AVS COUNTER CONTROL REGISTER (DEFAULT: 0X00000000)

Offset:0x80			Register Name: AVS_CNT_CTL_REG
Bit	**Read /Write**	**Default**	**Description**
31:10	/	/	/
9	R/W	0x0	AVS_CNT1_PS. Audio/Video Sync Counter 1 Pause Control 0: Not pause 1: Pause Counter 1
8	R/W	0x0	AVS_CNT0_PS.

			Audio/Video Sync Counter 0 Pause Control 0: Not pause 1: Pause Counter 0
7:2	/	/	/
1	R/W	0x0	AVS_CNT1_EN. Audio/Video Sync Counter 1 Enable/ Disable. The counter source is OSC24M. 0: Disable 1: Enable
0	R/W	0x0	AVS_CNT0_EN. Audio/Video Sync Counter 1 Enable/ Disable. The counter source is OSC24M. 0: Disable 1: Enable

3.9.4.22. AVS COUNTER 0 REGISTER (DEFAULT: 0X00000000)

Offset:0x84			Register Name: AVS_CNT0_REG
Bit	**Read /Write**	**Default**	**Description**
31:0	R/W	0x0	AVS_CNT0. Counter 0 for Audio/ Video Sync Application The high 32 bits of the internal 33-bits counter register. The initial value of the internal 33-bits counter register can be set by software. The LSB bit of the 33-bits counter register should be zero when the initial value is updated. It will count from the initial value. The initial value can be updated at any time. It can also be paused by setting AVS_CNT0_PS to '1'. When it is paused, the counter won't increase.

3.9.4.23. AVS COUNTER 1 REGISTER (DEFAULT: 0X00000000)

Offset:0x88			Register Name: AVS_CNT1_REG
Bit	Read /Write	Default	Description
31:0	R/W	0x0	AVS_CNT1. Counter 1 for Audio/ Video Sync Application The high 32 bits of the internal 33-bits counter register. The initial value of the internal 33-bits counter register can be set by software. The LSB bit of the 33-bits counter register should be zero when the initial value is updated. It will count from the initial value. The initial value can be updated at any time. It can also be paused by setting AVS_CNT1_PS to '1'. When it is paused, the counter won't increase.

3.9.4.24. AVS COUNTER DIVISOR REGISTER (DEFAULT: 0X05DB05DB)

Offset:0x8C			Register Name: AVS_CNT_DIV_REG
Bit	Read /Write	Default	Description
31:28	/	/	/
27:16	R/W	0x5DB	AVS_CNT1_D. Divisor N for AVS Counter 1 AVS CN1 CLK=24MHz/Divisor_N1. Divisor N1 = Bit [27:16] + 1. The number N is from 1 to 0x7ff. The zero value is reserved. The internal 33-bits counter engine will maintain another 12-bits counter. The 12-bits counter is used for counting the cycle number of one 24Mhz clock. When the 12-bits counter reaches (>= N) the divisor value, the internal 33-bits counter register will increase 1 and the 12-bits counter will reset to zero and restart again. ***Note***: It can be configured by software at any time.

15:12	/	/	/
11:0	R/W	0x5DB	AVS_CNT0_D. Divisor N for AVS Counter 0 AVS CN0 CLK=24MHz/Divisor_N0. Divisor N0 = Bit [11:0] + 1 The number N is from 1 to 0x7ff. The zero value is reserved. The internal 33-bits counter engine will maintain another 12-bits counter. The 12-bits counter is used for counting the cycle number of one 24Mhz clock. When the 12-bits counter reaches (>= N) the divisor value, the internal 33-bits counter register will increase 1 and the 12-bits counter will reset to zero and restart again. ***Note***: It can be configured by software at any time.

3.9.4.25. WATCHDOG 1 IRQ ENABLE REGISTER (DEFAULT: 0X00000000)

Offset:0xA0			**Register Name: WDOG1_IRQ_EN_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	WDOG1_IRQ_EN. Watchdog 1 Interrupt Enable. 0: No effect, 1: Watchdog 1 interrupt enable.

3.9.4.26. WATCHDOG 1 STATUS REGISTER (DEFAULT: 0X00000000)

Offset:0xA4			**Register Name: WDOG1_IRQ_STA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	WDOG1_IRQ _PEND. Watchdog 1 IRQ Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending, Watchdog 1 interval value is reached.

3.9.4.27. WATCHDOG 1 CONTROL REGISTER (DEFAULT: 0X00000000)

Offset:0xB0			Register Name: WDOG1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	WDOG1_RSTART. Watchdog 1 Restart. 0: No effect, 1: Restart the Watchdog 1.

3.9.4.28. WATCHDOG 1 CONFIGURATION REGISTER (DEFAULT: 0X00000000)

Offset:0xB4			Register Name: WDOG1_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	WDOG1_CONFIG. Watchdog 1 generates a reset signal 00: / 01: to whole system 10: only interrupt 11: /

3.9.4.29. WATCHDOG 1 MODE REGISTER (DEFAULT: 0X00000000)

Offset:0xB8			Register Name: WDOG1_MODE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:4	R/W	0x0	WDOG1_INTV_VALUE. Watchdog 1 Interval Value Watchdog 1 clock source is *OSC24M / 750*. If the clock source is turned off, Watchdog 1 will not work. 0000: 16000 cycles (0.5s) 0001: 32000 cycles (1s)

			0010: 64000 cycles (2s) 0011: 96000 cycles (3s) 0100: 128000 cycles (4s) 0101: 160000 cycles (5s) 0110: 192000 cycles (6s) 0111: 256000 cycles (8s) 1000: 320000 cycles (10s) 1001: 384000 cycles (12s) 1010: 448000 cycles (14s) 1011: 512000 cycles (16s) others: /
3:1	/	/	/
0	R/W	0x0	WDOG1_EN. Watchdog 1 Enable. 0: No effect; 1: Enable the Watchdog 1.

3.9.4.30. WATCHDOG 2 IRQ ENABLE REGISTER (DEFAULT: 0X00000000)

Offset:0xC0			Register Name: WDOG2_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	WDOG2_IRQ_EN. Watchdog 2 Interrupt Enable. 0: No effect, 1: Watchdog 2 interrupt enable.

3.9.4.31. WATCHDOG 2 STATUS REGISTER (DEFAULT: 0X00000000)

Offset:0xC4			Register Name: WDOG2_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/

0	R/W	0x0	WDOG2_IRQ _PEND. Watchdog 2 IRQ Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending, Watchdog 2 interval value is reached.

3.9.4.32. WATCHDOG 2 CONTROL REGISTER (DEFAULT: 0X00000000)

Offset:0xD0			Register Name: WDOG2_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:1	R/W	0x0	/
0	R/W	0x0	WDOG2_RSTART. Watchdog 2 Restart. 0: No effect, 1: Restart the Watchdog 2.

3.9.4.33. WATCHDOG 2 CONFIGURATION REGISTER (DEFAULT: 0X00000000)

Offset:0xD4			Register Name: WDOG2_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/.
1:0	R/W	0x0	WDOG2_CONFIG. Watchdog 2 generates a reset signal 00: / 01: to whole system 10: only interrupt 11: /

3.9.4.34. WATCHDOG 2 MODE REGISTER (DEFAULT: 0X00000000)

Offset:0xD8			Register Name: WDOG2_MODE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/.
7:4	R/W	0x0	WDOG2_INTV_VALUE.

			Watchdog 2 Interval Value Watchdog 2 clock source is *OSC24M / 750*. If the clock source is turned off, Watchdog 2 will not work. 0000: 16000 cycles (0.5s) 0001: 32000 cycles (1s) 0010: 64000 cycles (2s) 0011: 96000 cycles (3s) 0100: 128000 cycles (4s) 0101: 160000 cycles (5s) 0110: 192000 cycles (6s) 0111: 256000 cycles (8s) 1000: 320000 cycles (10s) 1001: 384000 cycles (12s) 1010: 448000 cycles (14s) 1011: 512000 cycles (16s) others: /
3:1	/	/	/
0	R/W	0x0	WDOG2_EN. Watchdog 2 Enable. 0: No effect; 1: Enable the Watchdog 2.

3.9.4.35. WATCHDOG 3 IRQ ENABLE REGISTER (DEFAULT: 0X00000000)

Offset:0xE0			Register Name: WDOG3_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/.
0	R/W	0x0	WDOG3_IRQ_EN. Watchdog 1 Interrupt Enable. 0: No effect, 1: Watchdog 3 interrupt enable.

3.9.4.36. WATCHDOG 3 STATUS REGISTER (DEFAULT: 0X00000000)

Offset:0xE4			Register Name: WDOG3_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/.
0	R/W	0x0	WDOG3_IRQ _PEND. Watchdog 3 IRQ Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending, Watchdog 3 interval value is reached.

3.9.4.37. WATCHDOG 3 CONTROL REGISTER (DEFAULT: 0X00000000)

Offset:0xF0			Register Name: WDOG3_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:1	R/W	0x0	/
0	R/W	0x0	WDOG3_RSTART. Watchdog 3 Restart. 0: No effect; 1: Restart the Watchdog 3.

3.9.4.38. WATCHDOG 3 CONFIGURATION REGISTER (DEFAULT: 0X00000000)

Offset:0xF4			Register Name: WDOG3_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/.
1:0	R/W	0x0	WDOG3_CONFIG. Watchdog 3 generates a reset signal 00: / 01: to whole system 10: only interrupt 11: /

3.9.4.39. WATCHDOG 3 MODE REGISTER (DEFAULT: 0X00000000)

Offset:0xF8			Register Name: WDOG3_MODE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:4	R/W	0x0	WDOG3_INTV_VALUE. Watchdog 3 Interval Value Watchdog 3 clock source is *OSC24M / 750*. If the clock source is turned off, Watchdog 3 will not work. 0000: 16000 cycles (0.5s) 0001: 32000 cycles (1s) 0010: 64000 cycles (2s) 0011: 96000 cycles (3s) 0100: 128000 cycles (4s) 0101: 160000 cycles (5s) 0110: 192000 cycles (6s) 0111: 256000 cycles (8s) 1000: 320000 cycles (10s) 1001: 384000 cycles (12s) 1010: 448000 cycles (14s) 1011: 512000 cycles (16s) others: /
3:1	/	/	/
0	R/W	0x0	WDOG3_EN. Watchdog 3 Enable. 0: No effect, 1: Enable the Watchdog 3.

3.9.4.40. WATCHDOG 4 IRQ ENABLE REGISTER (DEFAULT: 0X00000000)

Offset:0x100	Register Name: WDOG4_IRQ_EN_REG

Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	WDOG4_IRQ_EN. Watchdog 1 Interrupt Enable. 0: No effect, 1: Watchdog 4 interrupt enable.

3.9.4.41. WATCHDOG 4 STATUS REGISTER (DEFAULT: 0X00000000)

Offset: 0x104			Register Name: WDOG4_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/.
0	R/W	0x0	WDOG4_IRQ _PEND. Watchdog 4 IRQ Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending, Watchdog 4 interval value is reached.

3.9.4.42. WATCHDOG 4 CONTROL REGISTER (DEFAULT: 0X00000000)

Offset:0x110			Register Name: WDOG4_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:1	R/W	0x0	/
0	R/W	0x0	WDOG4_RSTART. Watchdog 4 Restart. 0: No effect, 1: Restart the Watchdog 4.

3.9.4.43. WATCHDOG 4 CONFIGURATION REGISTER (DEFAULT: 0X00000000)

Offset:0x114			Register Name: WDOG4_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	WDOG4_CONFIG. Watchdog 4 generates a reset signal

			00:/ 01: to whole system 10: only interrupt 11: /

3.9.4.44. WATCHDOG 4 MODE REGISTER (DEFAULT: 0X00000000)

Offset:0x118			Register Name: WDOG4_MODE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:4	R/W	0x0	WDOG4_INTV_VALUE. Watchdog 4 Interval Value Watchdog 4 clock source is *OSC24M / 750*. If the clock source is turned off, Watchdog 4 will not work. 0000: 16000 cycles (0.5s) 0001: 32000 cycles (1s) 0010: 64000 cycles (2s) 0011: 96000 cycles (3s) 0100: 128000 cycles (4s) 0101: 160000 cycles (5s) 0110: 192000 cycles (6s) 0111: 256000 cycles (8s) 1000: 320000 cycles (10s) 1001: 384000 cycles (12s) 1010: 448000 cycles (14s) 1011: 512000 cycles (16s) others: /
3:1	/	/	/
0	R/W	0x0	WDOG4_EN. Watchdog 4 Enable.

			0: No effect; 1: Enable the Watchdog 4.

3.10. HIGH SPEED TIMER

3.10.1. OVERVIEW

There are four high speed timers (HS_Timer 0/1/2/3) supported on A31 platform, and their clock source is fixed to AHB clock.

3.10.2. HIGH SPEED TIMER REGISTER LIST

Module Name	Base Address
High Speed Timer	0x01C60000

Register Name	Offset	Description
HS_TMR_IRQ_EN_REG	0x0	HS Timer IRQ Enable Register
HS_TMR_IRQ_STAS_REG	0x4	HS Timer Status Register
HS_TMR0_CTRL_REG	0x10	HS Timer 0 Control Register
HS_TMR0_INTV_LO_REG	0x14	HS Timer 0 Interval Value Low Register
HS_TMR0_INTV_HI_REG	0x18	HS Timer 0 Interval Value High Register
HS_TMR0_CURNT_LO_REG	0x1C	HS Timer 0 Current Value Low Register
HS_TMR0_CURNT_HI_REG	0x20	HS Timer 0 Current Value High Register
HS_TMR1_CTRL_REG	0x30	HS Timer 1 Control Register
HS_TMR1_INTV_LO_REG	0x34	HS Timer 1 Interval Value Low Register
HS_TMR1_INTV_HI_REG	0x38	HS Timer 1 Interval Value High Register
HS_TMR1_CURNT_LO_REG	0x3C	HS Timer 1 Current Value Low Register
HS_TMR1_CURNT_HI_REG	0x40	HS Timer 1 Current Value High Register
HS_TMR2_CTRL_REG	0x50	HS Timer 2 Control Register
HS_TMR2_INTV_LO_REG	0x54	HS Timer 2 Interval Value Low Register

HS_TMR2_INTV_HI_REG	0x58	HS Timer 2 Interval Value High Register
HS_TMR2_CURNT_LO_REG	0x5C	HS Timer 2 Current Value Low Register
HS_TMR2_CURNT_HI_REG	0x60	HS Timer 2 Current Value High Register
HS_TMR3_CTRL_REG	0x70	HS Timer 3 Control Register
HS_TMR3_INTV_LO_REG	0x74	HS Timer 3 Interval Value Low Register
HS_TMR3_INTV_HI_REG	0x78	HS Timer 3 Interval Value High Register
HS_TMR3_CURNT_LO_REG	0x7C	HS Timer 3 Current Value Low Register
HS_TMR3_CURNT_HI_REG	0x80	HS Timer 3 Current Value High Register

3.10.3. HIGH SPEED TIMER REGISTER DESCRIPTION

3.10.3.1. HS TIMER IRQ ENABLE REGISTER (DEFAULT: 0X00000000)

Offset:0x0			Register Name: HS_TMR_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	HS_TMR3_INT_EN. High Speed Timer 3 Interrupt Enable. 0: No effect; 1: High Speed Timer 3 Interval Value reached interrupt enable.
2	R/W	0x0	HS_TMR2_INT_EN. High Speed Timer 2 Interrupt Enable. 0: No effect; 1: High Speed Timer 2 Interval Value reached interrupt enable.
1	R/W	0x0	HS_TMR1_INT_EN. High Speed Timer 1 Interrupt Enable. 0: No effect; 1: High Speed Timer 1 Interval Value reached interrupt enable.
0	R/W	0x0	HS_TMR0_INT_EN. High Speed Timer 0 Interrupt Enable.

			0: No effect; 1: High Speed Timer 0 Interval Value reached interrupt enable.

3.10.3.2. HS TIMER IRQ STATUS REGISTER (DEFAULT: 0X00000000)

Offset:0x4			Register Name: HS_TMR_IRQ_STAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	HS_TMR3_IRQ_PEND. High Speed Timer 3 IRQ Pending. Set 1 to the bit will clear it. 0: No effect; 1: Pending, High speed timer 3 interval value is reached.
2	R/W	0x0	HS_TMR2_IRQ_PEND. High Speed Timer 2 IRQ Pending. Set 1 to the bit will clear it. 0: No effect; 1: Pending, High speed timer 2 interval value is reached.
1	R/W	0x0	HS_TMR1_IRQ_PEND. High Speed Timer 1 IRQ Pending. Set 1 to the bit will clear it. 0: No effect; 1: Pending, High speed timer 1 interval value is reached.
0	R/W	0x0	HS_TMR0_IRQ_PEND. High Speed Timer 0 IRQ Pending. Set 1 to the bit will clear it. 0: No effect; 1: Pending, High speed timer 0 interval value is reached.

3.10.3.3. HS TIMER 0 CONTROL REGISTER (DEFAULT: 0X00000000)

Offset:0x10			Register Name: HS_TMR0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	/
30:8	/	/	/

7	R/W	0x0	HS_TMR0_MODE. High Speed Timer 0 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	HS_TMR0_CLK Select the pre-scale of the high speed timer 0 clock sources. 000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: /
3:2	/	/	/
1	R/W	0x0	HS_TMR0_RELOAD. High Speed Timer 0 Reload. 0: No effect, 1: Reload High Speed Timer 0 Interval Value.
0	R/W	0x0	HS_TMR0_EN. High Speed Timer 0 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If

			the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.10.3.4. HS TIMER 0 INTERVAL VALUE LO REGISTER

Offset:0x14			Register Name: HS_TMR0_INTV_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	x	HS_TMR0_INTV_VALUE_LO. High Speed Timer 0 Interval Value [31:0].

3.10.3.5. HS TIMER 0 INTERVAL VALUE HI REGISTER

Offset:0x18			Register Name: HS_TMR0_INTV_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	x	HS_TMR0_INTV_VALUE_HI. High Speed Timer 0 Interval Value [55:32].

Notes: The interval value register is a 56-bit register. When read or write the interval value, the Lo register should be read or write first. And the Hi register should be written after the Lo register.

3.10.3.6. HS TIMER 0 CURRENT VALUE LO REGISTER

Offset:0x1C			Register Name: HS_TMR0_CURNT_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	x	HS_TMR0_CUR_VALUE_LO. High Speed Timer 0 Current Value [31:0].

3.10.3.7. HS TIMER 0 CURRENT VALUE HI REGISTER

Offset:0x20			Register Name: HS_TMR0_CURNT_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/

23:0	R/W	x	HS_TMR0_CUR_VALUE_HI. High Speed Timer 0 Current Value [55:32].

Notes:

1) HS timer 0 current value is a 56-bit down-counter (from interval value to 0).

2) The current value register is a 56-bit register. When read or write the current value, the Lo register should be read or write first.

3.10.3.8. HS TIMER 1 CONTROL REGISTER (DEFAULT: 0X00000000)

Offset:0x30			Register Name:HS_TMR1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	/
30:8	/	/	/
7	R/W	0x0	HS_TMR1_MODE. High Speed Timer 1 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	HS_TMR1_CLK_SRC. Select the pre-scale of the high speed timer 1 clock sources. 000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: /
3:2	/	/	/

1	R/W	0x0	HS_TMR1_RELOAD. High Speed Timer 1 Reload. 0: No effect, 1: Reload High Speed Timer 1 Interval Value.
0	R/W	0x0	HS_TMR1_EN. High Speed Timer 1 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.10.3.9. HS TIMER 1 INTERVAL VALUE LO REGISTER

Offset:0x34			Register Name: HS_TMR1_INTV_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	x	HS_TMR1_INTV_VALUE_LO. High Speed Timer 1 Interval Value [31:0].

3.10.3.10. HS TIMER 1 INTERVAL VALUE HI REGISTER

Offset:0x38			Register Name: HS_TMR1_INTV_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	x	HS_TMR1_INTV_VALUE_HI. High Speed Timer 1 Interval Value [55:32].

Notes: The interval value register is a 56-bit register. When read or write the interval value, the Lo register

should be read or write first. And the Hi register should be written after the Lo register.

3.10.3.11. HS TIMER 1 CURRENT VALUE LO REGISTER

Offset:0x3C			Register Name: HS_TMR1_CURNT_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	x	HS_TMR1_CUR_VALUE_LO. High Speed Timer 1 Current Value [31:0].

3.10.3.12. HS TIMER 1 CURRENT VALUE HI REGISTER

Offset:0x40			Register Name: HS_TMR1_CURNT_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	**/**	**/**	**/**
23:0	R/W	x	HS_TMR1_CUR_VALUE_HI. High Speed Timer 1 Current Value [55:32].

Notes:

1) HS timer 1 current value is a 56-bit down-counter (from interval value to 0).

2) The current value register is a 56-bit register. When read or write the current value, the Low register should be read or write first

3.10.3.13. HS TIMER 2 CONTROL REGISTER (DEFAULT: 0X00000000)

Offset:0x50			Register Name: HS_TMR2_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	/
30:8	/	/	/
7	R/W	0x0	HS_TMR2_MODE. High Speed Timer 2 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable

			automatically.
6:4	R/W	0x0	HS_TMR0_CLK Select the pre-scale of the high speed timer 0 clock sources. 000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: /
3:2	/	/	/
1	R/W	0x0	HS_TMR2_RELOAD. High Speed Timer 2 Reload. 0: No effect, 1: Reload High Speed Timer 2 Interval Value.
0	R/W	0x0	HS_TMR2_EN. High Speed Timer 2 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.10.3.14. HS TIMER 2 INTERVAL VALUE LO REGISTER

Offset:0x54			Register Name: HS_TMR2_INTV_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	x	HS_TMR2_INTV_VALUE_LO. High Speed Timer 2 Interval Value [31:0].

3.10.3.15. HS TIMER 2 INTERVAL VALUE HI REGISTER

Offset:0x58			Register Name: HS_TMR2_INTV_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	x	HS_TMR2_INTV_VALUE_HI. High Speed Timer 2 Interval Value [55:32].

Notes: The interval value register is a 56-bit register. When read or write the interval value, the Lo register should be read or write first. And the Hi register should be written after the Lo register.

3.10.3.16. HS TIMER 2 CURRENT VALUE LO REGISTER

Offset: 0x5C			Register Name: HS_TMR2_CURNT_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	x	HS_TMR2_CUR_VALUE_LO. High Speed Timer 2 Current Value [31:0].

3.10.3.17. HS TIMER 2 CURRENT VALUE HI REGISTER

Offset: 0x60			Register Name: HS_TMR2_CURNT_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	x	HS_TMR2_CUR_VALUE_HI. High Speed Timer 2 Current Value [55:32].

Notes:

1) High speed timer 2 current value is a 56-bit down-counter (from interval value to 0).

2) The current value register is a 56-bit register. When read or write the current value, the Lo register should be read or write first.

3.10.3.18. HS TIMER 3 CONTROL REGISTER (DEFAULT: 0X00000000)

Offset: 0x70			Register Name:HS_TMR3_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	/
30:8	/	/	/
7	R/W	0x0	HS_TMR3_MODE. High Speed Timer 3 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	HS_TMR3_CLK_SRC. Select the pre-scale of the high speed timer 3 clock sources. 000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: /
3:2	/	/	/
1	R/W	0x0	HS_TMR3_RELOAD. High Speed Timer 3 Reload. 0: No effect, 1: Reload High Speed Timer 3 Interval Value.
0	R/W	0x0	HS_TMR3_EN.

			High Speed Timer 3 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.10.3.19. HS TIMER 3 INTERVAL VALUE LO REGISTER

Offset: 0x74			Register Name: HS_TMR3_INTV_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	x	HS_TMR3_INTV_VALUE_LO. High Speed Timer 3 Interval Value [31:0].

3.10.3.20. HS TIMER 3 INTERVAL VALUE HI REGISTER

Offset: 0x78			Register Name: HS_TMR3_INTV_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	**/**	**/**	**/**
23:0	R/W	x	HS_TMR3_INTV_VALUE_HI. High Speed Timer 3 Interval Value [55:32].

Notes: The interval value register is a 56-bit register. When read or write the interval value, the Lo register should be read or write first. And the Hi register should be written after the Lo register.

3.10.3.21. HS TIMER 3 CURRENT VALUE LO REGISTER

Offset: 0x7C	Register Name: HS_TMR3_CURNT_LO_REG

Bit	Read/Write	Default/Hex	Description
31:0	R/W	x	HS_TMR3_CUR_VALUE_LO. High Speed Timer 3 Current Value [31:0].

3.10.3.22. HS TIMER 3 CURRENT VALUE HI REGISTER

Offset: 0x80			Register Name: HS_TMR3_CURNT_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	x	HS_TMR3_CUR_VALUE_HI. High Speed Timer 3 Current Value [55:32].

Notes:

1) High speed timer 1 current value is a 56-bit down-counter (from interval value to 0).

2) The current value register is a 56-bit register. When read or write the current value, the Low register should be read or write first.

3.11. PWM

3.11.1. OVERVIEW

The PWM signals can be used for LCD contrast and brightness control.

The PWM outputs a toggling signal, whose frequency and duty cycle can be modulated in its programmable registers. Each channel has a dedicated internal 16-bit up counter, which will be reset if it reaches the value stored in the channel period register. At the beginning of a count period cycle, the PWMOUT is set to active state and counts from 0x0000.

When enabled, PWM can output two signals, which are reversed on two pins; when disabled, PWM can control the status of two pins.
The PWM divider divides the clock (24MHz) by 1-64 according to the pre-scalar bits in PWM control register. The PWM output frequency can be divided by 65536 at most.

PWM has two modes: in PWM cycle mode, the output will be a square waveform, and the frequency is set to the period register; in PWM pulse mode, the output will be a positive pulse or a negative pulse.

3.11.2. PWM BLOCK DIAGRAM

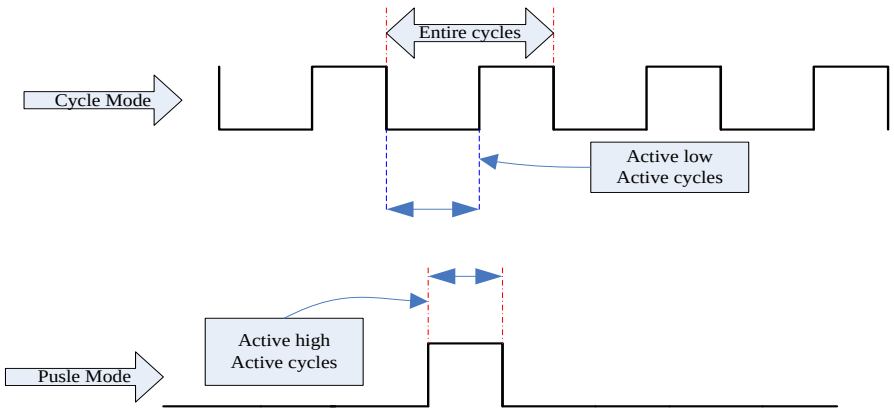


Figure 3-5 PWM Block Diagram

3.11.3. PWM REGISTER LIST

Module Name	Base Address
PWM	0x01C21400

Register Name	Offset	Description
PWM_CH0_CTRL	0x0	PWM Channel 0 Control Register
PWM_CH0_PERIOD	0x4	PWM Channel 0 Period Register
PWM_CH1_CTRL	0x10	PWM Channel 1 Control Register
PWM_CH1_PERIOD	0x14	PWM Channel 1 Period Register
PWM_CH2_CTRL	0x20	PWM Channel 2 Control Register
PWM_CH2_PERIOD	0x24	PWM Channel 2 Period Register
PWM_CH3_CTRL	0x30	PWM Channel 3 Control Register
PWM_CH3_PERIOD	0x34	PWM Channel 3 Period Register

3.11.4. PWM REGISTER DESCRIPTION

3.11.4.1. PWM CHANNEL 0 CONTROL REGISTER (DEFAULT: 0X00000000)

Offset:0x0			Register Name: PWM_CH0_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R	0x0	PWM0_RDY. PWM0 period register ready. 0: PWM0 period register is ready to write; 1: PWM0 period register is busy.
27:12	/	/	/
11:10	R/W	0x0	PWM0_PIN_STATUS. When PWM is disable, two output pins' status can be changed. 00: both low 01: pin 0 is high, pin 1 is low 10: pin 0 is low, pin 1 is high 11: both high
9	/	/	/
8	R/W	0x0	PWM_CH0_PUL_START. PWM Channel 0 pulse output start. 0: no effect, 1: output 1 pulse. The pulse width should be according to the period 0 register [15:0], and the pulse state should be according to the active state. After the pulse is finished, the bit will be cleared automatically.
7	R/W	0x0	PWM_CHANNEL0_MODE. 0: cycle mode, 1: pulse mode.
6	R/W	0x0	SCLK_CH0_GATING.

			Gating the Special Clock for PWM0 (0: mask, 1: pass).
5	R/W	0x0	PWM_CH0_ACT_STA. PWM Channel 0 Active State. 0: Low Level, 1: High Level.
4	R/W	0x0	PWM_CH0_EN. PWM Channel 0 Enable. 0: Disable, 1: Enable.
3:0	R/W	0x0	PWM_CH0_PRESCAL. PWM Channel 0 Prescalar. These bits should be setting before the PWM Channel 0 clock gate on. 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 others: /

3.11.4.2. PWM CHANNEL 0 PERIOD REGISTER

Offset:0x4			Register Name: PWM_CH0_PERIOD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	x	PWM_CH0_ENTIRE_CYS Number of the entire cycles in the PWM clock. 0 = 1 cycle 1 = 2 cycles …… N = N+1 cycles

			If the register need to be modified dynamically, the PCLK should be faster than the PWM CLK (PWM CLK = 24MHz/prescale).
15:0	R/W	x	PWM_CH0_ENTIRE_ACT_CYS Number of the active cycles in the PWM clock. 0 = 0 cycle 1 = 1 cycles …… N = N cycles

Notes: When the active cycles are larger than the period cycles, the duty cycle is 100%.

3.11.4.3. PWM CHANNEL 1 CONTROL REGISTER (DEFAULT: 0X00000000)

Offset:0x10			Register Name: PWM_CH1_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R	0x0	PWM1_RDY. PWM1 period register ready. 0: PWM1 period register is ready to write; 1: PWM1 period register is busy.
27:12	/	/	/
11:10	R/W	0x0	PWM1_PIN_STATUS. When PWM is disable, two output pins' status can be changed. 00: both low 01: pin 0 is high, pin 1 is low 10: pin 0 is low, pin 1 is high 11: both high
9	/	/	/
8	R/W	0x0	PWM_CH1_PUL_START. PWM Channel 1 pulse output start. 0: no effect, 1: output 1 pulse.

			The pulse width should be according to the period 1 register [15:0], and the pulse state should be according to the active state. After the pulse is finished, the bit will be cleared automatically.
7	R/W	0x0	PWM_CHANNEL1_MODE. 0: cycle mode, 1: pulse mode.
6	R/W	0x0	SCLK_CH1_GATING. Gating the Special Clock for PWM1 (0: mask, 1: pass).
5	R/W	0x0	PWM_CH1_ACT_STA. PWM Channel 1 Active State. 0: Low Level, 1: High Level.
4	R/W	0x0	PWM_CH1_EN. PWM Channel 1 Enable. 0: Disable, 1: Enable.
3:0	R/W	0x0	PWM_CH1_PRESCAL. PWM Channel 1 Prescalar. These bits should be setting before the PWM Channel 1 clock gate on. 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 others: /

3.11.4.4. PWM CHANNEL 1 PERIOD REGISTER

Offset:0x14	Register Name: PWM_CH1_PERIOD

Bit	Read/Write	Default/Hex	Description
31:16	R/W	x	PWM_CH1_ENTIRE_CYS Number of the entire cycles in the PWM clock. 0 = 1 cycle 1 = 2 cycles …… N = N+1 cycles If the register need to be modified dynamically, the PCLK should be faster than the PWM CLK (PWM CLK = 24MHz/prescale).
15:0	R/W	x	PWM_CH1_ENTIRE_ACT_CYS Number of the active cycles in the PWM clock. 0 = 0 cycle 1 = 1 cycles …… N = N cycles

Notes: When the active cycles are larger than the period cycles, the duty cycle is 100%

3.11.4.5. PWM CHANNEL 2 CONTROL REGISTER (DEFAULT: 0X00000000)

Offset:0x20			Register Name: PWM_CH2_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R	0x0	PWM2_RDY. PWM2 period register ready. 0: PWM2 period register is ready to write; 1: PWM2 period register is busy.
27:12	/	/	/
11:10	R/W	0x0	PWM2_PIN_STATUS. When PWM is disable, two output pins' status can be changed. 00: both low

			01: pin 0 is high, pin 1 is low 10: pin 0 is low, pin 1 is high 11: both high
9	/	/	/
8	R/W	0x0	PWM_CH2_PUL_START. PWM Channel 2 pulse output start. 0: no effect, 1: output 1 pulse. The pulse width should be according to the period 2 register [15:0], and the pulse state should be according to the active state. After the pulse is finished, the bit will be cleared automatically.
7	R/W	0x0	PWM_CHANNEL2_MODE. 0: cycle mode, 1: pulse mode.
6	R/W	0x0	SCLK_CH2_GATING. Gating the Special Clock for PWM 2 (0: mask, 1: pass).
5	R/W	0x0	PWM_CH2_ACT_STA. PWM Channel 2 Active State. 0: Low Level, 1: High Level.
4	R/W	0x0	PWM_CH2_EN. PWM Channel 2 Enable. 0: Disable, 1: Enable.
3:0	R/W	0x0	PWM_CH2_PRESCAL. PWM Channel 2 Prescalar. These bits should be setting before the PWM Channel 2 clock gate on. 0000: /1 0001: /2 0010: /4 0011: /8

			0100: /16 0101: /32 0110: /64 others: /

3.11.4.6. PWM CHANNEL 2 PERIOD REGISTER

Offset:0x24			Register Name: PWM_CH2_PERIOD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	x	PWM_CH2_ENTIRE_CYS Number of the entire cycles in the PWM clock. 0 = 1 cycle 1 = 2 cycles …… N = N+1 cycles If the register need to be modified dynamically, the PCLK should be faster than the PWM CLK (PWM CLK = 24MHz/prescale).
15:0	R/W	x	PWM_CH2_ENTIRE_ACT_CYS Number of the active cycles in the PWM clock. 0 = 0 cycle 1 = 1 cycles …… N = N cycles

Notes: When the active cycles are larger than the period cycles, the duty cycle is 100%.

3.11.4.7. PWM CHANNEL 3 CONTROL REGISTER (DEFAULT: 0X00000000)

Offset:0x30			Register Name: PWM_CH3_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R	0x0	PWM3_RDY.

			PWM3 period register ready. 0: PWM3 period register is ready to write; 1: PWM3 period register is busy.
27:12	/	/	/
11:10	R/W	0x0	PWM3_PIN_STATUS. When PWM is disable, two output pins' status can be changed. 00: both low 01: pin 0 is high, pin 1 is low 10: pin 0 is low, pin 1 is high 11: both high
9	/	/	/
8	R/W	0x0	PWM_CH3_PUL_START. PWM Channel 3 pulse output start. 0: no effect, 1: output 1 pulse. The pulse width should be according to the period 3 register [15:0], and the pulse state should be according to the active state. After the pulse is finished, the bit will be cleared automatically.
7	R/W	0x0	PWM_CHANNEL3_MODE. 0: cycle mode, 1: pulse mode.
6	R/W	0x0	SCLK_CH3_GATING. Gating the Special Clock for PWM 3 (0: mask, 1: pass).
5	R/W	0x0	PWM_CH3_ACT_STA. PWM Channel 3 Active State. 0: Low Level, 1: High Level.
4	R/W	0x0	PWM_CH3_EN. PWM Channel 3 Enable. 0: Disable, 1: Enable.
3:0	R/W	0x0	PWM_CH3_PRESCAL.

			PWM Channel 3 Prescalar. These bits should be setting before the PWM Channel 3 clock gate on. 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 others: /

3.11.4.8. PWM CHANNEL 3 PERIOD REGISTER

Offset:0x34			Register Name: PWM_CH3_PERIOD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	x	PWM_CH3_ENTIRE_CYS Number of the entire cycles in the PWM clock. 0 = 1 cycle 1 = 2 cycles …… N = N+1 cycles If the register need to be modified dynamically, the PCLK should be faster than the PWM CLK (PWM CLK = 24MHz/prescale).
15:0	R/W	x	PWM_CH3_ENTIRE_ACT_CYS Number of the active cycles in the PWM clock. 0 = 0 cycle 1 = 1 cycles …… N = N cycles

Notes: When the active cycles are larger than the period cycles, the duty cycle is 100%.

3.12. DMA

3.12.1. OVERVIEW

The chip supports 16 DMA channels, with each channel capable of generateing interrupts. Related DMA channel configuration is saved in DDR or SRAM.

3.12.2. DRQ TYPE AND PORT

Source DRQ Type		Destination DRQ Type	
port0	SRAM	port0	SRAM
port1	SDRAM	port1	SDRAM
port2	/	port2	/
port3	DAUDIO_0-RX	port3	DAUDIO_0-TX
port4	DAUDIO_1-RX	port4	DAUDIO_1-TX
port5	NAND0	port5	NAND0
port6	UART0-RX	port6	UART0-TX
port7	UART1-RX	port7	UART1-TX
port8	UART2-RX	port8	UART2-TX
port9	UART3-RX	port9	UART3-TX
port10	UART4-RX	port10	UART4-TX
port11		port11	TCON_0
port12		port12	TCON_1
port13	HDMI DDC	port13	HDMI DDC
port14	HDMI AUDIO	port14	HDMI AUDIO
port15	AUDIO CODEC	port15	AUDIO CODEC
port16	SS-RX	port16	SS-TX

port17	DRD_EP1	port17	DRD_EP1
port18	DRD_EP2	port18	DRD_EP2
port19	DRD_EP3	port19	DRD_EP3
port20	DRD_EP4	port20	DRD_EP4
port21	DRD_EP5	port21	DRD_EP5
port22	UART5-RX	port22	UART5-TX
port23	SPI_0-RX	port23	SPI_0-TX
port24	SPI_1-RX	port24	SPI_1-TX
port25	SPI_2-RX	port25	SPI_2-TX
port26	SPI_3-RX	port26	SPI_3-TX
port27	TP	port27	
port28	NAND1	port28	NAND1
port29	/	port29	/
Port30	DIGITAL MIC	Port30	DIGITAL MIC

3.12.3. DMA REGISTER LIST

Module Name	Base Address
DMA	0x01C02000

Register Name	Offset	Description
DMA_IRQ_EN_REG0	0x0	DMA IRQ Enable Register 0
DMA_IRQ_EN_REG1	0x4	DMA IRQ Enable Register 1
DMA_IRQ_PEND_REG0	0x10	DMA IRQ Pending Register 0
DMA_IRQ_PEND_REG1	0x14	DMA IRQ Pending Register 1
DMA_STA_REG	0x30	DMA Status Register
DMA_EN_REG	0x100+N*0x40	DMA Enable Register (N=0~15)
DMA_PAU_REG	0x100+N*0x40+0x4	DMA Pause Register(N=0~15)

DMA_STAR_ADDR_REG	0x100+N*0x40+0x8	DMA Start Address Register(N=0~15)
DMA_CFG_REG	0x100+N*0x40+0xC	DMA Configuration Register(N=0~15)
DMA_CUR_SRC_REG	0x100+N*0x40+0x10	DMA Current Source Register(N=0~15)
DMA_CUR_DEST_REG	0x100+N*0x40+0x14	DMA Current Destination Register(N=0~15)
DMA_BCNT_LEFT_REG	0x100+N*0x40+0x18	DMA Byte Counter Left Register(N=0~15)
DMA_PARA_REG	0x100+N*0x40+0x1C	DMA Parameter Register(N=0~15)

3.12.4. DMA REGISTER DESCRIPTION

3.12.4.1. DMA IRQ ENABLE REGISTER 0 (DEFAULT: 0X00000000)

Offset:0x0			Register Name: DMA_IRQ_EN_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	DMA7_QUEUE_IRQ_EN DMA 7 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable.
29	R/W	0x0	DMA7_PKG_IRQ_EN DMA 7 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable.
28	R/W	0x0	DMA7_HLAF_IRQ_EN DMA 7 Half Package Transfer Interrupt Enable. 0: Disable, 1: Enable.
27	/	/	/
26	R/W	0x0	DMA6_QUEUE_IRQ_EN DMA 6 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable.
25	R/W	0x0	DMA6_PKG_IRQ_EN DMA 6 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable.

24	R/W	0x0	DMA6_HLAF_IRQ_EN DMA 6 Half Package Transfer Interrupt Enable. 0: Disable, 1: Enable.
23	/	/	/
22	R/W	0x0	DMA5_QUEUE_IRQ_EN DMA 5 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable.
21	R/W	0x0	DMA5_PKG_IRQ_EN DMA 5 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable.
20	R/W	0x0	DMA5_HLAF_IRQ_EN DMA 5 Half package Transfer Interrupt Enable. 0: Disable, 1: Enable.
19	/	/	/
18	R/W	0x0	DMA4_QUEUE_IRQ_EN DMA 4 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable.
17	R/W	0x0	DMA4_PKG_IRQ_EN DMA 4 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable.
16	R/W	0x0	DMA4_HLAF_IRQ_EN DMA 4 Half Package Transfer Interrupt Enable. 0: Disable, 1: Enable.
15	/	/	/
14	R/W	0x0	DMA3_QUEUE_IRQ_EN DMA 3 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable.
13	R/W	0x0	DMA3_PKG_IRQ_EN DMA 3 Package End Transfer Interrupt Enable.

			0: Disable, 1: Enable.
12	R/W	0x0	DMA3_HLAF_IRQ_EN DMA 3 Half Package Transfer Interrupt Enable. 0: Disable, 1: Enable.
11	/	/	/
10	R/W	0x0	DMA2_QUEUE_IRQ_EN DMA 2 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable.
9	R/W	0x0	DMA2_PKG_IRQ_EN DMA 2 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable.
8	R/W	0x0	DMA2_HLAF_IRQ_EN DMA 2 Half Package Transfer Interrupt Enable. 0: Disable, 1: Enable.
7	/	/	/
6	R/W	0x0	DMA1_QUEUE_IRQ_EN DMA 1 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable.
5	R/W	0x0	DMA1_PKG_IRQ_EN DMA 1 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable.
4	R/W	0x0	DMA1_HLAF_IRQ_EN DMA 1 Half Package Transfer Interrupt Enable. 0: Disable, 1: Enable.
3	/	/	/
2	R/W	0x0	DMA0_QUEUE_IRQ_EN DMA 0 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable.
1	R/W	0x0	DMA0_PKG_IRQ_EN

			DMA 0 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable.
0	R/W	0x0	DMA0_HLAF_IRQ_EN DMA 0 Half Package Transfer Interrupt Enable. 0: Disable, 1: Enable

3.12.4.2. DMA IRQ ENABLE REGISTER 1 (DEFAULT: 0X00000000)

Offset:0x4			Register Name: DMA_IRQ_EN_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	DMA15_QUEUE_IRQ_EN DMA 15 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable.
29	R/W	0x0	DMA15_PKG_IRQ_EN DMA 15 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable.
28	R/W	0x0	DMA15_HLAF_IRQ_EN DMA 15 Half Package Transfer Interrupt Enable. 0: Disable, 1: Enable.
27	/	/	/
26	R/W	0x0	DMA14_QUEUE_IRQ_EN DMA 14 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable.
25	R/W	0x0	DMA14_PKG_IRQ_EN DMA 14 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable.
24	R/W	0x0	DMA14_HLAF_IRQ_EN DMA 14 Half Package Transfer Interrupt Enable. 0: Disable, 1: Enable.

23	/	/	/
22	R/W	0x0	DMA13_QUEUE_IRQ_EN DMA 13 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable.
21	R/W	0x0	DMA13_PKG_IRQ_EN DMA 13 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable.
20	R/W	0x0	DMA13_HLAF_IRQ_EN DMA 13 Half package Transfer Interrupt Enable. 0: Disable, 1: Enable.
19	/	/	/
18	R/W	0x0	DMA12_QUEUE_IRQ_EN DMA 12 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable.
17	R/W	0x0	DMA12_PKG_IRQ_EN DMA 12 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable.
16	R/W	0x0	DMA12_HLAF_IRQ_EN DMA 12 Half Package Transfer Interrupt Enable. 0: Disable, 1: Enable.
15	/	/	/
14	R/W	0x0	DMA11_QUEUE_IRQ_EN DMA 11 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable.
13	R/W	0x0	DMA11_PKG_IRQ_EN DMA 11 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable.
12	R/W	0x0	DMA11_HLAF_IRQ_EN DMA 11 Half Package Transfer Interrupt Enable.

			0: Disable, 1: Enable.
11	/	/	/
10	R/W	0x0	DMA10_QUEUE_IRQ_EN DMA 10 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable.
9	R/W	0x0	DMA10_PKG_IRQ_EN DMA 10 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable.
8	R/W	0x0	DMA10_HLAF_IRQ_EN DMA 10 Half Package Transfer Interrupt Enable. 0: Disable, 1: Enable.
7	/	/	/
6	R/W	0x0	DMA9_QUEUE_IRQ_EN DMA 9 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable.
5	R/W	0x0	DMA9_PKG_IRQ_EN DMA 9 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable.
4	R/W	0x0	DMA9_HLAF_IRQ_EN DMA 9 Half Package Transfer Interrupt Enable. 0: Disable, 1: Enable.
3	/	/	/
2	R/W	0x0	DMA8_QUEUE_IRQ_EN DMA 8 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable.
1	R/W	0x0	DMA8_PKG_IRQ_EN DMA 8 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable.
0	R/W	0x0	DMA8_HLAF_IRQ_EN

			DMA 8 Half Package Transfer Interrupt Enable. 0: Disable, 1: Enable

3.12.4.3. DMA IRQ PENDING STATUS REGISTER 0 (DEFAULT: 0X00000000)

Offset:0x10			Register Name: DMA_IRQ_PEND_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	DMA7_QUEUE_IRQ_PEND. DMA 7 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
29	R/W	0x0	DMA7_PKG_IRQ_ PEND DMA 7 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
28	R/W	0x0	DMA7_HLAF_IRQ_PEND. DMA 7 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
27	/	/	/
26	R/W	0x0	DMA6_QUEUE_IRQ_PEND. DMA 6 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
25	R/W	0x0	DMA6_PKG_IRQ_ PEND DMA 6 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
24	R/W	0x0	DMA6_HLAF_IRQ_PEND.

			DMA 6 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
23	/	/	/
22	R/W	0x0	DMA5_QUEUE_IRQ_PEND. DMA 5 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
21	R/W	0x0	DMA5_PKG_IRQ_ PEND DMA 5 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
20	R/W	0x0	DMA5_HLAF_IRQ_PEND. DMA 5 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
19	/	/	/
18	R/W	0x0	DMA4_QUEUE_IRQ_PEND. DMA 4 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
17	R/W	0x0	DMA4_PKG_IRQ_ PEND DMA 4 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
16	R/W	0x0	DMA4_HLAF_IRQ_PEND. DMA 4 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.

15	/	/	/
14	R/W	0x0	DMA3_QUEUE_IRQ_PEND. DMA 3 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
13	R/W	0x0	DMA3_PKG_IRQ_ PEND DMA 3 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
12	R/W	0x0	DMA3_HLAF_IRQ_PEND. DMA 3 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
11	/	/	/
10	R/W	0x0	DMA2_QUEUE_IRQ_PEND. DMA 2 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
9	R/W	0x0	DMA2_PKG_IRQ_ PEND DMA 2 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
8	R/W	0x0	DMA2_HLAF_IRQ_PEND. DMA 2 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
7	/	/	/
6	R/W	0x0	DMA1_QUEUE_IRQ_PEND. DMA 1 Queue End Transfer Interrupt Pending. Set 1 to the bit will

			clear it. 0: No effect, 1: Pending.
5	R/W	0x0	DMA1_PKG_IRQ_ PEND DMA 1 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
4	R/W	0x0	DMA1_HLAF_IRQ_PEND. DMA 1 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
3	/	/	/
2	R/W	0x0	DMA0_QUEUE_IRQ_PEND. DMA 0 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
1	R/W	0x0	DMA0_PKG_IRQ_ PEND DMA 0 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
0	R/W	0x0	DMA0_HLAF_IRQ_PEND. DMA 0 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.

3.12.4.4. DMA IRQ PENDING STATUS REGISTER 1 (DEFAULT: 0X00000000)

Offset:0x14			Register Name: DMA_IRQ_PEND_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	DMA15_QUEUE_IRQ_PEND.

			DMA 15 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
29	R/W	0x0	DMA15_PKG_IRQ_ PEND DMA 15 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
28	R/W	0x0	DMA15_HLAF_IRQ_PEND. DMA 15 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
27	/	/	/
26	R/W	0x0	DMA14_QUEUE_IRQ_PEND. DMA 14 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
25	R/W	0x0	DMA14_PKG_IRQ_ PEND DMA 14 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
24	R/W	0x0	DMA14_HLAF_IRQ_PEND. DMA 14 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
23	/	/	/
22	R/W	0x0	DMA13_QUEUE_IRQ_PEND. DMA 13 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.

21	R/W	0x0	DMA13_PKG_IRQ_ PEND DMA 13 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
20	R/W	0x0	DMA13_HLAF_IRQ_PEND. DMA 13 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
19	/	/	/
18	R/W	0x0	DMA12_QUEUE_IRQ_PEND. DMA 12 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
17	R/W	0x0	DMA12_PKG_IRQ_ PEND DMA 12 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
16	R/W	0x0	DMA12_HLAF_IRQ_PEND. DMA 12 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
15	/	/	/
14	R/W	0x0	DMA11_QUEUE_IRQ_PEND. DMA 11 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
13	R/W	0x0	DMA11_PKG_IRQ_ PEND DMA 11 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it.

			0: No effect, 1: Pending.
12	R/W	0x0	DMA11_HLAF_IRQ_PEND. DMA 11 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
11	/	/	/
10	R/W	0x0	DMA10_QUEUE_IRQ_PEND. DMA 10 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
9	R/W	0x0	DMA10_PKG_IRQ_ PEND DMA 10 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
8	R/W	0x0	DMA10_HLAF_IRQ_PEND. DMA 10 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
7	/	/	/
6	R/W	0x0	DMA9_QUEUE_IRQ_PEND. DMA 9 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
5	R/W	0x0	DMA9_PKG_IRQ_ PEND DMA 9 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
4	R/W	0x0	DMA9_HLAF_IRQ_PEND. DMA 9 Half Package Transfer Interrupt Pending. Set 1 to the bit will

			clear it. 0: No effect, 1: Pending.
3	/	/	/
2	R/W	0x0	DMA8_QUEUE_IRQ_PEND. DMA 8 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
1	R/W	0x0	DMA8_PKG_IRQ_ PEND DMA 8 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
0	R/W	0x0	DMA8_HLAF_IRQ_PEND. DMA 8 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.

3.12.4.5. DMA STATUS REGISTER (DEFAULT: 0X00000000)

Offset:0x30			Register Name: DMA_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	RO	0x0	DMA15_STATUS DMA Channel 15 Status. 0: Idle, 1: Busy.
14	RO	0x0	DMA14_STATUS DMA Channel 14 Status. 0: Idle, 1: Busy.
13	RO	0x0	DMA13_STATUS DMA Channel 13 Status. 0: Idle, 1: Busy.

12	RO	0x0	DMA12_STATUS DMA Channel 12 Status. 0: Idle, 1: Busy.
11	RO	0x0	DMA11_STATUS DMA Channel 11 Status. 0: Idle, 1: Busy.
10	RO	0x0	DMA10_STATUS DMA Channel 10 Status. 0: Idle, 1: Busy.
9	RO	0x0	DMA9_STATUS DMA Channel 9 Status. 0: Idle, 1: Busy.
8	RO	0x0	DMA8_STATUS DMA Channel 8 Status. 0: Idle, 1: Busy.
7	RO	0x0	DMA7_STATUS DMA Channel 7 Status. 0: Idle, 1: Busy.
6	RO	0x0	DMA6_STATUS DMA Channel 6 Status. 0: Idle, 1: Busy.
5	RO	0x0	DMA5_STATUS DMA Channel 5 Status. 0: Idle, 1: Busy.
4	RO	0x0	DMA4_STATUS DMA Channel 4 Status. 0: Idle, 1: Busy.
3	RO	0x0	DMA3_STATUS DMA Channel 3 Status.

			0: Idle, 1: Busy.
2	RO	0x0	DMA2_STATUS DMA Channel 2 Status. 0: Idle, 1: Busy.
1	RO	0x0	DMA1_STATUS DMA Channel 1 Status. 0: Idle, 1: Busy.
0	RO	0x0	DMA0_STATUS DMA Channel 0 Status. 0: Idle, 1: Busy.

3.12.4.6. DMA CHANNEL ENABLE REGISTER (DEFAULT: 0X00000000)

Offset:0x100+N*0x40+0x0 (N=0~15)			Register Name: DMA0_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	DMA_EN. DMA Channel Enable 0: Disable, 1: Enable.

3.12.4.7. DMA CHANNEL PAUSE REGISTER (DEFAULT: 0X00000000)

Offset:0x100+N*0x40+0x4 (N=0~15)			Register Name: DMA_PAU_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	DMA_PAUSE. Pausing DMA Channel Transfer Data. 0: Resume Transferring, 1: Pause Transferring.

3.12.4.8. DMA CHANNEL START ADDRESS REGISTER

Offset:0x100+N*0x40+0x8 (N=0~15)			Register Name: DMA_STAR_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	x	DMA_START_ADDR DMA Channel Start Address.

3.12.4.9. DMA CHANNEL CONFIGURATION REGISTER (DEFAULT: 0X00000000)

Offset:0x100+N*0x40+0xC (N=0~15)			Register Name: DMA_CFG_REG
Bit	**Read /Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:25	RO	0x0	DMA_DEST_DATA_WIDTH. DMA Destination Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: /
24:23	RO	0x0	DMA_DEST_BST_LEN. DMA Destination Burst Length. 00: 1 10: 8 11: /
22:21	RO	0x0	DMA_ADDR_MODE. DMA Destination Address Mode 0x0: Linear Mode 0x1: IO Mode 0x2: /

			0x3: /
20:16	RO	0x0	DMA_DEST_DRQ_TYPE. DMA Destination DRQ Type See *DRQ Type and Port* for details.
15:11	/	/	/
10:9	RO	0x0	DMA_SRC_DATA_WIDTH. DMA Source Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: /
8:7	RO	0x0	DMA_SRC_BST_LEN. DMA Source Burst Length. 00: 1 10: 8 11: /
6:5	RO	0x0	DMA_SRC_ADDR_MODE. DMA Source Address Mode 0x0: Linear Mode 0x1: IO Mode 0x2: / 0x3: /
4:0	RO	0x0	DMA_SRC_DRQ_TYPE. DMA Source DRQ Type See *DRQ Type and Port* for details.

Notes:

1) If the DRQ type is dram, then, the corresponding burst length will be fixed, and the options will be invalid.

2) The address of the *DMA Channel Configuration Register* must be word-aligned.

3.12.4.10. DMA CHANNEL CURRENT SOURCE ADDRESS REGISTER

Offset:0x100+N*0x40+0x10 (N=0~15)			Register Name: DMA_CUR_SRC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	RO	0x0	DMA_CUR_SRC. DMA Channel Current Source Address, read only.

Notes: The address of the *DMA Channel Current Source Address Register* must be word-aligned.

3.12.4.11. DMA CHANNEL CURRENT DESTINATION ADDRESS REGISTER

Offset:0x100+N*0x40+0x14 (N=0~15)			Register Name: DMA_CUR_DEST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	RO	0x0	DMA_CUR_DEST. DMA Channel Current Destination Address, read only.

Notes: The address of the *DMA Channel Current Destination Address Register* must be word-aligned.

3.12.4.12. DMA CHANNEL BYTE COUNTER LEFT REGISTER

Offset:0x100+N*0x40+0x18 (N=0~15)			Register Name: DMA_BCNT_LEFT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24:0	RO	0x0	DMA_BCNT_LEFT. DMA Channel Byte Counter Left, read only.

Notes: The address of the *DMA Channel Byte Counter Left Register* must be word-aligned.

3.12.4.13. DMA PARAMETER REGISTER

Offset:0x100+N*0x40+0x1C (N=0~15)			Register Name: DMA_PARA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:16	/	/	/
15:8	RO	0x0	DATA_BLK_SIZE. Data Block Size ***N***.
7:0	RO	0x0	WAIT_CYC. Wait Clock Cycles ***n***.

Notes:

1) The number of data block size usually depends on the capacity of the device's FIFO in the practical application.

2) The data block size must be multiple of ***burst*width*** (byte). For example: if burst is 4 and the width is 32-bit, so the data block size must be ***m*16***(byte), i.e. ***N = m * 16.***

3) When DMA controller has completed transferring ***N*** bytes data, and waiting ***n*** clock cycles to check the DRQ signal.

4) This register is only effective to devices, and the *Data Block Size* ***N*** should be **0** if it is less than **32**.

3.13. GIC

For details about GIC, please refer to the ***GIC PL400 technical reference manual*** and ***ARM GIC Architecture Specification V2.0.***

3.13.1. INTERRUPT SOURCE

Interrupt Source	SRC	Vector	Description
SGI 0	0	0x0000	SGI 0 interrupt
SGI 1	1	0x0004	SGI 1 interrupt
SGI 2	2	0x0008	SGI 2 interrupt
SGI 3	3	0x000C	SGI 3 interrupt
SGI 4	4	0x0010	SGI 4 interrupt
SGI 5	5	0x0014	SGI 5 interrupt
SGI 6	6	0x0018	SGI 6 interrupt
SGI 7	7	0x001C	SGI 7 interrupt
SGI 8	8	0x0020	SGI 8 interrupt
SGI 9	9	0x0024	SGI 9 interrupt
SGI 10	10	0x0028	SGI 10 interrupt
SGI 11	11	0x002C	SGI 11 interrupt
SGI 12	12	0x0030	SGI 12 interrupt
SGI 13	13	0x0034	SGI 13 interrupt
SGI 14	14	0x0038	SGI 14 interrupt
SGI 15	15	0x003C	SGI 15 interrupt
PPI 0	16	0x0040	PPI 0 interrupt
PPI 1	17	0x0044	PPI 1 interrupt
PPI 2	18	0x0048	PPI 2 interrupt

Interrupt Source	SRC	Vector	Description
PPI 3	19	0x004C	PPI 3 interrupt
PPI 4	20	0x0050	PPI 4 interrupt
PPI 5	21	0x0054	PPI 5 interrupt
PPI 6	22	0x0058	PPI 6 interrupt
PPI 7	23	0x005C	PPI 7 interrupt
PPI 8	24	0x0060	PPI 8 interrupt
PPI 9	25	0x0064	PPI 9 interrupt
PPI 10	26	0x0068	PPI 10 interrupt
PPI 11	27	0x006C	PPI 11 interrupt
PPI 12	28	0x0070	PPI 12 interrupt
PPI 13	29	0x0074	PPI 13 interrupt
PPI 14	30	0x0078	PPI 14 interrupt
PPI 15	31	0x007C	PPI 15 interrupt
UART 0	32	0x0080	UART 0 interrupt
UART 1	33	0x0084	UART 1 interrupt
UART 2	34	0x0088	UART 2 interrupt
UART 3	35	0x008C	UART 3 interrupt
UART 4	36	0x0090	UART 4 interrupt
UART 5	37	0x0094	UART 5 interrupt
TWI 0	38	0x0098	TWI 0 interrupt
TWI 1	39	0x009C	TWI 1 interrupt
TWI 2	40	0x00A0	TWI 2 interrupt
TWI 3	41	0x00A4	TWI 3 interrupt
/	42	0x00A8	/
PA_EINT	43	0x00AC	PA_EINT interrupt
/	44	0x00B0	/
DAUDIO-0	45	0x00B4	DAUDIO-0 interrupt

Interrupt Source	SRC	Vector	Description
DAUDIO-1	46	0x00B8	DAUDIO-1 interrupt
PB_EINT	47	0x00BC	PB_EINT interrupt
PE_EINT	48	0x00C0	PE_EINT interrupt
PG_EINT	49	0x00C4	PG_EINT interrupt
Timer 0	50	0x00C8	Timer 0 interrupt
Timer 1	51	0x00CC	Timer 1 interrupt
Timer 2	52	0x00D0	Timer 2 interrupt
Timer 3	53	0x00D4	Timer 3 interrupt
Timer 4	54	0x00D8	Timer 4 interrupt
Timer 5	55	0x00DC	Timer 5 interrupt
Watchdog 4	56	0x00E0	Watchdog 4 interrupt
Watchdog 1	57	0x00E4	Watchdog 1 interrupt
Watchdog 2	58	0x00E8	Watchdog 2 interrupt
Watchdog 3	59	0x00EC	Watchdog 3 interrupt
Touch Panel	60	0x00F0	Touch Panel interrupt
Audio Codec	61	0x00F4	Analogy Audio Codec interrupt
LRADC	62	0x00F8	LRADC interrupt
/	63	0x00FC	/
External NMI	64	0x100	External Non-Mask Interrupt
/	65	0x104	/
/	66	0x108	/
/	67	0x010C	/
/	68	0x0110	/
/	69	0x0114	/
/	70	0x0118	/
/	71	0x011C	/
/	72	0x0120	/

Interrupt Source	SRC	Vector	Description
/	73	0x0124	/
/	74	0x0128	/
/	75	0x012C	/
/	76	0x0130	/
/	77	0x0134	/
/	78	0x0138	/
/	79	0x013C	/
/	80	0x0140	/
/	81	0x0144	/
DMA	82	0x0148	DMA channel interrupt
HS Timer 0	83	0x014C	HS Timer 0 interrupt
HS Timer 1	84	0x0150	HS Timer 1 interrupt
HS Timer 2	85	0x0154	HS Timer 2 interrupt
HS Timer 3	86	0x0158	HS Timer 3 interrupt
/	87	0x015C	/
TZASC	88	0x0160	TZASC interrupt
/	89	0x0164	/
VE	90	0x0168	VE interrupt
DIG_MIC	91	0x016C	DIG_MIC interrupt
SD/MMC 0	92	0x0170	SD/MMC Host Controller 0 interrupt
SD/MMC 1	93	0x0174	SD/MMC Host Controller 1 interrupt
SD/MMC 2	94	0x0178	SD/MMC Host Controller 2 interrupt
SD/MMC 3	95	0x017C	SD/MMC Host Controller 3 interrupt
/	96	0x0180	/
SPI 0	97	0x0184	SPI 0 interrupt
SPI 1	98	0x0188	SPI 1 interrupt
SPI 2	99	0x018C	SPI 2 interrupt

Interrupt Source	SRC	Vector	Description
SPI 3	100	0x0190	SPI 3 interrupt
NAND1	101	0x0194	NAND1 Flash Controller interrupt
NAND0	102	0x0198	NAND0 Flash Controller interrupt
USB-DRD	103	0x019C	USB-DRD interrupt
USB-EHCI0	104	0x01A0	USB-EHCI0 interrupt
USB-OHCI0	105	0x01A4	USB-OHCI0 interrupt
USB-EHCI1	106	0x01A8	USB-EHCI1 interrupt
USB-OHCI1	107	0x01AC	USB-OHCI1 interrupt
/	108	0x01B0	/
USB-OHCI2	109	0x01B4	USB-OHCI2 interrupt
/	110	0x01B8	/
/	111	0x01BC	/
SS	112	0x01C0	Security System interrupt
TS	113	0x01C4	TS interrupt
EMAC	114	0x01C8	EMAC interrupt
MP	115	0x01CC	MP interrupt
CSI-0	116	0x01D0	CSI 0 interrupt
CSI-1	117	0x01D4	CSI 1 interrupt
LCD-0	118	0x01D8	LCD Controller interrupt
LCD-1	119	0x01DC	LCD Controller interrupt
HDMI	120	0x01E0	HDMI interrupt
MIPI DSI	121	0x01E4	MIPI DSI interrupt
MIPI CSI	122	0x01E8	MIPI CSI interrupt
DRC 0/1	123	0x01EC	DRC 0/1 interrupt
DEU 0/1	124	0x01F0	DEU 0/1 interrupt
DE_FE0	125	0x01F4	DE_FE0 interrupt
DE_FE1	126	0x01F8	DE_FE1 interrupt

Interrupt Source	SRC	Vector	Description
DE_BE0	127	0x01FC	DE_BE0 interrupt
DE_BE1	128	0x0200	DE_BE1 interrupt
GPU	129	0x0204	GPU interrupt
/	130	0x0208	/
/	131	0x020C	/
/	132	0x0210	/
/	133	0x0214	/
/	134	0x0218	/
/	135	0x021C	/
/	136	0x0220	/
/	137	0x0224	/
/	138	0x0228	/
/	139	0x022C	/
CTI0	140	0x0230	CTI0 interrupt
CTI1	141	0x0234	CTI1 interrupt
CTI2	142	0x0238	CTI2 interrupt
CTI3	143	0x023C	CTI3 interrupt
COMMTX0	144	0x0240	COMMTX0 interrupt
COMMTX1	145	0x0244	COMMTX1 interrupt
COMMTX2	146	0x0248	COMMTX2 interrupt
COMMTX3	147	0x024C	COMMTX3 interrupt
COMMRX0	148	0x0250	COMMRX0 interrupt
COMMRX1	149	0x0254	COMMRX1 interrupt
COMMRX2	150	0x0258	COMMRX2 interrupt
COMMRX3	151	0x025C	COMMRX3 interrupt
PMU0	152	0x0260	PMU0 interrupt
PMU1	153	0x0264	PMU1 interrupt

Interrupt Source	SRC	Vector	Description
PMU2	154	0x0268	PMU2 interrupt
PMU3	155	0x026C	PMU3 interrupt
AXI_ERROR	156	0x0270	AXI_ERROR interrupt

3.14. RTC

3.14.1. OVERVIEW

The Real Time Clock (RTC) is for calendar usage. It is built around a 30-bit counter and used to count elapsed time in YY-MM-DD and HH-MM-SS. The unit can operate using the backup battery while the system power is off. Besides, it features a built-in leap year generator and an independent power pin (RTC_VIO).

The alarm can generate an alarm signal at a specific time in normal operation mode as well as power-off mode. In normal operation mode, both the alarm interrupt and the power management wakeup are activated, while in power-off mode, only power management wakeup signal is activated. There are two kinds of alarm supported. Alarm 0 is a general alarm, whose counter is based on second, and Alarm 1 is a weekly alarm, whose counter is based on the real time.

The 32768Hz oscillator is used only to provide a low power, accurate reference for the RTC.
The General Purpose Registers can be flag registers, and they can save the values when VDD_RTC is powered on.

3.14.2. RTC REGISTER LIST

Module Name	Base Address
RTC	0x01F00000

Register Name	Offset	Description
LOSC_CTRL_REG	0x0	Low Oscillator Control Register l
LOSC_AUTO_SWT_STA_REG	0x4	LOSC Auto Switch Status Register
INTOSC_CLK_PRESCAL_REG	0x8	Internal OSC Clock Prescalar Register

RTC_YY_MM_DD_REG	0x10	RTC Year-Month-Day Register
RTC_HH_MM_SS_REG	0x14	RTC Hour-Minute-Second Register
ALARM0_COUNTER_REG	0x20	Alarm 0 Counter Register
ALARM0_CUR_VLU_REG	0x24	Alarm 0 Counter Current Value Register
ALARM0_ENABLE_REG	0x28	Alarm 0 Enable Register
ALARM0_IRQ_EN	0x2C	Alarm 0 IRQ Enable Register
ALARM0_IRQ_STA_REG	0x30	Alarm 0 IRQ Status Register
ALARM1_WK_HH_MM-SS	0x40	Alarm 1 Week HMS Register
ALARM1_ENABLE_REG	0x44	Alarm 1 Enable Register
ALARM1_IRQ_EN	0x48	Alarm 1 IRQ Enable Register
ALARM1_IRQ_STA_REG	0x4C	Alarm 1 IRQ Status Register
ALARM_CONFIG_REG	0x50	Alarm Config Register
GP_DATA_REG	0x100 + N*0x4	General Purpose Register (N=0~15)
GPL_HOLD_OUTPUT_REG	0x180	GPL Hold Output Register
GPM_HOLD_OUTPUT_REG	0x184	GPM Hold Output Register
VDD_RTC_REG	0x190	VDD RTC Regulate Register

3.14.3. RTC REGISTER DESCRIPTION

3.14.3.1. LOSC CONTROL (DEFAULT: 0X00004000)

Offset:0x0			Register Name: LOSC_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14	R/W	0x1	LOSC_AUTO_SWT_EN. LOSC auto switch enable. 0: Disable, 1: Enable.
13:10	/	/	/
9	R/W	0x0	ALM_DDHHMMSS_ACCE.

			ALARM DD-HH-MM-SS access. After writing the ALARM DD-HH-MM-SS register, this bit is set and it will be cleared until the real writing operation is finished.
8	R/W	0x0	RTC_HHMMSS_ACCE. RTC HH-MM-SS access. After writing the RTC HH-MM-SS register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC YY-MM-DD register, the YY-MM-DD register will be refreshed for at most one second.
7	R/W	0x0	RTC_YYMMDD_ACCE. RTC YY-MM-DD access. After writing the RTC YY-MM-DD register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC YY-MM-DD register, the YY-MM-DD register will be refreshed for at most one second.
6:4	/	/	/
3:2	R/W	0x0	EXT_LOSC_GSM. External 32768Hz Crystal GSM. 00 low 01 10 11 high
1	/	/	/
0	R/W	0x0	LOSC_SRC_SEL. LOSC Clock source Select. ‘N’ is the value of Internal OSC Clock Prescalar register. 0: InternalOSC / N, 1: External 32.768KHz OSC.

Notes:

1) Any bit of [9:7] is set, the RTC HH-MM-SS, YY-MM-DD and ALARM DD-HH-MM-SS register can’t be

written.

2) Internal OSC is about 600 KHz ~700 KHz.

3.14.3.2. LOSC AUTO SWITCH STATUS REGISTER (DEFAULT: 0X00000000)

Offset:0x4			Register Name: LOSC_AUTO_SWT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	LOSC_AUTO_SWT_PEND. LOSC auto switch pending. 0: no effect; 1: auto switches pending. Set 1 to this bit will clear it.
0	RO	0x0	LOSC_SRC_SEL_STA. Checking LOSC Clock Source Status. 'N' is the value of Internal OSC Clock Prescalar register. 0: InternalOSC / N; 1: External 32.768KHz OSC.

3.14.3.3. INTERNAL OSC CLOCK PRESCALAR REGISTER (DEFAULT: 0X00000014)

Offset:0x8			Register Name: INTOSC_CLK_PRESCAL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4:0	R/W	0x14	INTOSC_CLK_PRESCAL. Internal OSC Clock Prescalar value N. 00000: 1 00001: 2 00010: 3 ..... 11111: 32

3.14.3.4. RTC YY-MM-DD REGISTER (DEFAULT: 0X00000000)

Offset:0x10			Register Name: RTC_YY_MM_DD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22	R/W	0x0	LEAP. Leap Year. 0: not, 1: Leap year. This bit can not set by hardware. It should be set or clear by software.
21:16	R/W	x	YEAR. Year. Range from 0~63.
15:12	/	/	/
11:8	R/W	x	MONTH. Month. Range from 1~12.
7:5	/	/	/
4:0	R/W	x	DAY. Day. Range from 1~31.

Notes:

1) If the written value is not from 1 to 31 in Day Area, it turns into 31 automatically. Month Area and Year Area are similar to Day Area.

2) The number of days in different month may be different.

3.14.3.5. RTC HH-MM-SS REGISTER (DEFAULT: 0X00000000)

Offset:0x14	Register Name: RTC_HH_MM_SS_REG

Bit	Read/Write	Default/Hex	Description
31:29	R/W	0x0	WK_NO. Week number. 000: Monday 001: Tuesday 010: Wednesday 011: Thursday 100: Friday 101: Saturday 110: Sunday 111: /
28:21	/	/	/
20:16	R/W	x	HOUR. Range from 0~23
15:14	/	/	/
13:8	R/W	x	MINUTE. Range from 0~59
7:6	/	/	/
5:0	R/W	x	SECOND. Range from 0~59

Notes: If the written value is not from 0 to 59 in Second Area, it turns into 59 automatically. Minute Area and Hour Area are similar to Second Area.

3.14.3.6. ALARM 0 COUNTER REGISTER (DEFAULT: 0X00000000)

Offset:0x20			Register Name: ALARM0_COUNTER_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	ALARM0_COUNTER. Alarm 0 Counter is Based on Second.

Notes: If the second is set to 0, it will be 1 second in fact.

3.14.3.7. ALARM 0 CURRENT VALUE REGISTER

Offset:0x24			Register Name: ALARM0_CUR_VLU_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	RO	x	ALARM0_CUR_VLU. Check Alarm 0 Counter Current Values.

Notes: If the second is set to 0, it will be 1 second in fact.

3.14.3.8. ALARM 0 ENABLE REGISTER (DEFAULT: 0X00000000)

Offset:0x28			Register Name: ALARM0_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALM_0_EN Alarm 0 Enable. If this bit is set to “1”, the Alarm 0 Counter register’s valid bits will down count to zero, and the alarm pending bit will be set to “1”. 0: disable, 1: enable.

3.14.3.9. ALARM 0 IRQ ENABLE REGISTER (DEFAULT: 0X00000000)

Offset:0x2C			Register Name: ALARM0_IRQ_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALARM0_IRQ_EN. Alarm 0 IRQ Enable. 0: disable; 1: enable.

3.14.3.10. ALARM 0 IRQ STATUS REGISTER (DEFAULT: 0X00000000)

Offset:0x30			Register Name: ALARM0_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALARM0_IRQ_PEND. Alarm 0 IRQ Pending bit. 0: No effect; 1: Pending, alarm 0 counter value is reached. If alarm 0 irq enable is set to 1, the pending bit will be sent to the interrupt controller.

3.14.3.11. ALARM 1 WEEK HH-MM-SS REGISTER (DEFAULT: 0X00000000)

Offset:0x40			Register Name: ALARM1_WK_HH_MM-SS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	x	HOUR. Range from 0~23.
15:14	/	/	/
13:8	R/W	x	MINUTE. Range from 0~59.
7:6	/	/	/.
5:0	R/W	x	SECOND. Range from 0~59.

Notes: If the written value is not from 0 to 59 in Second Area, it turns into 59 automatically. Minute Area and Hour Area are similar to Second Area.

3.14.3.12. ALARM 1 ENABLE REGISTER (DEFAULT: 0X00000000)

Offset:0x44			Register Name: ALARM1_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:7	/	/	/
6	R/W	0x0	WK6_ALM1_EN. Week 6 (Sunday) Alarm 1 Enable. 0: Disable; 1: Enable. If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS register valid bits equals to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 6, the week 6 alarm irq pending bit will be set to “1”.
5	R/W	0x0	WK5_ALM1_EN. Week 5 (Saturday) Alarm 1 Enable. 0: Disable; 1: Enable. If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS register valid bits equals to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 5, the week 5 alarm irq pending bit will be set to “1”.
4	R/W	0x0	WK4_ALM1_EN. Week 4 (Friday) Alarm 1 Enable. 0: Disable, 1: Enable. If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS register valid bits equals to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 4, the week 4 alarm irq pending bit will be set to “1”.
3	R/W	0x0	WK3_ALM1_EN. Week 3 (Thursday) Alarm 1 Enable. 0: Disable; 1: Enable. If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS

			register valid bits equals to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 3, the week 3 alarm irq pending bit will be set to “1”.
2	R/W	0x0	WK2_ALM1_EN. Week 2 (Wednesday) Alarm 1 Enable. 0: Disable; 1: Enable. If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS register valid bits equals to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 2, the week 2 alarm irq pending bit will be set to “1”.
1	R/W	0x0	WK1_ALM1_EN. Week 1 (Tuesday) Alarm 1 Enable. 0: Disable; 1: Enable. If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS register valid bits equals to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 1, the week 1 alarm irq pending bit will be set to “1”.
0	R/W	0x0	WK0_ALM1_EN. Week 0 (Monday) Alarm 1 Enable. 0: Disable; 1: Enable. If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS register valid bits equals to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 0, the week 0 alarm irq pending bit will be set to “1”.

3.14.3.13. ALARM 1 IRQ ENABLE REGISTER (DEFAULT: 0X00000000)

Offset:0x48			Register Name: ALARM1_IRQ_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALARM1_IRQ_EN. Alarm 1 IRQ Enable. 0: disable; 1: enable.

3.14.3.14. ALARM 1 IRQ STATUS REGISTER (DEFAULT: 0X00000000)

Offset:0x4C			Register Name: ALARM1_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALARM1_WEEK_IRQ_PEND. Alarm 1 Week (0/1/2/3/4/5/6) IRQ Pending. 0: No effect; 1: Pending, week counter value is reached. If alarm 1 week irq enable is set to 1, the pending bit will be sent to the interrupt controller.

3.14.3.15. ALARM CONFIG REGISTER (DEFAULT: 0X00000000)

Offset:0x50			Register Name: ALARM_CONFIG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALARM_WAKEUP. Configuration of alarm wake up output. 0: disable alarm wake up output; 1: enable alarm wake up output.

3.14.3.16. GENERAL PURPOSE REGISTER (DEFAULT: 0X00000000))

Offset:0x100+N *0x4 (N=0~15)			Register Name: GP_DATA_REGn
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	GP_DATA. Data [31:0].

Notes: General purpose register 0/1/2/…./15 value can be stored when VDD_RTC is larger than 1.0v.

3.14.3.17. GPL HOLD OUTPUT REGISTER (DEFAULT: 0X00000000)

Offset:0x180			Register Name: GPL_HOLD_OUTPUT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	GPL8_HOLD_OUTPUT. Hold the output of GPIOL8 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
7	R/W	0x0	GPL7_HOLD_OUTPUT. Hold the output of GPIOL7 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
6	R/W	0x0	GPL6_HOLD_OUTPUT. Hold the output of GPIOL6 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable

			1: Hold enable
5	R/W	0x0	GPL5_HOLD_OUTPUT. Hold the output of GPIOL5 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
4	R/W	0x0	GPL4_HOLD_OUTPUT. Hold the output of GPIOL4 when system's power is changing. The outputs must be low level (0) or high level (1) or High-Z; any other output may not hold on. 0: Hold disable 1: Hold enable
3	R/W	0x0	GPL3_HOLD_OUTPUT. Hold the output of GPIOL3 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
2	R/W	0x0	GPL2_HOLD_OUTPUT. Hold the output of GPIOL2 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
1:0	/	/	/

3.14.3.18. GPM HOLD OUTPUT REGISTER (DEFAULT: 0X00000000)

Offset:0x184	Register Name: GPM_HOLD_OUTPUT_REG

Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	GPM7_HOLD_OUTPUT. Hold the output of GPIOM7 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
6	R/W	0x0	GPM6_HOLD_OUTPUT. Hold the output of GPIOM6 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
5	R/W	0x0	GPM5_HOLD_OUTPUT. Hold the output of GPIOM5 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
4	R/W	0x0	GPM4_HOLD_OUTPUT. Hold the output of GPIOM4 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
3	R/W	0x0	GPM3_HOLD_OUTPUT. Hold the output of GPIOM3 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other

			outputs may not hold on. 0: Hold disable 1: Hold enable
2	R/W	0x0	GPM2_HOLD_OUTPUT. Hold the output of GPIOM2 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
1	R/W	0x0	GPM1_HOLD_OUTPUT. Hold the output of GPIOM1 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
0	R/W	0x0	GPM0_HOLD_OUTPUT. Hold the output of GPIOM0 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable

3.14.3.19. VDD RTC REGULATION REGISTER (DEFAULT: 0X00000004)

Offset:0x190			Register Name: VDD_RTC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x100	VDD_RTC_REGU. These bits are useful for regulating the RTC_VIO from 0.7v to 1.4v, and the regulation step is 0.1v.

			000: 0.7v 001: 0.8v 010: 0.9v 011: 1.0v 100: 1.1v 101: 1.2v 110: 1.3v 111: 1.4v

3.15. SECURITY SYSTEM

3.15.1. OVERVIEW

The Security System (SS) is one encrypt/ decrypt function accelerator that is suitable for a variety of applications. Several modes are supported. Both CPU mode and DMA method are supported for different applications.

It features:

- AES, DES, 3DES, SHA-1, MD5 are supported by this system
- ECB, CBC modes for AES/DES/3DES
- 128-bits, 192-bits and 256-bits key size for AES
- 160-bits hardware PRNG with 192-bits seed
- 32-words RX FIFO and 32-words TX FIFO for high speed application
- CPU mode and DMA mode are supported
- Interrupt supported

3.15.2. SECURITY SYSTEM BLOCK DIAGRAM

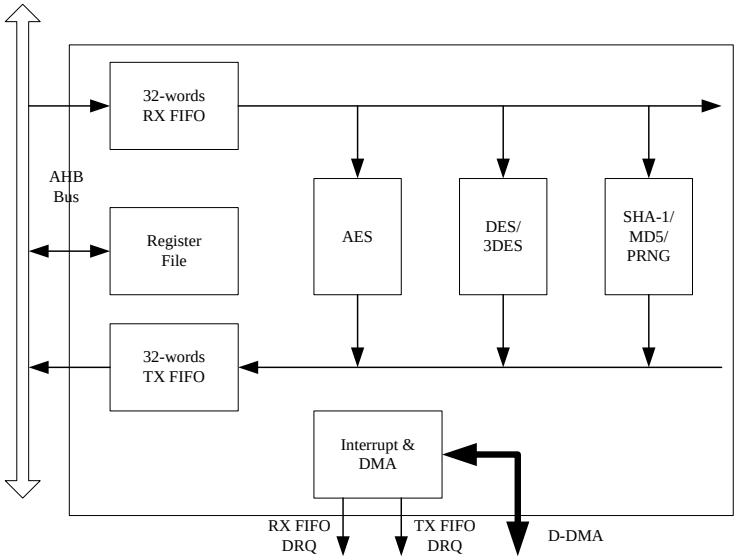


Figure 3-6 Security System Block Diagram

3.15.3. SECURITY SYSTEM REGISTER LIST

Module Name	Base Address
SS	0x01C15000

Register Name	Offset	Description
SS_CTL	0x00	Security Control Register
SS_KEY0	0x04	Security Input Key 0/ PRNG Seed 0
SS_KEY1	0x08	Security Input Key 1/ PRNG Seed 1
…	…	…
SS_KEY7	0x20	Security Input Key 7
SS_IV0	0x24	Security Initialization Vector 0
SS_IV1	0x28	Security Initialization Vector 1
SS_IV2	0x2C	Security Initialization Vector 2
SS_IV3	0x30	Security Initialization Vector 3

SS_CNT0	0x34	Security Preload Counter 0
SS_CNT1	0x38	Security Preload Counter 1
SS_CNT2	0x3C	Security Preload Counter 2
SS_CNT3	0x40	Security Preload Counter 3
SS_FCSR	0x44	Security FIFO Control/ Status Register
SS_ICSR	0x48	Security Interrupt Control/ Status Register
SS_MD0	0x4C	SHA1/MD5 Message Digest 0/PRNG Data0
SS_MD1	0x50	SHA1/MD5 Message Digest 1/PRNG Data1
SS_MD2	0x54	SHA1/MD5 Message Digest 2/PRNG Data2
SS_MD3	0x58	SHA1/MD5 Message Digest 3/PRNG Data3
SS_MD4	0x5C	SHA1/MD5 Message Digest 4/PRNG Data4
SS_RXFIFO	0x200	RX FIFO input port
SS_TXFIFO	0x204	TX FIFO output port

3.15.4. SECURITY SYSTEM REGISTER DESCRIPTION

3.15.4.1. SECURITY SYSTEM CONTROL REGISTER

Offset: 0x00			**Register Name: SS_CTL** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:28	/	/	/
27:24	R/W	0	SKEY_SELECT AES/DES/3DES key select 0: Select input SS_KEYx (Normal Mode) 1: Select SID_RKEYx from Security ID 2: Select SID_BKEYx from Security ID 3-10: Select internal Key n (n from 0 to 7) Others: Reserved

18:16	R	x	DIE_ID Die Bonding ID
15	R/W	0	PRNG_MODE PRNG generator mode 0: One-shot mode 1: Continue mode
14	R/W	0	IV_MODE IV Steady of SHA-1/MD5 constants 0: Constants 1: Arbitrary IV Notes: It is only used for SHA-1/MD5 engine. If the number of IV word is beyond of 4, Counter 0 register is used for IV4.
13:12	R/W	0	SS_OP_MODE SS Operation Mode 00: Electronic Code Book (ECB) mode 01: Cipher Block Chaining (CBC) mode 1X: Reserved
11:10	/	/	/
9:8	R/W	0	AES_KEY_SIZE Key Size for AES 00: 128-bits 01: 192-bits 10: 256-bits 11: Reserved
7	R/W	0	SS_OP_DIR SS Operation Direction 0: Encryption 1: Decryption
6:4	R/W	0	SS_METHOD

			SS Method 000: AES 001: DES 010: Triple DES (3DES) 011: SHA-1 100: MD5 101: PRNG Others: Reserved
3	/	/	/
2	R/W	0	SHA1_MD5_END_BIT SHA-1/MD5 Data End bit Write '1' to tell SHA-1/MD5 engine that the text data is end. If there is some data in FIFO, the engine would fetch these data and process them. After finishing message digest, this bit is clear to '0' by hardware and message digest can be read out from digest registers. Notes: It is only used for SHA-1/MD5 engine.
1	R/W	0	PRNG_START PRNG start bit In PRNG one-shot mode, write '1' to start PRNG. After generating one group random data (5 words), this bit is clear to '0' by hardware.
0	R/W	0	SS_ENABLE SS Enable A disable on this bit overrides any other block and flushes all FIFOs. 0: Disable 1: Enable

3.15.4.2. SECURITY SYSTEM KEY [N] REGISTER

Offset: 0x04 +4*n	**Register Name: SS_KEY[n]** **Default Value: 0x0000_0000**

Bit	Read/Write	Default	Description
31:0	R/W	0	SS_KEY Key[n] Input Value (n= 0~7)/ PRNG Seed[n] (n= 0~5)

3.15.4.3. SECURITY SYSTEM IV[N] REGISTER

Offset: 0x24 +4*n			Register Name: SS_IV[n] Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0	SS_IV_VALUE Initialization Vector (IV[n]) Input Value (n= 0~3)

3.15.4.4. SECURITY SYSTEM COUNTER[N] REGISTER

Offset: 0x34 +4*n			Register Name: SS_CNT[n] Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0	SS_CNT_VALUE Preload Counter Input Value (n= 0~3)

3.15.4.5. SECURITY SYSTEM FIFO CONTROL/ STATUS REGISTER

Offset: 0x44			Register Name: SS_FCSR Default Value: 0x6000_0F0F
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30	R	0x1	RXFIFO_STATUS RX FIFO Empty 0: No room for new word in RX FIFO 1: More than one room for new word in RX FIFO (>= 1 word)
29:24	R	0x20	RXFIFO_EMP_CNT RX FIFO Empty Space Word Counter

23	/	/	/
22	R	0	TXFIFO_STATUS TX FIFO Data Available Flag 0: No available data in TX FIFO 1: More than one data in TX FIFO (>= 1 word)
21:16	R	0	TXFIFO_AVA_CNT TX FIFO Available Word Counter
15:13	/	/	/
12:8	R/W	0xF	RXFIFO_INT_TRIG_LEVEL RX FIFO Empty Trigger Level Interrupt and DMA request trigger level for RXFIFO normal condition Trigger Level = RXTL + 1 Notes: RX FIFO is used for input the data.
7:5	/	/	/
4:0	R/W	0xF	TXFIFO_INT_TRIG_LEVEL TX FIFO Trigger Level Interrupt and DMA request trigger level for TXFIFO normal condition Trigger Level = TXTL + 1 Notes: TX FIFO is used for output the result data.

3.15.4.6. SECURITY SYSTEM INTERRUPT CONTROL/ STATUS REGISTER

Offset: 0x48			**Register Name: SS_ICSR** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:11	/	/	/
10	R/W	0	RXFIFO_EMP_PENDING_BIT RX FIFO Empty Pending bit 0: No pending 1: RX FIFO Empty pending

			Notes: Write ‘1’ to clear or automatic clear if interrupt condition fails.
9	/	/	/
8	R/W	0	TXFIFO_AVA_PENDING_BIT TX FIFO Data Available Pending bit 0: No TX FIFO pending 1: TX FIFO pending Notes: Write ‘1’ to clear or automatic clear if interrupt condition fails.
7:5	/	/	/
4	R/W	0	DRA_ENABLE DRQ Enable 0: Disable DRQ (CPU polling mode) 1: Enable DRQ (DMA mode)
3	/	/	/
2	R/W	0	RXFIFO_EMP_INT_ENABLE RX FIFO Empty Interrupt Enable 0: Disable 1: Enable Notes: If it is set to ‘1’, when the number of empty room is great or equal (>=) the preset threshold, the interrupt is trigger and the correspond flag is set.
1	/	/	/
0	R/W	0	TXFIFO_AVA_INT_ENABLE TX FIFO Data Available Interrupt Enable 0: Disable 1: Enable Notes: If it is set to ‘1’, when available data number is great or equal (>=) the preset threshold, the interrupt is trigger and the correspond flag is set.

3.15.4.7. SECURITY SYSTEM MESSAGE DIGEST[N] REGISTER

Offset: 0x4C +4*n			Register Name: SS_MD[n] Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R	0	SS_MID_DATA SHA1/ MD5 Message digest MD[n] for SHA1/MD5 (n= 0~4)

3.15.4.8. SECURITY SYSTEM RX FIFO REGISTER

Offset: 0x200			Register Name: SS_RX Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	W	0	SS_RX_FIFO 32-bits RX FIFO for Input

3.15.4.9. SECURITY SYSTEM TX FIFO REGISTER

Offset: 0x204			Register Name: SS_TX Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R	0	SS_TX_FIFO 32-bits TX FIFO for Output

3.15.5. SECURITY SYSTEM CLOCK REQUIREMENT

Clock Name	Description	Requirement
ahb_clk	AHB bus clock	>=24MHz
ss_clk	SS serial clock	<= 150MHz

3.15.6. SECURITY SYSTEM PROGRAMMING GUIDE

For SHA1,It should be noted the sequence of the message digest.

Let the message,24-bit ASCII string “abc”,the resulting 160-bit message digest for Fips180-2 is :

a9993e36 4706816a ba3e2571 7850c26c 9cd0d89d

For SHA1 of the Allwinner:

Let the message,24-bit ASCII string “abc”,the read message digest result from SS_MD[n](n=0~4) register,in Hex:

SS_MD[0] = a9993e36

SS_MD[1] = 4706816a

SS_MD[2] = ba3e2571

SS_MD[3] = 7850c26c

SS_MD[4] = 9cd0d89d

It is worth nothing that SHA1 is a big-endian algorithm, the most significant bit is stored in the left-most bit position. But the default access mode of ARM is litter-endian ,so every word of SS_MD[n](n=0~4) register need convert the byte sequence by the software.

3.16. GPADC

3.16.1. OVERVIEW

The general purpose ADC unit is used to monitor the voltage status of the peripheral in many application such as temperature measurement ， light sensor and power detection. There are 4 input pins allowing up to 4 channel analog input to be sampled simultaneously.

It features:

- 12-bit resolution
- Maximum conversion rate: 1 msps
- Low power consumption
- Power supply voltage: 3 v
- Analog input range: 0 to 3 v
- On-chip sample-and-hold function
- Single or mutiple input channel select mode
- Median and averaging filter to reduce noise

3.16.2. BLOCK DIAGRAM

The embedded SAR ADC block diagram is shown below:

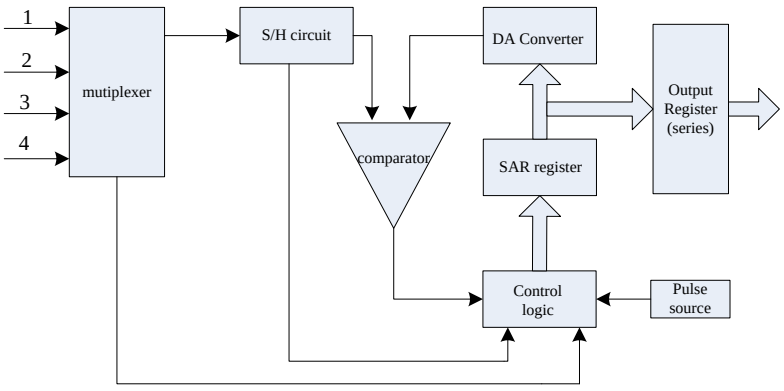


Figure 3-7 GPADC Typical Functional Block Diagram

3.16.3. CLOCK TREE AND CONVERISON TIME

3.16.3.1. CLOCK TREE

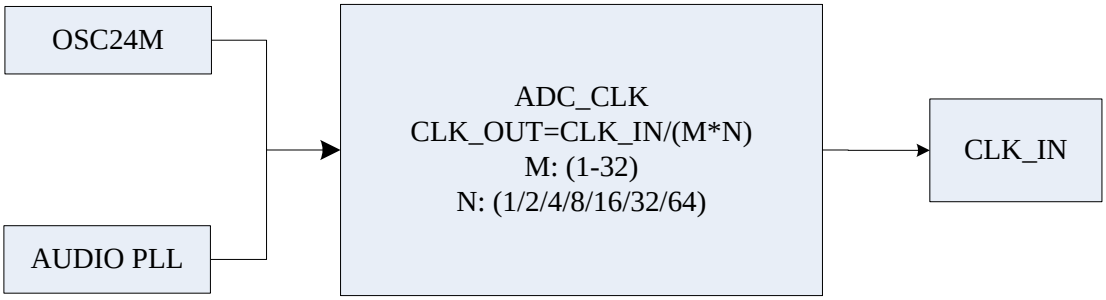


Figure 3-8 ADC Clock Tree

3.16.3.2. A/D CONVERSION TIME

When the clock source is 24MHz and the prescaler value M*N is 6, total 12-bit conversion time is as follows.

CLK_IN = 24MHz/6 = 4MHz

Conversion Time = 1/(4MHz/14Cycles) =3.50us

If ADC acquire time divider is 5, then TACQ =1/(4MHz/6) = 1.50us

FS_TIME (configured by the FS_DIV register) bases on the summation of Conversion Time and TACQ. The FS_TIME must be greater or equal than (TACQ + Conversion Time)

FS_TIME >= TACQ + Conversion Time=5.0us

This A/D converter was designed to operate at maximum 24MHz clock, and the conversion rate can go up to 1 MSPS.

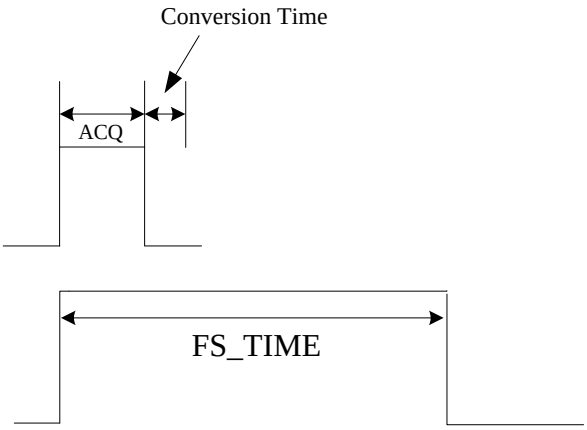


Figure 3-9 ADC Conversion phase

3.16.4. GPADC REGISTER LIST

Module Name	Base Address
GPADC	0x01C25000

Register Name	Offset	Description
GPADC_CTRL0	0x00	GPADC Control Register0
GPADC_CTRL1	0x04	GPADC Control Register1
GPADC_CTRL2	0x0c	Median and Averaging Filter Controller Register
GPADC_INT_FIFOC	0x10	GPADC Interrupt FIFO Control Register
GPADC_INT_FIFOS	0x14	GPADC Interrupt FIFO Status Register
GPADC_DATA	0x24	GPADC Data Register
GPADC_IO_CONFIG	0x28	GPADC IO Configuration
GPADC_PORT_DATA	0x2c	GPADC IO Port Data

3.16.5. GPADC REGISTER DESCRIPTION

3.16.5.1. GPADC CONTROL REGISTER 0

Offset: 0x00			Register Name: GPADC_CTRL0
Bit	Read/ Write	Default /Hex	Description
31:24	R/W	0xF	ADC_FIRST_DLY. ADC First Convert Delay Time(T_FCDT)setting Based on ADC First Convert Delay Mode select (Bit 23) T_FCDT = ADC_FIRST_DLY * ADC_FIRST_DLY_MODE
23	R/W	0x1	ADC_FIRST_DLY_MODE. ADC First Convert Delay Mode Select 0: CLK_IN/16 1: CLK_IN/16*256

22	R/W	0x0	ADC_CLK_SELECT. ADC Clock Source Select: 0: HOSC(24MHZ) 1: Audio PLL
21:20	R/W	0x0	ADC_CLK_DIVIDER. ADC Clock Divider(CLK_IN) 00: CLK/2 01: CLK/3 10: CLK/6 11: CLK/1
19:16	R/W	0x0	FS_DIV. ADC Sample Frequency Divider 0000: CLK_IN/$2^{(20-n)}$ 0001: CLK_IN/$2^{(20-n)}$ 0010: CLK_IN/$2^{(20-n)}$ …. 1111: CLK_IN/32
15:0	R/W	0x0	TACQ. GPADC acquire time CLK_IN/(16*(N+1))

3.16.5.2. GPADC CONTROL REGISTER 1

Offset: 0x04			**Register Name: GPADC_CTRL1**
Bit	**Read/ Write**	**Default /Hex**	**Description**
31:16	/	/	/
5	R/W	0x0	GPADC_EN. GPADC Function Enable 0: Disable

			1: Enable
4	R/W	0x0	GPADC_MODE_SELECT. Auxiliary ADC Mode Select 0: Reserved 1: Auxiliary ADC
3	R/W	0x0	ADC_CHAN3_SELECT. Analog input channel 3 Select 0: Disable 1: Enable
2	R/W	0x0	ADC_CHAN2_SELECT. Analog input channel 2 Select 0: Disable 1: Enable
1	R/W	0x0	ADC_CHAN1_SELECT. Analog input channel 1 Select 0: Disable 1: Enable
0	R/W	0x1	ADC_CHAN0_SELECT. Analog input channel 0 Select 0: Disable 1: Enable

Notes：Channel 0~3 can be selected at the same time, but N channel selected, each channel has 1/N full speed of the ADC. When there are only one channel selected, it has the full conversion rate.

3.16.5.3. MEDIAN AND AVERAGING FILTER CONTROL REGISTER

Offset: 0x0c			**Register Name: GPADC_CTRL2**
Bit	**Read/Write**	**Default/Hex**	**Description**

31:3	/	/	/
2	R/W	0x0	FILTER_EN. Filter Enable 0: Disable 1: Enable
1:0	R/W	0x1	FILTER_TYPE. Filter Type 00: 4/2 01: 5/3 10: 8/4 11: 16/8

3.16.5.4. GPADC INTERRUPT& FIFO CONTROL REGISTER

Offset: 0x10			Register Name: GPADC_INT
Bit	**Read/Write**	**Default/Hex**	**Description** **0x0000_0F00**
31:18	/	/	/
17	R/W	0x0	GPADC_OVERRUN_IRQ_EN. GPADC FIFO Over Run IRQ Enable 0: Disable 1: Enable
16	R/W	0x0	GPADC_DATA_IRQ_EN. GPADC FIFO Data Available IRQ Enable 0: Disable 1: Enable
15:13	/	/	/
12:8	R/W	0xF	GPADC_FIFO_TRIG_LEVEL. GPADC FIFO Data Available Trigger Level Interrupt and DMA request trigger level for Auxiliary ADC

			Trigger Level = TXTL + 1
7	R/W	0x0	GPADC_DATA_DRQ_EN. GPADC FIFO Data Available DRQ Enable 0: Disable 1: Enable
6:5	/	/	/
4	R/W	0x0	GPADC_FIFO_FLUSH. GPADC FIFO Flush Write '1' to flush TX FIFO, self clear to '0'
3:0	/	/	/

3.16.5.5. GPADC INTERRUPT& FIFO STATUS REGISTER

Offset: 0x14			Register Name: GPADC_FIFOCS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	FIFO_OVERRUN_PENDING. GPADC FIFO Over Run IRQ pending 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
16	R/W	0x0	FIFO_DATA_PENDING. GPADC FIFO Data Available pending Bit 0: NO Pending IRQ 1: FIFO Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
15:13	/	/	/
12:8	R	0x0	RXA_CNT. GPADC FIFO available Sample Word Counter
7:0	/	/	/

3.16.5.6. GPADC DATA REGISTER

Offset: 0x24			Register Name: GPDAC_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x0	GPADC_DATA. Auxiliary analog input data converted by the internal ADC

Notes： In Auxiliary ADC mode, the data stored in this register bases on ADC_CHAN_SELECT. If four channels are all enable, FIFO will access the input data in successive turn, first is ADC_CHAN0 data, then ADC_CHAN1, ADC_CHAN2, ADC_CHAN3 data. If there are only two or three channels selected, such as ADC_CHAN0 and ADC_CHAN3, firstly ADC_CHAN0 input data is accessed, then ADC_CHAN3 input data.

3.16.5.7. GPADC PORT IO CONFIGURE REGISTER

Offset: 0x28			Register Name: GPADC_IO_CONFIG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:12	R/W	0x2	ADCY2_SELECT ADCY2 Port Function Select: 000：Input 001:Output 010: 011:/ 100: / 101:/ 110: / 111:/
11	/	/	/
10:8	R/W	0x2	ADCY1_SELECT ADCY1 Port Function Select: 000：Input 001:Output 010: 011:/ 100: / 101:/ 110: / 111:/

7	/	/	/
6:4	R/W	0x2	ADCX2_SELECT ADCX2 Port Function Select: 000：Input 001:Output 010: 011:/ 100: / 101:/ 110: / 111:/
3	/	/	/
2:0	R/W	0x2	ADCX1_SELECT ADCX1 Port Function Select: 000：Input 001:Output 010: 011:/ 100: / 101:/ 110: / 111:/

3.16.5.8. GPADC PORT DATA REGISTER

Offset: 0x2c			Register Name: GPADC_PORT_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x0	GPADC_PORT_DATA GPADC Port Data Value,

3.17. LRADC

3.17.1. OVERVIEW

The LRADC of 6-bit resolution is used for key application.

It features:

- Support APB 32-bit bus width
- Support interrupt
- Support Hold Key and General Key
- Support Single Key and Continue Key mode
- 6-bit resolution
- Voltage input range between 0V to 2V

3.17.2. LRADC BLOCK DIAGRAM

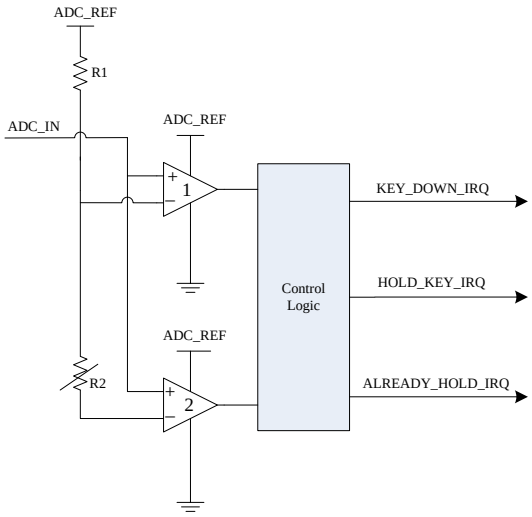


Figure 3-10 LRADC Block Diagram

3.17.3. LRADC REGISTER LIST

Module Name	Base Address
LRADC	0x01C22800

Register Name	Offset	Description
LRADC_CTRL	0x00	LRADC Control Register
LRADC_INTC	0x04	LRADC Interrupt Control Register
LRADC_INTS	0x08	LRADC Interrupt Status Register
LRADC_DATA0	0x0c	LRADC Data Register 0
LRADC_DATA1	0x10	LRADC Data Register 1

3.17.4. LRADC REGISTER DESCRIPTION

3.17.4.1. LRADC CONTROL REGISTER DESCRIPTION

Offset: 0x00			Register Name: LRADC_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x1	FIRST_CONVERT_DLY. ADC First Convert Delay setting, ADC conversion is delayed by (n+1) samples
23:22	R/W	0x0	ADC_CHAN_SELECT. ADC channel select 00: ADC0 channel 01： ADC1 channel 1x: ADC0&ADC1 channel
21:20	/	/	/
19:16	R/W	0x0	CONTINUE_TIME_SELECT. Continue Mode time select, one of 8*(N+1) sample as a valuable sample

			data
15:14	/	/	/
13:12	R/W	0x0	KEY_MODE_SELECT. Key Mode Select: 00: Normal Mode 01: Single Mode 10: Continue Mode
11:8	R/W	0x1	LEVELA_B_CNT. Level A to Level B time threshold select, judge ADC convert value in level A to level B in n+1 samples
7	R/W	0x0	LRADC_HOLD_KEY_EN LRADC hold key Enable 0: Disable 1: Enable
6	R/W	0x1	LRADC_HOLD_EN. LRADC Sample hold Enable 0: Disable 1: Enable
5: 4	R/W	0x2	LEVELB_VOL. Level B Corresponding Data Value setting (the real voltage value) 00: 0x3C (~1.9v) 01: 0x39 (~1.8v) 10: 0x36 (~1.7v) 11: 0x33 (~1.6v)
3: 2	R/W	0x2	LRADC_SAMPLE_RATE. LRADC Sample Rate 00: 250 Hz 01: 125 Hz 10: 62.5 Hz

			11: 32.25 Hz
1	/	/	/
0	R/W	0x0	LRADC_EN. LRADC enable 0: Disable 1: Enable

3.17.4.2. LRADC INTERRUPT CONTROL REGISTER

Offset: 0x04			Register Name: LRADC_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12	R/W	0x0	ADC1_KEYUP_IRQ_EN. ADC 1 Key Up IRQ Enable 0: Disable 1: Enable
11	R/W	0x0	ADC1_ALRDY_HOLD_IRQ_EN. ADC 1 Already Hold Key IRQ Enable 0: Disable 1: Enable
10	R/W	0x0	ADC 1 Hold Key IRQ Enable 0: Disable 1: Enable
9	R/W	0x0	ADC1_KEY DOWN IRQ_EN. ADC 1 Key Down IRQ Enable 0: Disable 1: Enable
8	R/W	0x0	ADC1_DATA_IRQ_EN. ADC 1 DATA IRQ Enable

			0: Disable 1: Enable
7:5	/	/	/
4	R/W	0x0	ADC0_KEYUP_IRQ_EN. ADC 0 Key Up IRQ Enable 0: Disable 1: Enable
3	R/W	0x0	ADC0_ALRDY_HOLD_IRQ_EN. ADC 0 Already Hold IRQ Enable 0: Disable 1: Enable
2	R/W	0x0	ADC0_HOLD_IRQ_EN. ADC 0 Hold Key IRQ Enable 0: Disable 1: Enable
1	R/W	0x0	ADC0_KEYDOWN_EN ADC 0 Key Down Enable 0: Disable 1: Enable
0	R/W	0x0	ADC0_DATA_IRQ_EN. ADC 0 Data IRQ Enable 0: Disable 1: Enable

3.17.4.3. LRADC INTERRUPT STATUS REGISTER

Offset: 0x08			Register Name: LRADC_INT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12		0x0	ADC1_KEYUP_PENDING.

			ADC 1 Key up pending Bit When general key pull up, if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable
11	R/W	0x0	ADC1_ALRDY_HOLD_PENDING. ADC 1 Already Hold Pending Bit When hold key pull down and pull the general key down, if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable
10	R/W	0x0	ADC1_HOLDKEY_PENDING. ADC 1 Hold Key pending Bit When Hold key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled. 0: NO IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.
9	R/W	0x0	ADC1_KEYDOWN_IRQ_PENDING. ADC 1 Key Down IRQ Pending Bit When General key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending

			Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.
8	R/W	0x0	ADC1_DATA_IRQ_PENDING. ADC 1 Data IRQ Pending Bit 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.
7:5	/	/	/
4	R/W	0x0	ADC0_KEYUP_PENDING. ADC 0 Key up pending Bit When general key pull up, it the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable
3	R/W	0x0	ADC0_ALRDY_HOLD_PENDING. ADC 0 Already Hold Pending Bit When hold key pull down and pull the general key down, if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable
2	R/W	0x0	ADC0_HOLDKEY_PENDING. ADC 0 Hold Key pending Bit When Hold key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled.

			0: NO IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.
1	R/W	0x0	ADC0_KEYDOWN_PENDING. ADC 0 Key Down IRQ Pending Bit When General key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.
0	R/W	0x0	ADC0_DATA_PENDING. ADC 0 Data IRQ Pending Bit 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.

3.17.4.4. LRADC DATA 0 REGISTER

Offset: 0x0c			Register Name: LRADC_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:0	R	0x0	LRADC0_DATA. LRADC 0 Data

3.17.4.5. LRADC DATA 1 REGISTER

Offset: 0x10			Register Name: LRADC_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**

31:6	/	/	/
5:0	R	0x0	LRADC1_DATA. LRADC 1 Data

3.18. AUDIO CODEC

3.18.1. OVERVIEW

The embedded Audio Codec is a high-quality stereo audio codec with headphone amplifier used for mobile computing and communications. It provides a stereo DAC for playback as well a stereo ADC for recording.

The audio CODEC features:

- Two audio digital-to-analog(DAC) channels
- Stereo capless headphone drivers:
- Support up to 100dBA SNR for DAC playback
- Support DAC Sample Rates from 8KHz to 192KHz
- Support analog/ digital volume control
- Differential receiver driver
- Two low-noise analog microphone bias outputs
- Analog low-power loop from line-in /microphone/phonein to headphone/receiver outputs
- Accessory button press detection
- Support five audio inputs (three differential microphone inputs, Stereo line-in input, differential Phonein input)
- Support two audio analog-to-digital(ADC) channels
- Support 96dBA SNR for ADC record
- Support ADC sample rates from 8KHz to 48KHz
- Support Automatic Gain Control (AGC)
- Support digital MIC interface

3.18.2. AUDIO CODEC BLOCK DIAGRAM

The embedded Audio Codec block diagram is shown below:

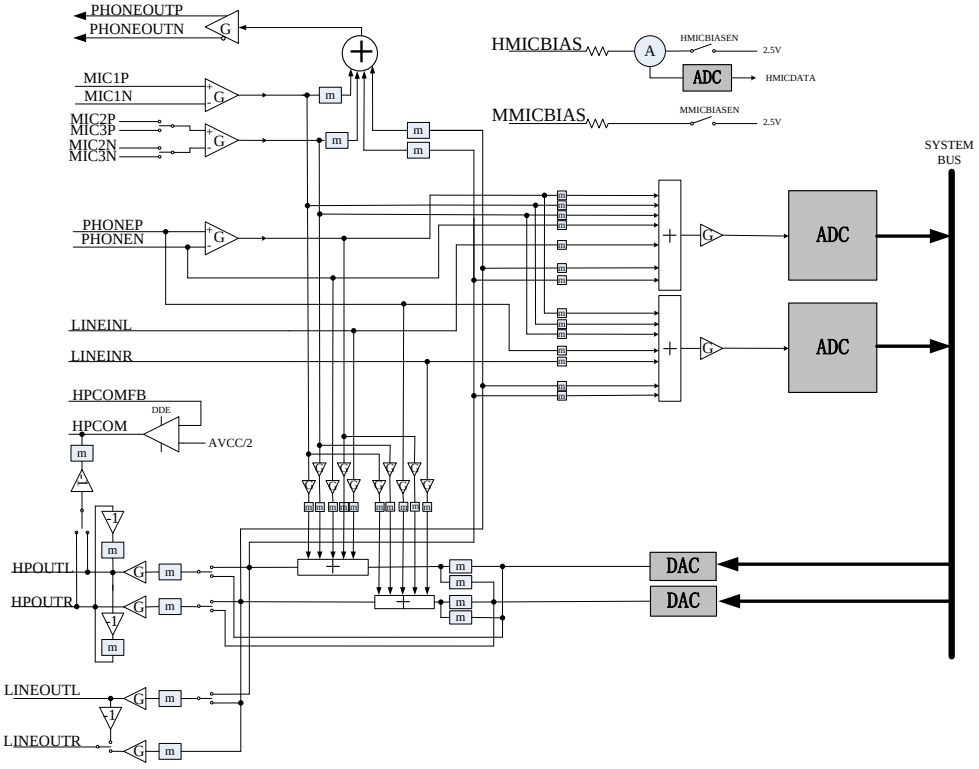


Figure 3-11 Audio Codec Block Diagram

3.18.3. AUDIO CODEC REGISTER LIST

Module Name	Base Address
AC	0x01C22C00

Register Name	Offset	Description
AC_DAC_DPC	0x00	DAC Digital Part Control Register
AC_DAC_FIFOC	0x04	DAC FIFO Control Register
AC_DAC_FIFOS	0x08	DAC FIFO Status Register
AC_DAC_TXDATA	0x0c	DAC TX Data Register

AC_ADC_FIFOC	0x10	ADC FIFO Control Register
AC_ADC_FIFOS	0x14	ADC FIFO Status Register
AC_ADC_RXDATA	0x18	ADC RX Data Register
OM_DACA_CTRL	0x20	Output Mixer & DAC Analog Control Register
OM_PA_CTRL	0x24	Output Mixer & PA Control Register
AC_MIC_CTRL	0x28	Microphone, Lineout and Phoneout Control Register
AC_ADCA_CTRL	0x2c	ADC Analog Control Register
ADDA_TUNE	0x30	ADDA Analog Performance Tuning Register
AC_CALIBRATION	0x34	Bias & DA16 Calibration Verify Register
AC_DAC_CNT	0x40	DAC TX FIFO Counter Register
AC_ADC_CNT	0x44	ADC RX FIFO Counter Register
HMIC_CTL	0x50	HMIC Control Register
HMIC_DATA	0x54	HMIC ADC Data Register
AC_DAC_DAPCTL	0x60	DAC DAP Control Register
AC_DAC_DAPVOL	0x64	DAC DAP Volume Register
AC_DAC_DAPCOF	0x68	DAC DAP Coefficient Register
AC_DAC_DAPOPT	0x6c	DAC DAP Optimum Register
AC_ADC_DAPCTL	0x70	ADC DAP Control Register
AC_ADC_DAPVOL	0x74	ADC DAP Volume Register
AC_ADC_DAPLCTL	0x78	ADC DAP Left Control Register
AC_ADC_DAPRCTL	0x7c	ADC DAP Right Control Register
AC_ADC_DAPPARA	0x80	ADC DAP Parameter Control Register
AC_ADC_DAPLAC	0x84	ADC DAP Left Average Coefficient Register
AC_ADC_DAPLDAT	0x88	ADC DAP Left Decay&Attack Time Register
AC_ADC_DAPRAC	0x8c	ADC DAP Right Average Coefficient Register
AC_ADC_DAPRDAC	0x90	ADC DAP Right Decay&Attack Time Register
AC_ADC_DAPHPFC	0x94	ADC DAP HPF Coefficient Register

3.18.4. AUDIO CODEC REGISTER DESCRIPTION

3.18.4.1. 00H_DAC DIGITAL PART CONTROL REGISTER

Offset: 0x00			Register Name: AC_DAC_DPC
Bit	**Read/Write**	**Default**	**Description**
31	R/W	0x0	EN_DA. DAC Digital Part Enable 0: Disable 1: Enable
30:29	/	/	/
28:25	R/W	0x0	MODQU. Internal DAC Quantization Levels Levels=[7*(21+MODQU[3:0])]/128 Default levels=7*21/128=1.15
24	R/W	0x0	DWA. DWA Function Disable 0: Enable 1: Disable
23:19	/	/	/
18	R/W	0x0	HPF_EN. High Pass Filter Enable 0: Disable 1: Enable
17:12	R/W	0x0	DVOL. Digital volume control: dvc, ATT=DVC[5:0]*(-1.16dB) 64 steps, -1.16dB/step
11:0	/	/	/

3.18.4.2. 04H_DAC FIFO CONTROL REGISTER

Offset: 0x04			Register Name: AC_DAC_FIFOC
Bit	**Read/Write**	**Default**	**Description**
31:29	R/W	0x0	DAC_FS. Sample Rate of DAC 000: 48KHz 010: 24KHz 100: 12KHz 110: 192KHz 001: 32KHz 011: 16KHz 101: 8KHz 111: 96KHz 44.1KHz/22.05KHz/11.025KHz can be supported by Audio PLL Configure Bit
28	R/W	0	FIR_VER FIR Version 0: 64-Tap FIR; 1: 32-Tap FIR
27	/	/	/
26	R/W	0x0	SEND_LASAT. Audio sample select when TX FIFO under run 0: Sending zero 1: Sending last audio sample
25:24	R/W	0x0	FIFO_MODE. For 24-bits transmitted audio sample: **00/10:** FIFO_I[23:0] = {TXDATA[31:8]} **01/11:** Reserved For 16-bits transmitted audio sample: **00/10:** FIFO_I[23:0] = {TXDATA[31:16], 8'b0}

			01/11: FIFO_I[23:0] = {TXDATA[15:0], 8'b0}
23	/	/	/
22:21	R/W	0x0	DAC_DRQ_CLR_CNT. When TX FIFO available room less than or equal N, DRQ Request will be de-asserted. N is defined here: 00: IRQ/DRQ Deasserted when WLEVEL > TXTL 01: 4 10: 8 11: 16
20:15	/	/	/
14:8	R/W	0xF	TX_TRIG_LEVEL. TX FIFO Empty Trigger Level (TXTL[12:0]) Interrupt and DMA request trigger level for TX FIFO normal condition. IRQ/DRQ Generated when WLEVEL ≤ TXTL **Notes:** 1. WLEVEL represents the number of valid samples in the TX FIFO 2. Only TXTL[6:0] valid when TXMODE = 0
7	R/W	0x0	ADDA_LOOP_EN. ADDA loop Enable 0: Disable 1: Enable
6	R/W	0x0	DAC_MONO_EN. DAC Mono Enable 0: Stereo, 64 levels FIFO 1: mono, 128 levels FIFO When enabled, L & R channel send same data
5	R/W	0x0	TX_SAMPLE_BITS. Transmitting Audio Sample Resolution 0: 16 bits 1: 24 bits

4	R/W	0x0	DAC_DRQ_EN. DAC FIFO Empty DRQ Enable 0: Disable 1: Enable
3	R/W	0x0	DAC_IRQ_EN. DAC FIFO Empty IRQ Enable 0: Disable 1: Enable
2	R/W	0x0	FIFO_UNDERRUN_IRQ_EN. DAC FIFO Under Run IRQ Enable 0: Disable 1: Enable
1	R/W	0x0	FIFO_OVERRUN_IRQ_EN. DAC FIFO Over Run IRQ Enable 0: Disable 1: Enable
0	R/W	0x0	FIFO_FLUSH. DAC FIFO Flush Write ‘1’ to flush TX FIFO, self clear to ‘0’

3.18.4.3. 08H_DAC FIFO STATUS REGISTER

Offset: 0x08			**Register Name: AC_DAC_FIFOS**
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
23	R	0x1	TX_EMPTY. TX FIFO Empty 0: No room for new sample in TX FIFO 1: More than one room for new sample in TX FIFO (>= 1 word)

22:8	R	0x80	TXE_CNT. TX FIFO Empty Space Word Counter
7:4	/	/	/
3	R/W	0x1	TXE_INT. TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt Write '1' to clear this interrupt or automatic clear if interrupt condition fails.
2	R/W	0x0	TXU_INT. TX FIFO Under run Pending Interrupt 0: No Pending Interrupt 1: FIFO Under run Pending Interrupt Write '1' to clear this interrupt
1	R/W	0x0	TXO_INT. TX FIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Overrun Pending Interrupt Write '1' to clear this interrupt
0	/	/	/

3.18.4.4. 0CH_DAC TX DATA REGISTER

Offset: 0x0C			Register Name: AC_DAC_TXDATA
Bit	**Read/Write**	**Default**	**Description**
31:0	W	0x0	TX_DATA. Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.

3.18.4.5. 10H_ADC FIFO CONTROL REGISTER

Offset: 0x10			Register Name: AC_ADC_FIFOC
Bit	**Read/Write**	**Default**	**Description**
31:29	R/W	0x0	ADFS. Sample Rate of ADC 000: 48KHz 010: 24KHz 100: 12KHz 110: Reserved 001: 32KHz 011: 16KHz 101: 8KHz 111: Reserved 44.1KHz/22.05KHz/11.025KHz can be supported by Audio PLL Configure Bit
28	R/W	0x0	EN_AD. ADC Digital Part Enable, en_ad 0: Disable 1: Enable
27	R/W	0x0	DigMic_EN Digital Microphone Enable, en_digmic 0: Analog ADC Mode 1: Digital Microphone Mode
26:25	/	/	/
24	R/W	0x0	RX_FIFO_MODE. RX FIFO Output Mode (Mode 0, 1) 0: Expanding '0' at LSB of TX FIFO register 1: Expanding received sample sign bit at MSB of TX FIFO register For 24-bits received audio sample:

			Mode 0: RXDATA[31:0] = {FIFO_O[23:0], 8'h0} Mode 1: Reserved For 16-bits received audio sample: Mode 0: RXDATA[31:0] = {FIFO_O[23:8], 16'h0} Mode 1: RXDATA[31:0] = {16{FIFO_O[23]}, FIFO_O[23:8]}
23:19	/	/	/
18:17	R/W	0x0	ADCFDT. ADC FIFO Delay Time For writing Data after en_ad 00:5ms 01:10ms 10:20ms 11:30ms
16	R/W	0x0	ADCDFEN. ADC FIFO Delay Function For writing Data after en_ad 0: Disable 1: Enable
15:13	/	/	/
12:8	R/W	0xF	RX_FIFO_TRG_LEVEL. RX FIFO Trigger Level (RXTL[4:0]) Interrupt and DMA request trigger level for TX FIFO normal condition IRQ/DRQ Generated when WLEVEL ＞ RXTL[4:0] **Notes:** WLEVEL represents the number of valid samples in the RX FIFO
7	R/W	0x0	ADC_MONO_EN. ADC Mono Enable. 0: Stereo, 16 levels FIFO 1: mono, 32 levels FIFO When set to '1', Only left channel samples are recorded
6	R/W	0x0	RX_SAMPLE_BITS.

			Receiving Audio Sample Resolution 0: 16 bits 1: 24 bits
5	/	/	/
4	R/W	0x0	ADC_DRQ_EN. ADC FIFO Data Available DRQ Enable. 0: Disable 1: Enable
3	R/W	0x0	ADC_IRQ_EN. ADC FIFO Data Available IRQ Enable. 0: Disable 1: Enable
2	/	/	/
1	R/W	0x0	ADC_OVERRUN_IRQ_EN. ADC FIFO Over Run IRQ Enable 0: Disable 1: Enable
0	R/W	0x0	ADC_FIFO_FLUSH. ADC FIFO Flush. Write '1' to flush TX FIFO, self clear to '0'.

3.18.4.6. 14H_ADC FIFO STATUS REGISTER

Offset: 0x14			**Register Name: AC_ADC_FIFOS**
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
23	R	0x0	RXA. RX FIFO Available 0: No available data in RX FIFO 1: More than one sample in RX FIFO (>= 1 word)

22:14	/	/	/
13:8	R	0x0	RXA_CNT. RX FIFO Available Sample Word Counter
7:4	/	/	/
3	R/W	0x0	RXA_INT. RX FIFO Data Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails.
2	/	/	/
1	R/W	0x0	RXO_INT. RX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt
0	/	/	/

3.18.4.7. 18H_ADC RX DATA REGISTER

Offset: 0x18			Register Name: AC_ADC_RXDATA
Bit	**Read/Write**	**Default**	**Description**
31:0	R	0x0	RX_DATA. RX Sample Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

3.18.4.8. 20H_OUTPUT MIXER & DAC ANALOG CONTROL REGISTER

Offset:0x20			Register Name: OMIXER_DACA_CTRL
Bit	**R/W**	**Default**	**Description**

31	R/W	0x0	DACAREN Internal DAC Analog Right channel Enable 0:Disable 1:Enable
30	R/W	0x0	DACALEN Internal DAC Analog Left channel Enable 0:Disable 1:Enable
29	R/W	0x0	RMIXEN Right Analog Output Mixer Enable 0:Disable 1:Enable
28	R/W	0x0	LMIXEN Left Analog Output Mixer Enable 0:Disable 1:Enable
27:24	/	/	/
23:17	R/W	0x0	RMIXMUTE Right Output Mixer Mute Control 0-Mute, 1-Not mute Bit 23: MIC1 Boost stage Bit 22: MIC2 Boost stage Bit 21: PHONEP-PHONEN Bit 20: PHONEP Bit 19: LINEINR Bit 18: DACR Bit 17: DACL
16:10	R/W	0x0	LMIXMUTE Left Output Mixer Mute Control

			0-Mute, 1-Not mute Bit 16: MIC1 Boost stage Bit 15: MIC2 Boost stage Bit 14: PHONEP-PHONEN Bit 13: PHONEN Bit 12: LINEINL Bit 11: DACL Bit 10: DACR
9	R/W	0x0	RHPIS Right Headphone Power Amplifier (PA) Input Source Select 0: DACR 1: Right Analog Mixer
8	R/W	0x0	LHPIS Left Headphone Power Amplifier (PA) Input Source Select 0: DACL 1: Left Analog Mixer
7	R/W	0x0	RHPPAMUTE All input source to Right Headphone PA mute, including Right Output mixer and Internal DACR: 0:Mute, 1: Not mute
6	R/W	0x0	LHPPAMUTE All input source to Left Headphone PA mute, including Left Output mixer and Internal DACL: 0:Mute, 1: Not mute
5:0	R/W	0x0	HPVOL Headphone Volume Control, (HPVOL): Total 64 level, from 0dB to -62dB, 1dB/step, mute when 000000

3.18.4.9. 24H_OUTPUT MIXER & PA CONTROL REGISTER

Offset:0x24			Register Name: OMIXER_PA_CTRL
Bit	**R/W**	**Default**	**Description**
31	R/W	0x0	HPPAEN Right & Left Headphone Power Amplifier Enable 0-disable 1-enable
30:29	R/W	0x0	HPCOM_CTL HPCOM function control 00: HPCOM off & output is floating 01: HPL inverting output 10: HPR inverting output 11: Direct driver for HPL & HPR
28	R/W	0x0	COMPTEN HPCOM output protection enable when it is set as Direct driver for HPL/R (COMPTEN) 0: protection disable 1: protection enable
27:26	R/W	0x1	PA_ANTI_POP_CTRL PA Anti-pop time Control 00:131ms; 01: 262ms; 10: 393ms; 11:524ms
25:18	/	/	/
17:15	R/W	0x3	MIC1G MIC1 BOOST stage to L or R output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
14:12	R/W	0x3	MIC2G MIC2 BOOST stage to L or R output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
11:9	R/W	0x3	LINEING

			LINEINL/R to L/R output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
8:6	R/W	0x3	PHONEG PHONEP-PHONEN gain stage to L/R output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
5:3	R/W	0x3	PHONEPG PHONEP to Right output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
2:0	R/W	0x3	PHONENG PHONEN to Left output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB

3.18.4.10. 28H_MICROPHONE, LINEOUT AND PHONEOUT CONTROL REGISTER

Offset:0x28			Register Name: AC_MIC_CTRL
Bit	**R/W**	**Default**	**Description**
31	R/W	0x0	HBIASEN Headset Microphone Bias enable 0: disable, 1: enable
30	R/W	0x0	MBIASEN Master Microphone Bias enable 0: disable, 1: enable
29	R/W	0x0	HBIASADCEN Headset MIC Bias Current sensor & ADC enable 0: Current sensor & ADC disabled 1: Current sensor & ADC enabled
28	R/W	0x0	MIC1AMPEN MIC1 Boost AMP Enable 0-Disable 1-Enable

27:25	R/W	0x4	MIC1BOOST MIC1 Boost AMP Gain Control 0dB when 000, 24dB to 42dB when 001 to 111, 3dB/step, default is 33dB
24	R/W	0x0	MIC2AMPEN MIC2 Boost AMP Enable 0-Disable 1-Enable
23:21	R/W	0x4	MIC2BOOST MIC2 Boost AMP Gain Control 0dB when 000, 24dB to 42dB when 001 to 111, 3dB/step, default is 33dB
20	R/W	0x0	MIC2SLT MIC2 Source Select 0:MIC3 1: MIC2
19	R/W	0x0	LINEOUTLEN Lineout Left Enable 0-disable 1-enable
18	R/W	0x0	LINEOUTREN Lineout Right Enable 0-disable 1-enable
17	R/W	0x0	LINEOUTLSRC Left lineout source select 0-left output mixer 1-left output mixer + right output mixer
16	R/W	0x0	LINEOUTRSRC Right lineout source select 0-right output mixer 1-left lineout, for differential output

15:11	R/W	0x0	LIENOUTVC Lineout Volume Control, Total 31 level, from 0dB to -48dB, 1.5dB/step, mute when 00000 & 00001
10:8	R/W	0x4	PHONEPREG PHONEP-PHONEN pre-amplifier gain control -12dB to 9dB, 3dB/step, default is 0dB
7:5	R/W	0x3	PHONEOUTG Phoneout Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
4	R/W	0x0	PHONEOUTEN Phoneout Enable 0: disable 1: enable
3	R/W	0x0	PHONEOUTS0 MIC1 Boost stage to Phone out mute 0: Mute, 1: Not mute
2	R/W	0x0	PHONEOUTS1 MIC2 Boost stage to Phone out mute 0: Mute, 1: Not mute
1	R/W	0x0	PHONEOUTS2 Right Output mixer to Phone out mute 0: Mute, 1: Not mute
0	R/W	0x0	PHONEOUTS3 Left Output mixer to Phone out mute 0: Mute, 1: Not mute

3.18.4.11. 2CH_ADC ANALOG CONTROL REGISTER

Offset:0x2c			Register Name: AC_ADCA_CTRL
Bit	**R/W**	**Default**	**Description**
31	R/W	0x0	ADCREN

			ADC Right Channel Enable 0-Disable; 1-Enable
30	R/W	0x0	ADCLEN ADC Left Channel Enable 0-Disable; 1-Enable
29:27	R/W	0x3	ADCRG ADC right channel Input Gain Control From -4.5dB to 6dB, 1.5dB/step default is 0dB
26:24	R/W	0x3	ADCLG ADC left channel Input Gain Control From -4.5dB to 6dB, 1.5dB/step default is 0dB
23:14	/	/	/
13:7	R/W	0x0	RADCMIXMUTE Right ADC Mixer Mute Control: 0: Mute; 1:On Bit 13: MIC1 Boost stage Bit 12: MIC2 Boost stage Bit 11: PHONEP-PHONEN Bit 10: PHONEP Bit 9: LINEINR Bit 8: Right output mixer Bit 7: Left output mixer
6:0	R/W	0x0	LADCMIXMUTE Left ADC Mixer Mute Control: 0: Mute; 1:On Bit 6: MIC1 Boost stage Bit 5: MIC2 Boost stage Bit 4: PHONEP-PHONEN Bit 3: PHONEN

			Bit 2: LINEINL Bit 1: Left output mixer Bit 0: Right output mixer

3.18.4.12. 30H_ADDA ANALOG PERFORMANCE TUNING REGISTER

Offset:0x30			Register Name: ADDA_TUNE
Bit	**R/W**	**Default**	**Description**
31	R/W	0x0	PA_SPEED_SELECT PA setup speed control 0: slow; 1: fast
30	R/W	0x0	PA_SLOPE_SELECT PA slope select cosine or ramp 0: select cosine 1: select ramp
29	R/W	0x0	/
28	R/W	0x1	MMIC_BIAS_CHOPPER_EN Main mic bias chopper enable 0: disable; 1:enable
27:26	R/W	0x2	MMIC BIAS_CHOPPER_CLK Main mic bias chopper clock select 00: 250KHz; 01: 500KHz; 10: 1MHz; 11: 2MHz
25	R/W	0x1	DITHER ADC dither on/off control 0: dither off; 1: dither on
24:23	R/W	0x1	DITHER_CLK ADC dither clock select 00: ADC FS * (8/9), about 43KHz when FS=48KHz 01: ADC FS * (16/15), about 51KHz when FS=48KHz 10: ADC FS * (4/3), about 64KHz when FS=48KHz

			11: ADC FS * (16/9), about 85KHz when FS=48KHz
22	R/W	0x1	ZERO_CROSSOVER_EN function enable for master volume change at zero cross over 0: disable; 1: enable
21	R/W	0x1	ZERO_CROSSOVER_TIME Timeout control for master volume change at zero cross over 0: 32ms; 1: 64ms
20:19	R/W	0x2	BIHE_CTRL BIHE control 00: no BIHE 01: BIHE=7.5 HOSC 10: BIHE=11.5 HOSC 11: BIHE=15.5 HOSC
18:17	R/W	0x0	PTDBS HPCOM protect de-bounce time setting 00: 2-3ms; 01: 4-6ms; 10: 8-12ms; 11: 16-24ms at the same time, bit 17 is used to control the AVCCPORFLAG, write 1 to this bit, flag will be clear, and the calibration is done again
16:14	R/W	0x2	USB_BIAS_CUR. USB bias current tuning From 23uA to 30uA, Default is 25uA
13:12	R/W	0x1	OPVR_BIAS_CUR. OPVR Bias Current Control
11:10	R/W	0x1	OPDAC_BIAS_CUR. OPDAC Bias Current Control Note: 00 is minimum, 11 is maximum
9:8	R/W	0x1	OPMIX_BIAS_CUR. OPMIX/OPLPF/OPDRV/OPCOM Bias Current Control Note: 00 is minimum, 11 is maximum

7:6	R/W	0x1	OPDRV_OPCOM_CUR. OPDRV/OPCOM output stage current setting Note: 00 is minimum, 11 is maximum
5:4	R/W	0x1	OPADC1_BIAS_CUR. OPADC1 Bias Current Select Note: 00 is minimum, 11 is maximum
3:2	R/W	0x1	OPADC2_BIAS_CUR. OPADC2 Bias Current Select Note: 00 is minimum, 11 is maximum
1:0	R/W	0x1	OPAAF_BIAS_CUR. OPAAF in ADC Bias Current Select Note: 00 is minimum, 11 is maximum

3.18.4.13. 34H_BIAS & DA16 CALIBRATION VERIFY REGISTER

Offset: 0x34			Register Name: AC_CALIBRATION
Bit	**Read/Write**	**Default**	**Description**
31:30	R/W	0x1	OPMIC_BIAS_CUR OPMIC bias current control
29	R/W	0x0	BIASCALIVERIFY Bias Calibration Verify 0: Calibration 1: Register setting
28:23	R/W	0x20	BIASVERIFY Bias Register Setting Data
22:17	R	0x0	BIASCALI Bias Calibration Data
16	R/W	0x0	DA16CALIVERIFY DA16 Calibration Verify 0: Calibration

			1: Register setting
15:8	R/W	0x80	DA16VERIFY DA16 Register Setting Data
7:0	R	0x0	DA16CALI DA16 Calibration Data

3.18.4.14. 40H_DAC TX COUNTER REGISTER

Offset: 0x40			**Register Name:** AC_**DAC_CNT**
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0x0	TX_CNT. TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value. Notes: It is used for Audio/ Video Synchronization

3.18.4.15. 44H_ADC RX COUNTER REGISTER

Offset: 0x44			**Register Name:** AC_**ADC_CNT**
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0x0	RX_CNT. RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value. Notes: It is used for Audio/ Video Synchronization

3.18.4.16. 50H_HMIC CONTROL REGISTER

Offset: 0x50			Register Name: HMIC_CTL
Bit	**Read/Write**	**Default**	**Description**
31:28	R/W	0x0	HMIC_M debounce when Key down or key up
27:24	R/W	0x0	HMIC_N debounce when earphone plug in or pull out
23	R/W	0x0	HMIC_DATA_IRQ_MODE Hmic Data Irq Mode Select 0: Hmic data irq once after key down 1: Hmic data irq from key down, util key up
22:21	R/W	0x0	HMIC_TH1_HYSTERESIS Hmic Hysteresis Threshold1 00: no Hysteresis 01: Pull Out when Data <= (Hmic_th2-1) 10: Pull Out when Data <= (Hmic_th2-2) 11: Pull Out when Data <= (Hmic_th2-3)
20	R/W	0x0	HMIC_PULLOUT_IRQ Hmic Earphone Pull out Irq Enable 00: disable 11: enable
19	R/W	0x0	HMIC_PLUGIN_IRQ Hmic Earphone Plug in Irq Enable 00: disable 11: enable
18	R/W	0x0	HMIC_KEYUP_IRQ Hmic Key Up Irq Enable 00: disable 11: enable
17	R/W	0x0	HMIC_KEYDOWN_IRQ Hmic Key Down Irq Enable

			00: disable 11: enable
16	R/W	0x0	HMIC_DATA_IRQ_EN Hmic Data Irq Enable 00: disable 11: enable
15:14	R/W	0x0	HMIC_SAMPLE_SELECT Down Sample Setting Select 00: Down by 1, 128Hz 01: Down by 2, 64Hz 10: Down by 4, 32Hz 11: Down by 8, 16Hz
13	R/W	0x0	HMIC_TH2_HYSTERESIS Hmic Hysteresis Threshold2 0: no Hysteresis 1: Key Up when Data <= (Hmic_th2-1)
12:8	R/W	0x0	HMIC_TH2 Hmic_th2 for detecting Key down or Key up.
7:6	R/W	0x0	HMIC_SF Hmic Smooth Filter setting 00: by pass 01: (x1+x2)/2 10: (x1+x2+x3+x4)/4 11: (x1+x2+x3+x4+ x5+x6+x7+x8)/8
5	R/W	0x0	KEYUP_CLEAR Key Up Irq Pending bit auto clear when Key Down Irq 0: don’t clear 1: auto clear
4:0	R/W	0x0	HMIC_TH1 Hmic_th1[4:0], detecting eraphone plug in or pull out.

3.18.4.17. 54H_HMIC DATA REGISTER

Offset: 0x54			Register Name: HMIC_DATA
Bit	**Read/Write**	**Default**	**Description**
31:21	/	/	/
20	R/W	0x0	HMIC_PULLOUT_PENDING Hmic Earphone Pull out Irq pending bit, write 1 to clear 0: No Pending Interrupt 1: Pull out Irq Pending Interrupt
19	R/W	0x0	HMIC_PLUGIN_PENDING Hmic Earphone Plug in Irq pending bit, write 1 to clear 0: No Pending Interrupt 1: Plug in Irq Pending Interrupt
18	R/W	0x0	HMIC_KEYUP_PENDING Hmic Key Up Irq pending bit, write 1 to clear 0: No Pending Interrupt 1: Key up Irq Pending Interrupt
17	R/W	0x0	HMIC_KEYDOWN_PENDING Hmic Key Down Irq pending bit, write 1 to clear 0: No Pending Interrupt 1: Key down Irq Pending Interrupt
16	R/W	0x0	HMIC_DATA_PENDING Hmic Data Irq pending bit, write 1 to clear 0: No Pending Interrupt 1: Data Irq Pending Interrupt
15:5	/	/	/
4:0	R	0x0	HMIC_DATA HMIC ADC Data

3.18.4.18. 60H_DAC DAP CONTROL REGISTER

Offset: 0x60			Register Name: AC_DAC_DAPCTL
Bit	**Read/Write**	**Default**	**Description**
31	R/W	0x0	DDAP _EN DAP for dac Enable 0 : bypass 1 : enable
30	R/W	0x1	DDAP _START DAP start control 0: start the DAP 1: shut down the DAP
29	R	0x1	DDAP_ STATE Dap for dac state 0: DAP working 1: shutdown When shut down the DAC, it should wait this bit to going to 1, and then shut down the DAC.
28:17	/	/	/
16	R/W	0x0	DDAP_BQ_EN BQ enable control 0:disable 1:enable
15	R/W	0x0	DDAP_DRC_EN DRC enable control 0:disable 1:enable
14	R/W	0x0	DDAP_HPF_EN HPF enable control 0:disable 1:enable
13:12	R/W	0x0	DDAP_DE_CTL DE function control 00:disable DE; 01:resvered;

			10:fs=44.1kHz DE; 11:fs=48kHz DE;
11:7	/	/	/
6:0	R/W	0x00	RAM_ADDR Ram address It will increase by one when the APB reading or writing the ram. When the APB writing or reading the ram, it must enable DAP (0x60.bit31) and disable BQ, DRC, DE, HPF firstly.

3.18.4.19. 64H_DAC DAP VOLUME REGISTER

Offset: 0x64			Register Name: AC_DAC_DAPVOL
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30	R/W	0x0	DDAP_LCHAN_MUTE Left channel soft mute control 0:unmute 1:mute
29	R/W	0x0	DDAP_RCHAN_MUTE Right channel soft mute control 0:unmute 1:mute
28	R/W	0x1	DDAP_MMUTE Master soft mute control 0:unmute 1:mute
27:26	/	/	/
25:24	R/W	0x1	DDAP_SKEW_CTL The volume skew time control. 00 : 256/fs 01 : 512/fs 10 : 1024/fs 11 : 2048/fs

			When user change the volume, the actual gain will increase or decrease 0.5dB at every skew time to reach the setting volume.
23:16	R/W	0x30(0dB)	M_GAIN Master Volume gain (-79dB – 24dB : the step is 0.5dB) 0x00 : 24dB 0x01 : 23.5dB ---------- 0xCE :-79dB
15:8	R/W	0x30(0dB)	DDAP_LCHAN_GAIN Left channel volume gain (-79dB – 24dB :the step is 0.5dB) 0x00 : 24dB 0x01 : 23.5dB ---------- 0xCE : -79dB
7:0	R/W	0x30(0dB)	DDAP_RCHAN_GAIN Right channel volume gain (-79dB – 24dB :the step is 0.5dB) 0x00 : 24dB 0x01 : 23.5dB ---------- 0xCE : -79dB

3.18.4.20. 68H_DAC DAP COEFFICIENT REGISTER

Offset: 0x68			Register Name: AC_DAC_DAPCOF
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0x0	DDAP_COF When the APB reading，the data is the RAM data，and writing，the data

			is being written to the RAM。 The Address of Coef Ram auto increment by 1 after reading or writing this register.

3.18.4.21. 70H_ADC DAP CONTROL REGISTER

Offset: 0x70			Register Name: AC_ADC_DAPCTL
Bit	**Read/Write**	**Default**	**Description**
31	R/W	0	ADAP _EN DAP for ADC enable 0 : bypass 1: enable
30	R/W	0	ADAP_ START DAP for ADC start up 0 : disable 1: start up
29:22	/	/	/
21	R	0	ADAP_LSATU_FLAG Left channel AGC saturation flag 0 : non_saturation 1: saturation
20	R	0	ADAP_LNOI_FLAG Left channel AGC noise-threshold flag
19:12	R	0x00	ADAP_LCHAN_GAIN Left channel Gain applied by AGC (7.1format 2s component(-20dB – 40dB), 0.5dB/ step) 0x50 : 40dB 0x4F : 39.5dB ---------- 0x00 : 00dB 0xFF : -0.5dB
11:10	/	/	/
9	R	0	ADAP_RSATU_FLAG

			Right AGC saturation flag 0 : non_saturation 1: saturation
8	R	0	ADAP_RNOI_FLAG Right channel AGC noise-threshold flag
7:0	R	0x00	ADAP_LCHAN_GAIN Right Channel Gain applied by AGC (7.1format 2s component)(0.5dB step） 0x50 : 40dB 0x4F : 39.5dB ---------- 0x00 : 00dB 0xFF : -0.5dB

3.18.4.22. 74H_ADC DAP VOLUME REGISTER

Offset: 0x74			Register Name: AC_ADC_DAPVOL
Bit	**Read/Write**	**Default**	**Description**
31:19	/	/	/
18	R/W	0	ADAP_LCHAN_MUTE Left channel volume mute 0:unmute 1:mute
17	R/W	0	ADAP_RCHAN_MUTE Right channel volume mute 0:unmute 1:mute
16	R/W	0	ADAP_SKEW_CTL Volume skew time control 0: every sample 1:two samples
15:14	/	/	/
13:8	R/W	0x28(0dB)	ADAP_LCHAN_GAIN Left channel volume gain setting

			(0.5dB/step) 000000 : 20dB 000001 : 19.5dB 000010 : 19dB --------- 101000 : 00dB 101001 : -0.5dB ---------- 111111 : -11.5dB
7:6	/	/	/
5:0	R/W	0x28(0dB)	ADAP_RCHAN_GAIN Right channel volume gain setting (0.5dB/step) 000000 : 20dB 000001 : 19.5dB 000010 : 19dB --------- 101000 : 00dB 101001 : -0.5dB ---------- 111111 :-11.5dB

3.18.4.23. 78H_ADC DAP LEFT CONTROL REGISTER

Offset: 0x78			Register Name: AC_ADC_DAPLCTL
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
23:16	R/W	0xA6(-90dB)	ADAP_LNOI_SET Left channel noise threshold setting (-90 -- -30dB, 8.0format).
15	/	/	/

14	R/W	1	AAGC_LCHAN_EN Left AGC funtion enable 0:disable 1: enable
13	R/W	1	ADAP_LHPF_EN Left HPF enable 0: disable 1: enable
12	R/W	1	ADAP_LNOI_DET Left Noise detect enable 0: disable 1: enable
11:10	/	/	/
9:8	R/W	0x0	ADAP_LCHAN_HYS Left Hysteresis setting 00 : 1dB 01 : 2dB 10 : 4dB 11 : disable;
7:4	R/W	0x0	ADAP_LNOI_DEB Left Noise debounce time 0000:0/fs 0001:4/fs 0010:8/fs ---------- 1111 :16*4096/fs $T=2^{(N+1)}/fs$, except N=0
3:0	R/W	0x0	ADAP_LSIG_DEB Left Signal debounce time 0000:0/fs 0001:4/fs 0010:8/fs

			---------- 1111 :16*4096/fs $T=2^{(N+1)}/fs$, except N=0

3.18.4.24. 7CH_ADC DAP RIGHT CONTROL REGISTER

Offset: 0x7c			Register Name: AC_ADC_DAPRCTL
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
23:16	R/W	0xA6(-90dB)	ADAP_RNOI_SET Right channel noise threshold setting (-90 -- -30dB, 8.0format).
15	/	/	/
14	R/W	1	AAGC_RCHAN_EN Right AGC enable 0:disable 1:enable
13	R/W	1	ADAP_RHPF_EN Right HPF enable 0: disable 1: enable
12	R/W	1	ADAP_RNOI_DET Right Noise detect enable 0: disable 1:enable
11:10	/	/	/
9:8	R/W	0x0	ADAP_RCHAN_HYS Right Hysteresis setting 00 : 1dB 01 : 2dB 10 : 4dB 11 : disable;
7:4	R/W	0x0	ADAP_RNOI_DEB Right Noise debounce time

			0000:0/fs 0001:4/fs 0010:8/fs ---------- 1111：16*4096/fs $T=2^{(N+1)}$/fs ,except N=0
3:0	R/W	0x0	ADAP_RSIG_DEB Right Signal debounce time 0000:0/fs 0001:4/fs 0010:8/fs ---------- 1111：16*4096/fs $T=2^{(N+1)}$/fs ,except N=0

3.18.4.25. 80H_ADC DAP PARAMETER REGISTER

Offset: 0x80			Register Name: AC_ADC_DAPPARA
Bit	**Read/Write**	**Default**	**Description**
31:30	/	/	/
29:24	R/W	0x2C(-20dB)	ADAP_LTARG_SET Left channel target level setting (-1dB -- -30dB). (6.0format 2s component)
23:22	/	/	/
21:16	R/W	0x2C(-20dB)	ADAP_RTARG_SET Right channel target level setting (-1dB -- -30dB). (6.0format 2s component)
15:8	R/W	0x28(20dB)	ADAP_LGAIN_MAX Left channel max gain setting (0-40dB). (7.1format 2s component)

7:0	R/W	0x28(20dB)	ADAP_RGAIN_MAX Right channel max gain setting (0-40dB). (7.1format 2s component)

3.18.4.26. 84H_ADC DAP LEFT AVERAGE COEF REGISTER

Offset: 0x84			Register Name: AC_ADC_DAPLAC
Bit	**Read/Write**	**Default**	**Description**
31:26	/	/	/
25:0	R/W	0x2_8F5C	ADAP_LAC Average level coefficient setting(3.23format 2s component)

3.18.4.27. 88H_ADC DAP LEFT DECAY&ATTACK TIME REGISTER

Offset: 0x88			Register Name: AC_ADC_DAPLDAT
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:16	R/W	0x0000	ADAP_LATT_SET Left attack time coefficient setting 0000 : 1x32/fs 0001 : 2x32/fs ---------- 7FFF : 2^{15} x32/fs T=(n+1)*31*fs When the gain decreases, the actual gain will decrease 0.5dB at every attack time.
15	/	/	/
14:0	R/W	0x001F (32x32fs)	ADAP_LDEC_SET Left decay time coefficient setting 0000 : 1x32/fs 0001 : 2x32/fs

			---------- 7FFF : 2^{15} x32/fs T=(n+1)*32/fs When the gain increases, the actual gain will increase 0.5dB at every decay time.

3.18.4.28. 8CH_ADC DAP RIGHT AVERAGE COEF REGISTER

Offset: 0x8c			Register Name: AC_ADC_DAPRAC
Bit	**Read/Write**	**Default**	**Description**
31:26	/	/	/
25:0	R/W	0x2_8F5C	ADAP_RAC Average level coefficient setting(3.23fomat)

3.18.4.29. 90H_ADC DAP RIGHT DECAY&ATTACK TIME REGISTER

Offset: 0x90			Register Name: AC_ADC_DAPRDAT
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:16	R/W	0x0000	ADAP_RATT_SET Right attack time coefficient setting 0000 : 1x32/fs 0001 : 2x32/fs ---------- 7FFF : 2^{15} x32/fs T=(n+1)*32/fs When the gain decreases, the actual gain will decrease 0.5dB at every attack time.
15	/	/	/
14:0	R/W	0x001F	ADAP_RDEC_SET Right decay time coefficient setting

			0000 : 1x32/fs 0001 : 2x32/fs ---------- 7FFF : 2^{15} x32/fs T=(n+1)*32/fs When the gain increases, the actual gain will increase 0.5dB at every decay time.

3.18.4.30. 94H_ADC DAP HPF COEF REGISTER

Offset: 0x94			Register Name: AC_ADC_DAPHPFC
Bit	**Read/Write**	**Default**	**Description**
31:26	/	/	/
25:0	R/W	0x07F FCB9	ADAP_HPFC HPF coefficient setting (3.23fomat)

3.19. PORT CONTROLLER(CPUX-PORT)

3.19.1. OVERVIEW

The chip has 8 ports for multi-functional input/out pins. They are:

- Port A(PA): 28 input/output port
- Port B(PB): 8 input/output port
- Port C(PC): 28 input/output port
- Port D(PD): 28 input/output port
- Port E(PE) : 17 input/output port
- Port F(PF) : 6 input/output port
- Port G(PG) : 19 input/output port
- Port H(PH) : 31 input/output port

These ports can be easily configured by software for various system configurations. All these ports can be configured as GPIO if multiplexed functions are not used. Totally 4 groups of external PIO interrupt sources are supported and interrupt mode can be configured by software.

3.19.2. PORT REGISTER LIST

Module Name	Base Address
PIO	0x01C20800

Register Name	Offset	Description
Pn_CFG0	n*0x24+0x00	Port n Configure Register 0 (n from 0 to 7)
Pn_CFG1	n*0x24+0x04	Port n Configure Register 1 (n from 0 to 7)
Pn_CFG2	n*0x24+0x08	Port n Configure Register 2 (n from 0 to 7)

Pn_CFG3	n*0x24+0x0C	Port n Configure Register 3 (n from 0 to 7)
Pn_DAT	n*0x24+0x10	Port n Data Register (n from 0 to 7)
Pn_DRV0	n*0x24+0x14	Port n Multi-Driving Register 0 (n from 0 to 7)
Pn_DRV1	n*0x24+0x18	Port n Multi-Driving Register 1 (n from 0 to 7)
Pn_PUL0	n*0x24+0x1C	Port n Pull Register 0 (n from 0 to 7)
Pn_PUL1	n*0x24+0x20	Port n Pull Register 1 (n from 0 to 7)
Pn_INT_CFG0	0x200+n*0x20+0x00	PIO Interrrupt Configure Register 0
Pn _INT_CFG1	0x200+n*0x20+0x04	PIO Interrrupt Configure Register 1
Pn _INT_CFG2	0x200+n*0x20+0x08	PIO Interrrupt Configure Register 2
Pn _INT_CFG3	0x200+n*0x20+0x0C	PIO Interrrupt Configure Register 3
Pn _INT_CTL	0x200+n*0x20+0x10	PIO Interrupt Control Register
Pn _INT_STA	0x200+n*0x20+0x14	PIO Interrupt Status Register
Pn _INT_DEB	0x200+n*0x20+0x18	PIO Interrupt Debounce Register

3.19.3. PORT REGISTER DESCRIPTION

3.19.3.1. PA CONFIGURE REGISTER 0

Offset: 0x00			**Register Name: PA_CFG0** **Default Value: 0x7777_7777**
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0x7	PA7_SELECT 000: Input 001: Output 010:ETXD7 011: LCD1_D7 100: UART1_CTS 101: Reserved 110: PA_EINT7 111: IO Disable
27	/	/	Reserved
26:24	R/W	0x7	PA6_SELECT

			000: Input	001: Output
			010:ETXD6	011: LCD1_D6
			100: UART1_RTS	101: Reserved
			110: PA_EINT6	111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PA5_SELECT 000: Input 010:ETXD5 100: UART1_RX 110: PA_EINT5	 001: Output 011: LCD1_D5 101: Reserved 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PA4_SELECT 000: Input 010: ETXD4 100: UART1_TX 110: PA_EINT4	 001: Output 011: LCD1_D4 101: Reserved 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PA3_SELECT 000: Input 010:ETXD3 100: UART1_RING 110: PA_EINT3	 001: Output 011: LCD1_D3 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PA2_SELECT 000: Input 010:ETXD2 100: UART1_DCD 110: PA_EINT2	 001: Output 011: LCD1_D2 101: Reserved 111: IO Disable
7	/	/	/	

6:4	R/W	0x7	PA1_SELECT 000: Input 010:ETXD1 100: UART1_DSR 110: PA_EINT1	 001: Output 011: LCD1_D1 101: Reserved 111: IO Disable
3	/	/	Reserved	
2:0	R/W	0x7	PA0_SELECT 000: Input 010:ETXD0 100: UART1_DTR 110: PA_EINT0	 001: Output 011: LCD1_D0 101: Reserved 111: IO Disable

3.19.3.2. PA CONFIGURE REGISTER 1

Offset: 0x04			**Register Name: PA_CFG1** **Default Value: 0x7777_7777**	
Bit	**Read/Write**	**Default**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PA15_SELECT 000: Input 010:ERXD4 100: CLKA_OUT 110: PA_EINT15	 001: Output 011: LCD1_D15 101: Reserved 111: IO Disable
27	/	/	/	
26:24	R/W	0x7	PA14_SELECT 000: Input 010:ERXD3 100: SDC3_D3 110: PA_EINT14	 001: Output 011: LCD1_D14 101: SDC2_D3 111: IO Disable
23	/	/	/	

22:20	R/W	0x7	PA13_SELECT 000: Input 010:ERXD2 100: SDC3_D2 110: PA_EINT13	 001: Output 011: LCD1_D13 101: SDC2_D2 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PA12_SELECT 000: Input 010:ERXD1 100: SDC3_D1 110: PA_EINT12	 001: Output 011: LCD1_D12 101: SDC2_D1 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PA11_SELECT 000: Input 010:ERXD0 100: SDC3_D0 110: PA_EINT11	 001: Output 011: LCD1_D11 101: SDC2_D0 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PA10_SELECT 000: Input 010:EGTXCLK 100: SDC3_CLK 110: PA_EINT10	 001: Output 011: LCD1_D10 101: SDC2_CLK 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PA9_SELECT 000: Input 010:ETXEN 100: SDC3_CMD 110: PA_EINT9	 001: Output 011: LCD1_D9 101: SDC2_CMD 111: IO Disable

3	/	/	/
2:0	R/W	0x7	PA8_SELECT 000: Input 001: Output 010:ETXCLK 011: LCD1_D8 100: ECLK_IN0 101: Reserved 110: PA_EINT8 111: IO Disable

3.19.3.3. PA CONFIGURE REGISTER 2

Offset: 0x08			Register Name: PA_CFG1 Default Value: 0x7777_7777
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0x7	PA23_SELECT 000: Input 001: Output 010:ECOL 011: LCD1_D23 100: SPI3_MOSI 101: Reserved 110: PA_EINT23 111: IO Disable
27	/	/	/
26:24	R/W	0x7	PA22_SELECT 000: Input 001: Output 010:ERXERR 011: LCD1_D22 100: SPI3_CLK 101: Reserved 110: PA_EINT22 111: IO Disable
23	/	/	/
22:20	R/W	0x7	PA21_SELECT 000: Input 001: Output 010:ETXERR 011: LCD1_D21 100: SPI3_CS0 101: Reserved 110: PA_EINT21 111: IO Disable

19	/	/	/
18:16	R/W	0x7	PA20_SELECT 000: Input 001: Output 010:ERXCLK 011: LCD1_D20 100: PWM3_N 101: Reserved 110: PA_EINT20 111: IO Disable
15	/	/	/
14:12	R/W	0x7	PA19_SELECT 000: Input 001: Output 010:ERXDV 011: LCD1_D19 100: PWM3_P 101: Reserved 110: PA_EINT19 111: IO Disable
11	/	/	/
10:8	R/W	0x7	PA18_SELECT 000: Input 001: Output 010:ERXD7 011: LCD1_D18 100: CLKB_OUT 101: Reserved 110: PA_EINT18 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PA17_SELECT 000: Input 001: Output 010:ERXD6 011: LCD1_D17 100: DMIC_DIN 101: Reserved 110: PA_EINT17 111: IO Disable
3	/	/	/
2:0	R/W	0x7	PA16_SELECT 000: Input 001: Output 010:ERXD5 011: LCD1_D16 100: DMIC_CLK 101: Reserved

			110: PA_EINT16	111: IO Disable

3.19.3.4. PA CONFIGURE REGISTER 3

Offset: 0x0C			Register Name: PA_CFG1 Default Value: 0x0000_7777	
Bit	**Read/Write**	**Default**	**Description**	
31:15	/	/	/	
14:12	R/W	0x7	PA27_SELECT 000: Input 010:EMDIO 100: ECLK_IN1 110: PA_EINT27	 001: Output 011: LCD1_VSYNC 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PA26_SELECT 000: Input 010:EMDC 100: CLKC_OUT 110: PA_EINT26	 001: Output 011: LCD1_HSYNC 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PA25_SELECT 000: Input 010:ECLKIN 100: SPI3_CS1 110: PA_EINT25	 001: Output 011: LCD1_DE 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PA24_SELECT 000: Input 010:ECRS 100: SPI3_MISO	 001: Output 011: LCD1_CLK 101: Reserved

			110: PA_EINT24 111: IO Disable

3.19.3.5. PA DATA REGISTER

Offset: 0x10			Register Name: PA_DAT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:28	/	/	/
27:0	R/W	0	PA_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.19.3.6. PA MULTI-DRIVING REGISTER 0

Offset: 0x14			Register Name: PA_DRV0 Default Value: 0x5555_5555
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x1	PA_DRV PA[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.19.3.7. PA MULTI-DRIVING REGISTER 1

Offset: 0x18			Register Name: PA_DRV1 Default Value: 0x0055_5555
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
[2i+1:2i]	R/W	0x1	PA_DRV

(i=0~11)			PA[n] Multi-Driving Select (n = 16~27) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.19.3.8. PA PULL REGISTER 0

Offset: 0x1C			Register Name: PA_PULL0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x0	PA_PULL PA[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.19.3.9. PA PULL REGISTER 1

Offset: 0x20			Register Name: PA_PULL1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x0	PA_PULL PA[n] Pull-up/down Select (n = 16~27) 00: Pull-up/down disable 01: Pull-up enable 10: Pull-down 11: Reserved

3.19.3.10. PB CONFIGURE REGISTER 0

Offset: 0x24			Register Name: PB_CFG0 Default Value: 0x7777_7777
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0x7	PB7_SELECT

			000: Input	001: Output
			010:I2S0_DI	011: Reserved
			100: Reserved	101: Reserved
			110: PB_EINT7	111: IO Disable
27	/	/	/	
26:24	R/W	0x7	PB6_SELECT 000: Input 010:I2S0_DO3 100: TWI3_SDA 110: PB_EINT6	 001: Output 011: UART3_RX 101: Reserved 111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PB5_SELECT 000: Input 010:I2S0_DO2 100: TWI3_SCK 110: PB_EINT5	 001: Output 011: UART3_TX 101: Reserved 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PB4_SELECT 000: Input 010:I2S0_DO1 100: Reserved 110: PB_EINT4	 001: Output 011: UART3_RTS 101: Reserved 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PB3_SELECT 000: Input 010:I2S0_DO0 100: Reserved 110: PB_EINT3	 001: Output 011: Reserved 101: Reserved 111: IO Disable
11	/	/	/	

10:8	R/W	0x7	PB2_SELECT 000: Input 010:I2S0_LRCK 100: Reserved 110: PB_EINT2	 001: Output 011: Reserved 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PB1_SELECT 000: Input 010:I2S0_BCLK 100: Reserved 110: PB_EINT1	 001: Output 011: Reserved 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PB0_SELECT 000: Input 010:I2S0_MCLK 100: MCS_MCLK1 110: PB_EINT0	 001: Output 011: UART3_CTS 101: Reserved 111: IO Disable

3.19.3.11. PB CONFIGURE REGISTER 1

Offset: 0x28			**Register Name: PB_CFG1** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.19.3.12. PB CONFIGURE REGISTER 2

Offset: 0x2C			**Register Name: PB_CFG2** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.19.3.13. PB CONFIGURE REGISTER 3

Offset: 0x30			Register Name: PB_CFG3 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.19.3.14. PB DATA REGISTER

Offset: 0x34			Register Name: PB_DAT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7:0	R/W	0	PB_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.19.3.15. PB MULTI-DRIVING REGISTER 0

Offset: 0x38			Register Name: PB_DRV0 Default Value: 0x0000_5555
Bit	**Read/Write**	**Default**	**Description**
31:16	/	/	Reserved
[2i+1:2i] (i=0~7)	R/W	0x1	PB_DRV PB[n] Multi-Driving Select (n = 0~7) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.19.3.16. PB MULTI-DRIVING REGISTER 1

Offset: 0x3C			Register Name: PB_DRV1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.19.3.17. PB PULL REGISTER 0

Offset: 0x40			Register Name: PB_PULL0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:16	/	/	Reserved
[2i+1:2i] (i=0~7)	R/W	0x0	PB_PULL PB[n] Pull-up/down Select (n = 0~7) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.19.3.18. PB PULL REGISTER 1

Offset: 0x44			Register Name: PB_PULL1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.19.3.19. PC CONFIGURE REGISTER 0

Offset: 0x48			Register Name: PC_CFG0 Default Value: 0x7777_7777
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0x7	PC7_SELECT 000: Input 001: Output

			010:NAND0_RB1	011: SDC2_CLK
			100: SDC3_CLK	101: Reserved
			110: Reserved	111: IO Disable
27	/	/	/	
26:24	R/W	0x7	PC6_SELECT 000: Input 010:NAND0_RB0 100: SDC3_CMD 110: Reserved	001: Output 011: SDC2_CMD 101: Reserved 111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PC5_SELECT 000: Input 010:NAND0_RE 100: Reserved 110: Reserved	001: Output 011: Reserved 101: Reserved 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PC4_SELECT 000: Input 010:NAND0_CE0 100: Reserved 110: Reserved	001: Output 011: Reserved 101: Reserved 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PC3_SELECT 000: Input 010:NAND0_NCE1 100: Reserved 110: Reserved	001: Output 011: Reserved 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PC2_SELECT	

			000: Input 001: Output 010:NAND0_CLE 011: SPI0_CLK 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PC1_SELECT 000: Input 001: Output 010:NAND0_ALE 011: SPI0_MISO 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
3	/	/	/
2:0	R/W	0x7	PC0_SELECT 000: Input 001: Output 010:NAND0_WE 011: SPI0_MOSI 100: Reserved 101: Reserved 110: Reserved 111: IO Disable

3.19.3.20. PC CONFIGURE REGISTER 1

Offset: 0x4C			**Register Name: PC_CFG1** **Default Value: 0x7777_7777**
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0x7	PC15_SELECT 000: Input 001: Output 010:NAND0_DQ7 011: SDC2_D7 100:SDC3_D7 101: Reserved 110: Reserved 111: IO Disable
27	/	/	/
26:24	R/W	0x7	PC14_SELECT

			000: Input 001: Output 010:NAND0_DQ6 011: SDC2_D6 100:SDC3_D6 101: Reserved 110: Reserved 111: IO Disable
23	/	/	/
22:20	R/W	0x7	PC13_SELECT 000: Input 001: Output 010: NAND0_DQ5 011: SDC2_D5 100: SDC3_D5 101: Reserved 110: Reserved 111: IO Disable
19	/	/	/
18:16	R/W	0x7	PC12_SELECT 000: Input 001: Output 010: NAND0_DQ4 011: SDC2_D4 100: SDC3_D4 101: Reserved 110: Reserved 111: IO Disable
15	/	/	/
14:12	R/W	0x7	PC11_SELECT 000: Input 001: Output 010: NAND0_DQ3 011: SDC2_D3 100: SDC3_D3 101: Reserved 110: Reserved 111: IO Disable
11	/	/	/
10:8	R/W	0x7	PC10_SELECT 000: Input 001: Output 010: NAND0_DQ2 011: SDC2_D2 100: SDC3_D2 101: Reserved 110: Reserved 111: IO Disable
7	/	/	/

6:4	R/W	0x7	PC9_SELECT 000: Input 010: NAND0_DQ1 100: SDC3_D1 110: Reserved	001: Output 011: SDC2_D1 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PC8_SELECT 000: Input 010: NAND0_DQ0 100: SDC3_D0 110: Reserved	001: Output 011: SDC2_D0 101: Reserved 111: IO Disable

3.19.3.21. PC CONFIGURE REGISTER 2

Offset: 0x50			Register Name: PC_CFG2 Default Value: 0x7777_7777	
Bit	**Read/Write**	**Default**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PC23_SELECT 000: Input 010:NAND0_DQ15 100: TRACE_DOUT7 110: Reserved	001: Output 011: NAND1_DQ7 101: Reserved 111: IO Disable
27	/	/	/	
26:24	R/W	0x7	PC22_SELECT 000: Input 010:NAND0_DQ14 100: TRACE_DOUT6 110: Reserved	001: Output 011: NAND1_DQ6 101: Reserved 111: IO Disable
23	/	/	/	

22:20	R/W	0x7	PC21_SELECT 000: Input 001: Output 010: NAND0_DQ13 011: NAND1_DQ5 100: TRACE_DOUT5 101: Reserved 110: Reserved 111: IO Disable
19	/	/	/
18:16	R/W	0x7	PC20_SELECT 000: Input 001: Output 010:NAND0_DQ12 011: NAND1_DQ4 100: TRACE_DOUT4 101: Reserved 110: Reserved 111: IO Disable
15	/	/	/
14:12	R/W	0x7	PC19_SELECT 000: Input 001: Output 010: NAND0_DQ11 011: NAND1_DQ3 100: TRACE_DOUT3 101: Reserved 110: Reserved 111: IO Disable
11	/	/	/
10:8	R/W	0x7	PC18_SELECT 000: Input 001: Output 010: NAND0_DQ10 011: NAND1_DQ2 100: TRACE_DOUT2 101: Reserved 110: Reserved 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PC17_SELECT 000: Input 001: Output 010:NAND0_DQ9 011: NAND1_DQ1 100:TRACE_DOUT1 101: Reserved 110: Reserved 111: IO Disable

3	/	/	/
2:0	R/W	0x7	PC16_SELECT 000: Input 001: Output 010: NAND0_DQ8 011: NAND1_DQ0 100: TRACE_DOUT0 101: Reserved 110: Reserved 111: IO Disable

3.19.3.22. PC CONFIGURE REGISTER 3

Offset: 0x54			Register Name: PC_CFG3 Default Value: 0x0000_7777
Bit	**Read/Write**	**Default**	**Description**
31:15	/	/	/
14:12	R/W	0x7	PC27_SELECT 000: Input 001: Output 010:Reserved 011: SPI0_CS0 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
11	/	/	/
10:8	R/W	0x7	PC26_SELECT 000: Input 001: Output 010: NAND0_CE3 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PC25_SELECT 000: Input 001: Output 010:NAND0_CE2 011: Reserved 100:Reserved 101: Reserved 110: Reserved 111: IO Disable

3	/	/	/
2:0	R/W	0x7	PC24_SELECT 000: Input 001: Output 010:NAND0_DQS 011: SDC2_RST 100:SDC3_RST 101: Reserved 110: Reserved 111: IO Disable

3.19.3.23. PC DATA REGISTER

Offset: 0x58			Register Name: PC_DAT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:28	/	/	/
27:0	R/W	0	PC_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.19.3.24. PC MULTI-DRIVING REGISTER 0

Offset: 0x5C			Register Name: PC_DRV0 Default Value: 0x5555_5555
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x1	PC_DRV PC[n] Multi-Driving_SELECT (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.19.3.25. PC MULTI-DRIVING REGISTER 1

Offset: 0x60			Register Name: PC_DRV1 Default Value: 0x0055_5555
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x1	PC_DRV PC[n] Multi-Driving Select (n = 16~27) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.19.3.26. PC PULL REGISTER 0

Offset: 0x64			Register Name: PC_PULL0 Default Value: 0x0000_5140
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x00005140	PC_PULL PC[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.19.3.27. PC PULL REGISTER 1

Offset: 0x68			Register Name: PC_PULL1 Default Value: 0x0054_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	**0x00540000**	PC_PULL PC[n] Pull-up/down Select (n = 16~27) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.19.3.28. PD CONFIGURE REGISTER 0

Offset: 0x6C			Register Name: PD_CFG0 Default Value: 0x7777_7777
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0x7	PD7_SELECT 000: Input 001: Output 010:LCD0_D7 011: LVDS0_VNC 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
27	/	/	Reserved
26:24	R/W	0x7	PD6_SELECT 000: Input 001: Output 010:LCD0_D6 011: LVDS0_VPC 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
23	/	/	/
22:20	R/W	0x7	PD5_SELECT 000: Input 001: Output 010:LCD0_D5 011: LVDS0_VN2 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
19	/	/	/
18:16	R/W	0x7	PD4_SELECT 000: Input 001: Output 010:LCD0_D4 011: LVDS0_VP2 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
15	/	/	/

14:12	R/W	0x7	PD3_SELECT 000: Input 010:LCD0_D3 100: Reserved 110: Reserved	001: Output 011: LVDS0_VN1 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PD2_SELECT 000: Input 010:LCD0_D2 100: Reserved 110: Reserved	001: Output 011: LVDS0_VP1 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PD1_SELECT 000: Input 010:LCD0_D1 100: Reserved 110: Reserved	001: Output 011: LVDS0_VN0 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PD0_SELECT 000: Input 010:LCD0_D0 100: Reserved 110: Reserved	001: Output 011: LVDS0_VP0 101: Reserved 111: IO Disable

3.19.3.29. PD CONFIGURE REGISTER 1

Offset: 0x70			**Register Name: PD_CFG1** **Default Value: 0x7777_7777**
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/

30:28	R/W	0x7	PD15_SELECT 000: Input 010:LCD0_D15 100:Reserved 110: Reserved	001: Output 011: LVDS1_VN2 101: Reserved 111: IO Disable
27	/	/	/	
26:24	R/W	0x7	PD14_SELECT 000: Input 010:LCD0_D14 100:Reserved 110: Reserved	001: Output 011: LVDS1_VP2 101: Reserved 111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PD13_SELECT 000: Input 010:LCD0_D13 100:Reserved 110: Reserved	001: Output 011: LVDS1_VN1 101: Reserved 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PD12_SELECT 000: Input 010:LCD0_D12 100:Reserved 110: Reserved	001: Output 011: LVDS1_VP1 101: Reserved 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PD11_SELECT 000: Input 010:LCD0_D11 100: Reserved 110: Reserved	001: Output 011: LVDS1_VN0 101: Reserved 111: IO Disable

11	/	/	/
10:8	R/W	0x7	PD10_SELECT 000: Input 001: Output 010:LCD0_D10 011: LVDS1_VP0 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PD9_SELECT 000: Input 001: Output 010:LCD0_D9 011: LVDS0_VN3 100:Reserved 101: Reserved 110: Reserved 111: IO Disable
3	/	/	/
2:0	R/W	0x7	PD8_SELECT 000: Input 001: Output 010:LCD0_D8 011: LVDS0_VP3 100:Reserved 101: Reserved 110: Reserved 111: IO Disable

3.19.3.30. PD CONFIGURE REGISTER 2

Offset: 0x74			**Register Name: PD_CFG2** **Default Value: 0x7777_7777**
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0x7	PD23_SELECT 000: Input 001: Output 010:LCD0_D23 011: Reserved 100:Reserved 101: Reserved 110: Reserved 111: IO Disable

27	/	/	/
26:24	R/W	0x7	PD22_SELECT 000: Input 001: Output 010: LCD0_D22 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
23	/	/	/
22:20	R/W	0x7	PD21_SELECT 000: Input 001: Output 010: LCD0_D21 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
19	/	/	/
18:16	R/W	0x7	PD20_SELECT 000: Input 001: Output 010: LCD0_D20 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
15	/	/	/
14:12	R/W	0x7	PD19_SELECT 000: Input 001: Output 010: LCD0_D19 011: LVDS1_VN3 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
11	/	/	/
10:8	R/W	0x7	PD18_SELECT 000: Input 001: Output 010: LCD0_D18 011: LVDS1_VP3 100: Reserved 101: Reserved

			110: Reserved	111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PD17_SELECT 000: Input 010: LCD0_D17 100: Reserved 110: Reserved	001: Output 011: LVDS1_VNC 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PD16_SELECT 000: Input 010: LCD0_D16 100: Reserved 110: Reserved	001: Output 011: LVDS1_VPC 101: Reserved 111: IO Disable

3.19.3.31. PD CONFIGURE REGISTER 3

Offset: 0x78			Register Name: PD_CFG3 Default Value: 0x0000_7777	
Bit	**Read/Write**	**Default**	**Description**	
31:16	/	/	/	
15	/	/	/	
14:12	R/W	0x7	PD27_SELECT 000: Input 010: LCD0_ VSYNC 100: Reserved 110: Reserved	001: Output 011: Reserved 101: Reserved 111: IO Disable
11	/	/	Reserved	
10:8	R/W	0x7	PD26_SELECT 000: Input 010: LCD0_ HSYNC	001: Output 011: Reserved

			100: Reserved	101: Reserved
			110: Reserved	111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PD25_SELECT 000: Input 010:LCD0_ DE 100:Reserved 110: Reserved	001: Output 011: Reserved 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PD24_SELECT 000: Input 010: LCD0_CLK 100: Reserved 110: Reserved	001: Output 011: Reserved 101: Reserved 111: IO Disable

3.19.3.32. PD DATA REGISTER

Offset: 0x7C			**Register Name: PD_DAT** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:28	/	/	/
27:0	R/W	0	PD_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.19.3.33. PD MULTI-DRIVING REGISTER 0

Offset: 0x80	**Register Name: PD_DRV0**

			Default Value: 0x5555_5555
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x1	PD_DRV PD[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.19.3.34. PD MULTI-DRIVING REGISTER 1

Offset: 0x84			**Register Name: PD_DRV1** **Default Value: 0x0055_5555**
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x1	PD_DRV PD[n] Multi-Driving Select (n = 16~27) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.19.3.35. PD PULL REGISTER 0

Offset: 0x88			**Register Name: PD_PULL0** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x0	PD_PULL PD[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.19.3.36. PD PULL REGISTER 1

Offset: 0x8C	**Register Name: PD_PULL1** **Default Value: 0x0000_0000**

Bit	Read/Write	Default	Description
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x0	PD_PULL PD[n] Pull-up/down Select (n = 16~27) 00: Pull-up/down disable 01: Pull-up enable 10: Pull-down 11: Reserved

3.19.3.37. PE CONFIGURE REGISTER 0

Offset: 0x90			Register Name: PE_CFG0 Default Value: 0x7777_7777
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0x7	PE7_SELECT 000: Input 001: Output 010: CSI_D3 011: UART5_CTS 100: Reserved 101: Reserved 110: PE_EINT7 111: IO Disable
27	/	/	/
26:24	R/W	0x7	PE6_SELECT 000: Input 001: Output 010: CSI_D2 011: UART5_RTS 100: Reserved 101: Reserved 110: PE_EINT6 111: IO Disable
23	/	/	/
22:20	R/W	0x7	PE5_SELECT 000: Input 001: Output 010: CSI_D1 011: UART5_RX 100: Reserved 101: Reserved 110: PE_EINT5 111: IO Disable

19	/	/	/
18:16	R/W	0x7	PE4_SELECT 000: Input 001: Output 010: CSI_D0 011: UART5_TX 100: Reserved 101: Reserved 110: PE_EINT4 111: IO Disable
15	/	/	/
14:12	R/W	0x7	PE3_SELECT 000: Input 001: Output 010:CSI_VSYNC 011: TS_DVLD 100: Reserved 101: Reserved 110: PE_EINT3 111: IO Disable
11	/	/	/
10:8	R/W	0x7	PE2_SELECT 000: Input 001: Output 010: CSI_HSYNC 011: TS_SYNC 100: Reserved 101: Reserved 110: PE_EINT2 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PE1_SELECT 000: Input 001: Output 010: CSI_MCLK 011: TS_ERR 100: Reserved 101: Reserved 110: PE_EINT1 111: IO Disable
3	/	/	/
2:0	R/W	0x7	PE0_SELECT 000: Input 001: Output 010: CSI_PCLK 011: TS_CLK 100: Reserved 101: Reserved

			110: PE_EINT0	111: IO Disable

3.19.3.38. PE CONFIGURE REGISTER 1

Offset: 0x94			Register Name: PE_CFG1 Default Value: 0x7777_7777	
Bit	**Read/Write**	**Default**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PE15_SELECT 000: Input 010: CSI_D11 100: Reserved 110: PE_EINT15	 001: Output 011: TS_D7 101: Reserved 111: IO Disable
27	/	/	/	
26:24	R/W	0x7	PE14_SELECT 000: Input 010: CSI_D10 100: Reserved 110: PE_EINT14	 001: Output 011: TS_D6 101: Reserved 111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PE13_SELECT 000: Input 010: CSI_D9 100: Reserved 110: PE_EINT13	 001: Output 011: TS_D5 101: Reserved 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PE12_SELECT 000: Input 010: CSI_D8 100: Reserved	 001: Output 011: TS_D4 101: Reserved

			110: PE_EINT12	111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PE11_SELECT 000: Input 010: CSI_D7 100: Reserved 110: PE_EINT11	001: Output 011: TS_D3 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PE10_SELECT 000: Input 010: CSI_D6 100: Reserved 110: PE_EINT10	001: Output 011: TS_D2 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PE9_SELECT 000: Input 010: CSI_D5 100: Reserved 110: PE_EINT9	001: Output 011: TS_D1 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PE8_SELECT 000: Input 010: CSI_D4 100: Reserved 110: PE_EINT8	001: Output 011: TS_D0 101: Reserved 111: IO Disable

3.19.3.39. PE CONFIGURE REGISTER 2

Offset: 0x98	**Register Name: PE_CFG2** **Default Value: 0x0000_0007**

Bit	Read/Write	Default	Description
31:3	/	/	/
2:0	R/W	0x7	PE16_SELECT 000: Input 001: Output 010: MCS_MCLK1 011: Reserved 100: Reserved 101: Reserved 110: PE_EINT16 111: IO Disable

3.19.3.40. PE CONFIGURE REGISTER 3

Offset: 0x9C			Register Name: PE_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.19.3.41. PE DATA REGISTER

Offset: 0xA0			Register Name: PE_DAT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:17	/	/	/
16:0	R/W	0	PE_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.19.3.42. PE MULTI-DRIVING REGISTER 0

Offset: 0xA4	Register Name: PE_DRV0 Default Value: 0x5555_5555

Bit	Read/Write	Default	Description
[2i+1:2i] (i=0~15)	R/W	0x1	PE_DRV PE[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.19.3.43. PE MULTI-DRIVING REGISTER 1

Offset: 0xA8			Register Name: PE_DRV1 Default Value: 0x0000_0001
Bit	**Read/Write**	**Default**	**Description**
31:2	/	/	/
1:0	R/W	0x1	PE_DRV PE[n] Multi-Driving Select (n = 16) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.19.3.44. PE PULL REGISTER 0

Offset: 0xAC			Register Name: PE_PULL0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x0	PE_PULL PE[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.19.3.45. PE PULL REGISTER 1

Offset: 0xB0			Register Name: PE_PULL1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**

31:0	/	/	/
1:0	R/W	0x0	PE_PULL PE[n] Pull-up/down Select (n = 16) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.19.3.46. PF CONFIGURE REGISTER 0

Offset: 0xB4			Register Name: PF_CFG0 Default Value: 0x0077_7777
Bit	**Read/Write**	**Default**	**Description**
31:23	/	/	/
22:20	R/W	0x7	PF5_SELECT 000: Input 001: Output 010: SDC0_D2 011: Reserved 100: JTAG_CK1 101: Reserved 110: Reserved 111: IO Disable
19	/	/	/
18:16	R/W	0x7	PF4_SELECT 000: Input 001: Output 010: SDC0_D3 011: Reserved 100: UART0_RX 101: Reserved 110: Reserved 111: IO Disable
15	/	/	/
14:12	R/W	0x7	PF3_SELECT 000: Input 001: Output 010: SDC0_CMD 011: Reserved 100: JTAG_DO1 101: Reserved 110: Reserved 111: IO Disable
11	/	/	/

10:8	R/W	0x7	PF2_SELECT 000: Input 010: SDC0_CLK 100: UART0_TX 110: Reserved	 001: Output 011: Reserved 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PF1_SELECT 000: Input 010:SDC0_D0 100: JTAG_DI1 110: Reserved	 001: Output 011: Reserved 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PF0_SELECT 000: Input 010:SDC0_D1 100: JTAG_MS1 110: Reserved	 001: Output 011: Reserved 101: Reserved 111: IO Disable

3.19.3.47. PF CONFIGURE REGISTER 1

Offset: 0xB8			**Register Name: PF_CFG1** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.19.3.48. PF CONFIGURE REGISTER 2

Offset: 0xBC			**Register Name: PF_CFG2** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**

31:0	/	/	/

3.19.3.49. PF CONFIGURE REGISTER 3

Offset: 0xC0			Register Name: PF_CFG3 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.19.3.50. PF DATA REGISTER

Offset: 0xC4			Register Name: PF_DAT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:6	/	/	/
5:0	R/W	0	PF_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.19.3.51. PF MULTI-DRIVING REGISTER 0

Offset: 0xC8			Register Name: PF_DRV0 Default Value: 0x0000_0555
Bit	**Read/Write**	**Default**	**Description**
31:12	/	/	/
[2i+1:2i] (i=0~5)	R/W	0x1	PF_DRV PF[n] Multi-Driving Select (n = 0~5) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.19.3.52. PF MULTI-DRIVING REGISTER 1

Offset: 0xCC			Register Name: PF_DRV1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/

3.19.3.53. PF PULL REGISTER 0

Offset: 0xD0			Register Name: PF_PULL0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:12	/	/	/
[2i+1:2i] (i=0~5)	R/W	0x0	PF_PULL PF[n] Pull-up/down Select (n = 0~5) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.19.3.54. PF PULL REGISTER 1

Offset: 0xD4			Register Name: PF_PULL1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.19.3.55. PG CONFIGURE REGISTER 0

Offset: 0xD8			Register Name: PG_CFG0 Default Value: 0x7777_7777
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0x7	PG7_SELECT

			000: Input	001: Output
			010: UART2_RX	011: Reserved
			100: Reserved	101: Reserved
			110: PG_EINT7	111: IO Disable
27	/	/	/	
26:24	R/W	0x7	PG6_SELECT 000: Input 010: UART2_TX 100: Reserved 110: PG_EINT6	001: Output 011: Reserved 101: Reserved 111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PG5_SELECT 000: Input 010: SDC1_D3 100: Reserved 110: PG_EINT5	001: Output 011: Reserved 101: Reserved 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PG4_SELECT 000: Input 010: SDC1_D2 100: Reserved 110: PG_EINT4	001: Output 011: Reserved 101: Reserved 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PG3_SELECT 000: Input 010: SDC1_D1 100: Reserved 110: PG_EINT3	001: Output 011: Reserved 101: Reserved 111: IO Disable
11	/	/	/	

10:8	R/W	0x7	PG2_SELECT 000: Input 010: SDC1_D0 100: Reserved 110: PG_EINT2	 001: Output 011: Reserved 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PG1_SELECT 000: Input 010: SDC1_CMD 100: Reserved 110: PG_EINT1	 001: Output 011: Reserved 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PG0_SELECT 000: Input 010: SDC1_CLK 100: Reserved 110: PG_EINT0	 001: Output 011: Reserved 101: Reserved 111: IO Disable

3.19.3.56. PG CONFIGURE REGISTER 1

Offset: 0xDC			**Register Name: PG_CFG1** **Default Value: 0x7777_7777**	
Bit	**Read/Write**	**Default**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PG15_SELECT 000: Input 010: SPI1_MOSI 100: Reserved 110: PG_EINT15	 001: Output 011: I2S1_DIN 101: Reserved 111: IO Disable
27	/	/	/	

26:24	R/W	0x7	PG14_SELECT 000: Input 010:SPI1_CLK 100: Reserved 110: PG_EINT14	001: Output 011: I2S1_LRCK 101: Reserved 111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PG13_SELECT 000: Input 010: SPI1_CS0 100: Reserved 110: PG_EINT13	001: Output 011: I2S1_BCLK 101: Reserved 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PG12_SELECT 000: Input 010: SPI1_CS1 100: Reserved 110: PG_EINT12	001: Output 011: I2S1_MCLK 101: Reserved 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PG11_SELECT 000: Input 010: TWI3_SDA 100: Reserved 110: PG_EINT11	001: Output 011: USB_DM3 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PG10_SELECT 000: Input 010: TWI3_SCK 100: Reserved 110: PG_EINT10	001: Output 011: USB_DP3 101: Reserved 111: IO Disable

7	/	/	/
6:4	R/W	0x7	PG9_SELECT 000: Input 001: Output 010: UART2_CTS 011: Reserved 100: Reserved 101: Reserved 110: PG_EINT9 111: IO Disable
3	/	/	/
2:0	R/W	0x7	PG8_SELECT 000: Input 001: Output 010: UART2_RTS 011: Reserved 100: Reserved 101: Reserved 110: PG_EINT8 111: IO Disable

3.19.3.57. PG CONFIGURE REGISTER 2

Offset: 0xE0			Register Name: PG_CFG2 Default Value: 0x0000_0777
Bit	**Read/Write**	**Default**	**Description**
31:11	/	/	/
10:8	R/W	0x7	PG18_SELECT 000: Input 001: Output 010: UART4_RX 011: USB_DM3 100: Reserved 101: Reserved 110: PG_EINT18 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PG17_SELECT 000: Input 001: Output 010: UART4_TX 011: USB_DP3 100: Reserved 101: Reserved 110: PG_EINT17 111: IO Disable

3	/	/	/
2:0	R/W	0x7	PG16_SELECT 000: Input 001: Output 010:SPI1_MISO 011: I2S1_DOUT 100: Reserved 101: Reserved 110: PG_EINT16 111: IO Disable

3.19.3.58. PG CONFIGURE REGISTER 3

Offset: 0xE4			Register Name: PG_CFG3 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.19.3.59. PG DATA REGISTER

Offset: 0xE8			Register Name: PG_DAT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:19	/	/	/
18:0	R/W	0	PG_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.19.3.60. PG MULTI-DRIVING REGISTER 0

Offset: 0xEC			Register Name: PG_DRV0 Default Value: 0x5555_5555
Bit	**Read/Write**	**Default**	**Description**

[2i+1:2i] (i=0~15)	R/W	0x1	PG_DRV PG[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.19.3.61. PG MULTI-DRIVING REGISTER 1

Offset: 0xF0			Register Name: PG_DRV1 Default Value: 0x0000_0015
Bit	**Read/Write**	**Default**	**Description**
31:6	/	/	/
[2i+1:2i] (i=0~2)	R/W	0x1	PG_DRV PG[n] Multi-Driving Select (n = 16~18) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.19.3.62. PG PULL REGISTER 0

Offset: 0xF4			Register Name: PG_PULL0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x0	PG_PULL PG[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.19.3.63. PG PULL REGISTER 1

Offset: 0xF8			Register Name: PG_PULL1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:6	/	/	/

[2i+1:2i] (i=0~2)	R/W	0x0	PG_PULL PG[n] Pull-up/down Select (n = 16~18) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.19.3.64. PH CONFIGURE REGISTER 0

Offset: 0xFC			Register Name: PH_CFG0 Default Value: 0x7777_7777
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0x7	PH7_SELECT 000: Input 001: Output 010: NAND1_RB1 011: Reserved 100: TRACE_DOUT15 101: Reserved 110: Reserved 111: IO Disable
27	/	/	/
26:24	R/W	0x7	PH6_SELECT 000: Input 001: Output 010:NAND1_RB0 011: Reserved 100: TRACE_DOUT14 101: Reserved 110: Reserved 111: IO Disable
23	/	/	/
22:20	R/W	0x7	PH5_SELECT 000: Input 001: Output 010: NAND1_RE 011: Reserved 100: TRACE_DOUT13 101: Reserved 110: Reserved 111: IO Disable
19	/	/	/
18:16	R/W	0x7	PH4_SELECT

			000: Input	001: Output
			010:NAND1_CE0	011: Reserved
			100: TRACE_DOUT12	101: Reserved
			110: Reserved	111: IO Disable
15	/	/	/	
			PH3_SELECT	
			000: Input	001: Output
			010: NAND1_CE1	011: Reserved
			100: TRACE_DOUT11	101: Reserved
14:12	R/W	0x7	110: Reserved	111: IO Disable
11	/	/	/	
			PH2_SELECT	
			000: Input	001: Output
			010: NAND1_CLE	011: Reserved
			100: TRACE_DOUT10	101: Reserved
10:8	R/W	0x7	110: Reserved	111: IO Disable
7	/	/	/	
			PH1_SELECT	
			000: Input	001: Output
			010: NAND1_ALE	011: Reserved
			100: TRACE_DOUT9	101: Reserved
6:4	R/W	0x7	110: Reserved	111: IO Disable
3	/	/	/	
			PH0_SELECT	
			000: Input	001: Output
			010: NAND1_WE	011: Reserved
			100: TRACE_DOUT8	101: Reserved
2:0	R/W	0x7	110: Reserved	111: IO Disable

3.19.3.65. PH CONFIGURE REGISTER 1

Offset: 0x100			Register Name: PH_CFG1 Default Value: 0x7777_7777
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0x7	PH15_SELECT 000: Input 001: Output 010: TWI0_SDA 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
27	/	/	/
26:24	R/W	0x7	PH14_SELECT 000: Input 001: Output 010:TWI0_SCK 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
23	/	/	/
22:20	R/W	0x7	PH13_SELECT 000: Input 001: Output 010: PWM0 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
19	/	/	/
18:16	R/W	0x7	PH12_SELECT 000: Input 001: Output 010: SPI2_MISO 011: JTAG_DI0 100: PWM2_N 101: Reserved 110: Reserved 111: IO Disable
15	/	/	/

14:12	R/W	0x7	PH11_SELECT 000: Input 001: Output 010:SPI2_MOSI 011: JTAG_DO0 100: PWM2_P 101: Reserved 110: Reserved 111: IO Disable
11	/	/	/
10:8	R/W	0x7	PH10_SELECT 000: Input 001: Output 010:SPI2_CLK 011: JTAG_CK0 100: PWM1_N 101: Reserved 110: Reserved 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PH9_SELECT 000: Input 001: Output 010: SPI2_CS0 011: JTAG_MS0 100: PWM1_P 101: Reserved 110: Reserved 111: IO Disable
3	/	/	/
2:0	R/W	0x7	PH8_SELECT 000: Input 001: Output 010: NAND1_DQS 011: Reserved 100: TRACE_CLK 101: Reserved 110: Reserved 111: IO Disable

3.19.3.66. PH CONFIGURE REGISTER 2

Offset: 0x104			**Register Name: PH_CFG2** **Default Value: 0x7777_7777**
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/

30:28	R/W	0x7	PH23_SELECT 000: Input 010: Reserved 100: Reserved 110: Reserved	001: Output 011: Reserved 101: Reserved 111: IO Disable
27	/	/	/	
26:24	R/W	0x7	PH22_SELECT 000: Input 010: Reserved 100: Reserved 110: Reserved	001: Output 011: Reserved 101: Reserved 111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PH21_SELECT 000: Input 010: UART0_RX 100: Reserved 110: Reserved	001: Output 011: Reserved 101: Reserved 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PH20_SELECT 000: Input 010:UART0_TX 100: Reserved 110: Reserved	001: Output 011: Reserved 101: Reserved 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PH19_SELECT 000: Input 010:TWI2_SDA 100: Reserved 110: Reserved	001: Output 011: Reserved 101: Reserved 111: IO Disable

11	/	/	/
10:8	R/W	0x7	PH18_SELECT 000: Input 001: Output 010:TWI2_SCK 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PH17_SELECT 000: Input 001: Output 010:TWI1_SDA 011: Reserved 100:Reserved 101: Reserved 110: Reserved 111: IO Disable
3	/	/	/
2:0	R/W	0x7	PH16_SELECT 000: Input 001: Output 010: TWI1_SCK 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable

3.19.3.67. PH CONFIGURE REGISTER 3

Offset: 0x108			**Register Name: PH_CFG3** **Default Value: 0x0777_7777**
Bit	**Read/Write**	**Default**	**Description**
31:27	/	/	/
26:24	R/W	0x7	PH30_SELECT 000: Input 001: Output 010: NAND1_CE3 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable

23	/	/	/
22:20	R/W	0x7	PH29_SELECT 000: Input 001: Output 010: NAND1_CE2 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
19	/	/	/
18:16	R/W	0x7	PH28_SELECT 000: Input 001: Output 010: Reserved 011: Reserved 100: TRACE_CTL 101: Reserved 110: Reserved 111: IO Disable
15	/	/	/
14:12	R/W	0x7	PH27_SELECT 000: Input 001: Output 010:Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
11	/	/	/
10:8	R/W	0x7	PH26_SELECT 000: Input 001: Output 010:Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PH25_SELECT 000: Input 001: Output 010: Reserved 011: Reserved 100: Reserved 101: Reserved

			110: Reserved 111: IO Disable
3	/	/	/
2:0	R/W	0x7	PH24_SELECT 000: Input 001: Output 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable

3.19.3.68. PH DATA REGISTER

Offset: 0x10C			Register Name: PH_DAT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:0	R/W	0	PH_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.19.3.69. PH MULTI-DRIVING REGISTER 0

Offset: 0x110			Register Name: PH_DRV0 Default Value: 0x5555_5555
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x1	PH_DRV PH[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.19.3.70. PH MULTI-DRIVING REGISTER 1

Offset: 0x114			Register Name: PH_DRV1 Default Value: 0x1555_5555
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
[2i+1:2i] (i=0~14)	R/W	0x1	PH_DRV PH[n] Multi-Driving Select (n = 16~30) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.19.3.71. PH PULL REGISTER 0

Offset: 0x118			Register Name: PH_PULL0 Default Value: 0x0000_5140
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x5140	PH_PULL PH[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.19.3.72. PH PULL REGISTER 1

Offset: 0x11C			Register Name: PH_PULL1 Default Value: 0x1400_0000
Bit	**Read/Write**	**Default**	**Description**
31:30	/	/	/
[2i+1:2i] (i=0~14)	R/W	0x14000000	PH_PULL PH[n] Pull-up/down Select (n = 16~30) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.19.3.73. PA EXTERNAL INTERRUPT CONFIGURE REGISTER 0

Offset: 0x200			Register Name:PA_EINT_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[4i+3:4i] (i=0~7)	R/W	0	EINT_CFG External INTn Mode (n = 0~7) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

3.19.3.74. PA EXTERNAL INTERRUPT CONFIGURE REGISTER 1

Offset: 0x204			Register Name: PA_EINT_CFG1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[4i+3:4i] (i=0~7)	R/W	0	ENT_CFG External INTn Mode (n = 8~15) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

3.19.3.75. PA EXTERNAL INTERRUPT CONFIGURE REGISTER 2

Offset: 0x208	Register Name: PA_EINT_CFG2 Default Value: 0x0000_0000

Bit	Read/Write	Default	Description
[4i+3:4i] (i=0~7)	R/W	0	EINT_CFG External INTn Mode (n = 16~23) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

3.19.3.76. PA EXTERNAL INTERRUPT CONFIGURE REGISTER 3

Offset: 0x20C			Register Name: PA_EINT_CFG3 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:16	/	/	/
[4i+3:4i] (i=0~3)	R/W	0	EINT_CFG External INTn Mode (n = 24~27) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

3.19.3.77. PA EXTERNAL INTERRUPT CONTROL REGISTER

Offset: 0x210			Register Name: PA_EINT_CTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:28	/	/	/

[n] (n=0~27)	R/W	0	EINT_CTL External INTn Enable (n = 0~27) 0: Disable 1: Enable

3.19.3.78. PA EXTERNAL INTERRUPT STATUS REGISTER

Offset: 0x214			Register Name: PA_EINT_STATUS Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:28	/	/	/
[n] (n=0~27)	R/W	0	EINT_STATUS External INTn Pending Bit (n = 0~27) 0: No IRQ pending 1: IRQ pending Write '1' to clear

3.19.3.79. PA EXTERNAL INTERRUPT DEBOUNCE REGISTER

Offset: 0x218			Register Name: PA_EINT_DEB Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:7	/	/	/
6:4	R/W	0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32Khz 1: HOSC 24Mhz

3.19.3.80. PB EXTERNAL INTERRUPT CONFIGURE REGISTER 0

Offset: 0x220			Register Name:PB_EINT_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[4i+3:4i] (i=0~7)	R/W	0	EINT_CFG External INTn Mode (n = 0~7) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

3.19.3.81. PB EXTERNAL INTERRUPT CONFIGURE REGISTER 1

Offset: 0x224			Register Name: PB_EINT_CFG1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.19.3.82. PB EXTERNAL INTERRUPT CONFIGURE REGISTER 2

Offset: 0x228			Register Name: PB_EINT_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.19.3.83. PB EXTERNAL INTERRUPT CONFIGURE REGISTER 3

Offset: 0x22C	Register Name: PB_EINT_CFG3 Default Value: 0x0000_0000

Bit	Read/Write	Default	Description
31:0	/	/	/

3.19.3.84. PB EXTERNAL INTERRUPT CONTROL REGISTER

Offset: 0x230			Register Name: PB_EINT_CTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
[n] (n=0~7)	R/W	0	EINT_CTL External INTn Enable (n = 0~7) 0: Disable 1: Enable

3.19.3.85. PB EXTERNAL INTERRUPT STATUS REGISTER

Offset: 0x234			Register Name: PB_EINT_STATUS Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
[n] (n=0~7)	R/W	0	EINT_STATUS External INTn Pending Bit (n = 0~7) 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear

3.19.3.86. PB EXTERNAL INTERRUPT DEBOUNCE REGISTER

Offset: 0x238			Register Name: PB_EINT_DEB Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:7	/	/	/

6:4	R/W	0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32Khz 1: HOSC 24Mhz

3.19.3.87. PE EXTERNAL INTERRUPT CONFIGURE REGISTER 0

Offset: 0x240			**Register Name:PE_EINT_CFG0** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
[4i+3:4i] (i=0~7)	R/W	0	EINT_CFG External INTn Mode (n = 0~7) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

3.19.3.88. PE EXTERNAL INTERRUPT CONFIGURE REGISTER 1

Offset: 0x244			**Register Name: PE_EINT_CFG1** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
[4i+3:4i] (i=0~7)	R/W	0	ENT_CFG External INTn Mode (n = 8~15) 0x0: Positive Edge

			0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

3.19.3.89. PE EXTERNAL INTERRUPT CONFIGURE REGISTER 2

Offset: 0x248			Register Name: PE_EINT_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:4	/	/	/
[4i+3:4i] (i=0)	R/W	0	EINT_CFG External INTn Mode (n = 16) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

3.19.3.90. PE EXTERNAL INTERRUPT CONFIGURE REGISTER 3

Offset: 0x24C			Register Name: PE_EINT_CFG3 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.19.3.91. PE EXTERNAL INTERRUPT CONTROL REGISTER

Offset: 0x250	Register Name: PE_EINT_CTL Default Value: 0x0000_0000

Bit	Read/Write	Default	Description
31:28	/	/	/
[n] (n=0~16)	R/W	0	EINT_CTL External INTn Enable (n = 0~16) 0: Disable 1: Enable

3.19.3.92. PE EXTERNAL INTERRUPT STATUS REGISTER

Offset: 0x254			Register Name: PE_EINT_STATUS Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:28	/	/	/
[n] (n=0~16)	R/W	0	EINT_STATUS External INTn Pending Bit (n = 0~16) 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear

3.19.3.93. PE EXTERNAL INTERRUPT DEBOUNCE REGISTER

Offset: 0x258			Register Name: PE_EINT_DEB Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:7	/	/	/
6:4	R/W	0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select

			0: LOSC 32Khz 1: HOSC 24Mhz

3.19.3.94. PG EXTERNAL INTERRUPT CONFIGURE REGISTER 0

Offset: 0x260			Register Name:PG_EINT_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[4i+3:4i] (i=0~7)	R/W	0	EINT_CFG External INTn Mode (n = 0~7) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

3.19.3.95. PG EXTERNAL INTERRUPT CONFIGURE REGISTER 1

Offset: 0x264			Register Name: PG_EINT_CFG1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[4i+3:4i] (i=0~7)	R/W	0	ENT_CFG External INTn Mode (n = 8~15) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

3.19.3.96. PG EXTERNAL INTERRUPT CONFIGURE REGISTER 2

Offset: 0x268			Register Name: PG_EINT_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:12	/	/	/
[4i+3:4i] (i=0~2)	R/W	0	EINT_CFG External INTn Mode (n = 16~18) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

3.19.3.97. PG EXTERNAL INTERRUPT CONFIGURE REGISTER 3

Offset: 0x26C			Register Name: PG_EINT_CFG3 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.19.3.98. PG EXTERNAL INTERRUPT CONTROL REGISTER

Offset: 0x270			Register Name: PG_EINT_CTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:19	/	/	/
[n] (n=0~18)	R/W	0	EINT_CTL External INTn Enable (n = 0~18) 0: Disable 1: Enable

3.19.3.99. PG EXTERNAL INTERRUPT STATUS REGISTER

Offset: 0x274			Register Name: PG_EINT_STATUS Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:19	/	/	/
[n] (n=0~18)	R/W	0	EINT_STATUS External INTn Pending Bit (n = 0~18) 0: No IRQ pending 1: IRQ pending Write '1' to clear

3.19.3.100. PG EXTERNAL INTERRUPT DEBOUNCE REGISTER

Offset: 0x278			Register Name: PG_EINT_DEB Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:7	/	/	/
6:4	R/W	0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32Khz 1: HOSC 24Mhz

3.20. PORT CONTROLLER(CPUs-PORT)

3.20.1. OVERVIEW

The chip has 2 ports for multi-functional input/out pins. They are:

- Port L(PL): 9 input/output port
- PortM(PM) :8 input/output port

For various system configurations, these ports can be easily configured by software. All these ports can be configured as GPIO if multiplexed functions not used. The external PIO interrupt sources are supported and interrupt mode can be configured by software.

3.20.2. PORT REGISTER LIST

Module Name	Base Address
PIO	0x01F02C00

Register Name	Offset	Description
Pn_CFG0	n*0x24+0x00	Port n Configure Register 0 (n from 0 to 1)
Pn_CFG1	n*0x24+0x04	Port n Configure Register 1 (n from 0 to 1)
Pn_CFG2	n*0x24+0x08	Port n Configure Register 2 (n from 0 to 1)
Pn_CFG3	n*0x24+0x0C	Port n Configure Register 3 (n from 0 to 1)
Pn_DAT	n*0x24+0x10	Port n Data Register (n from 0 to 1)
Pn_DRV0	n*0x24+0x14	Port n Multi-Driving Register 0 (n from 0 to 1)
Pn_DRV1	n*0x24+0x18	Port n Multi-Driving Register 1 (n from 0 to 1)
Pn_PUL0	n*0x24+0x1C	Port n Pull Register 0 (n from 0 to 1)
Pn_PUL1	n*0x24+0x20	Port n Pull Register 1 (n from 0 to 1)
Pn_INT_CFG0	0x200+n*0x20+0x00	PIO Interrrupt Configure Register 0
Pn _INT_CFG1	0x200+n*0x20+0x04	PIO Interrrupt Configure Register 1
Pn _INT_CFG2	0x200+n*0x20+0x08	PIO Interrrupt Configure Register 2

Pn _INT_CFG3	0x200+n*0x20+0x0C	PIO Interrrupt Configure Register 3
Pn _INT_CTL	0x200+n*0x20+0x10	PIO Interrupt Control Register
Pn _INT_STA	0x200+n*0x20+0x14	PIO Interrupt Status Register
Pn _INT_DEB	0x200+n*0x20+0x18	PIO Interrupt Debounce Register

3.20.3. PORT REGISTER DESCRIPTION

3.20.3.1. PL CONFIGURE REGISTER 0

Offset: 0x00			Register Name: PL_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0	PL7_SELECT 000: Input 001: Output 010:S_PL_EINT2 011: S_JTAG_DO 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	/	/	/
26:24	R/W	0	PL6_SELECT 000: Input 001: Output 010:S_PL_EINT1 011: S_JTAG_CK 100: Reserved 101: Reserved 110: Reserved 111: CSI1_D6
23	/	/	/
22:20	R/W	0	PL5_SELECT 000: Input 001: Output 010:S_PL_EINT0 011: S_JTAG_MS 100: Reserved 101: Reserved 110: Reserved 111: Reserved

19	/	/	/
18:16	R/W	0	PL4_SELECT 000: Input 001: Output 010:S_IR_RX 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
15	/	/	/
14:12	R/W	0	PL3_SELECT 000: Input 001: Output 010:S_UART_RX 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	/	/	/
10:8	R/W	0	PL2_SELECT 000: Input 001: Output 010:S_UART_TX 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
7	/	/	/
6:4	R/W	0	PL1_SELECT 000: Input 001: Output 010:S_TWI_SDA 011: S_P2TWI_SDA 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	/	/	/
2:0	R/W	0	PL0_SELECT 000: Input 001: Output 010:S_TWI_SCK 011: S_P2TWI_SCK 100: Reserved 101: Reserved

			110: Reserved	111: Reserved

3.20.3.2. PL CONFIGURE REGISTER 1

Offset: 0x04			Register Name: PL_CFG1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:3	/	/	/
2:0	R/W	0	PL8_SELECT 000: Input 001: Output 010:S_PL_EINT3 011: S_JTAG_DI 100:Reserved 101: Reserved 110: Reserved 111: Reserved

3.20.3.3. PL CONFIGURE REGISTER 2

Offset: 0x08			Register Name: PL_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.20.3.4. PL CONFIGURE REGISTER 3

Offset: 0x0C			Register Name: PL_CFG3 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.20.3.5. PL DATA REGISTER

Offset: 0x10			Register Name: PL_DAT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**

31:9	/	/	/
8:0	R/W	0	PL_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.20.3.6. PL MULTI-DRIVING REGISTER 0

Offset: 0x14			Register Name: PL_DRV0 Default Value: 0x0001_5555
Bit	**Read/Write**	**Default**	**Description**
31:18	/	/	/
[2i+1:2i] (i=0~8)	R/W	0x1	PL_DRV PL[n] Multi-Driving Select (n = 0~8) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.20.3.7. PL MULTI-DRIVING REGISTER 1

Offset: 0x18			Register Name: PL_DRV1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.20.3.8. PL PULL REGISTER 0

Offset: 0x1C			Register Name: PL_PULL0 Default Value: 0x0000_0005
Bit	**Read/Write**	**Default**	**Description**
31:18	/	/	/
[2i+1:2i]	R/W	0x0	PL_PULL

(i=0~8)			PL[n] Pull-up/down Select (n = 0~8) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.20.3.9. PL PULL REGISTER 1

Offset: 0x20			Register Name: PL_PULL1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.20.3.10. PM CONFIGURE REGISTER 0

Offset: 0x24			Register Name: PM_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	0	PM7_SELECT 000: Input 001: Output 010:S_PM_EINT7 011: RTC_CLKO 100: Reserved 101: Reserved 110: Reserved 111: Reserved
27	/	/	/
26:24	R/W	0	PM6_SELECT 000: Input 001: Output 010:S_PM_EINT6 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
23	/	/	/
22:20	R/W	0	PM5_SELECT 000: Input 001: Output 010:S_PM_EINT5 011: Reserved

			100: Reserved 101: Reserved 110: Reserved 111: Reserved
19	/	/	/
18:16	R/W	0	PM4_SELECT 000: Input 001: Output 010:S_PM_EINT4 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
15	/	/	/
14:12	R/W	0	PM3_SELECT 000: Input 001: Output 010:S_PM_EINT3 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
11	/	/	/
10:8	R/W	0	PM2_SELECT 000: Input 001: Output 010:S_PM_EINT2 011: 1WIRE 100: Reserved 101: Reserved 110: Reserved 111: Reserved
7	/	/	/
6:4	R/W	0	PM1_SELECT 000: Input 001: Output 010:S_PM_EINT1 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved
3	/	/	/
2:0	R/W	0	PM0_SELECT 000: Input 001: Output

			010:S_PM_EINT0 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved

3.20.3.11. PM CONFIGURE REGISTER 1

Offset: 0x28			Register Name: PM_CFG1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.20.3.12. PM CONFIGURE REGISTER 2

Offset: 0x2C			Register Name: PM_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.20.3.13. PM CONFIGURE REGISTER 3

Offset: 0x30			Register Name: PM_CFG3 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.20.3.14. PM DATA REGISTER

Offset: 0x34			Register Name: PM_DAT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7:0	R/W	0	PM_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the

			corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.20.3.15. PM MULTI-DRIVING REGISTER 0

Offset: 0x38			Register Name: PM_DRV0 Default Value: 0x0000_5555
Bit	**Read/Write**	**Default**	**Description**
31:16	/	/	/
[2i+1:2i] (i=0~7)	R/W	0x1	PM_DRV PM[n] Multi-Driving Select (n = 0~7) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.20.3.16. PM MULTI-DRIVING REGISTER 1

Offset: 0x3C			Register Name: PM_DRV1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.20.3.17. PM PULL REGISTER 0

Offset: 0x40			Register Name: PM_PULL0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:16	/	/	/
[2i+1:2i] (i=0~7)	R/W	0x0	PM_PULL PM[n] Pull-up/down Select (n = 0~7) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.20.3.18. PM PULL REGISTER 1

Offset: 0x44			Register Name: PM_PULL1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.20.3.19. PL EXTERNAL INTERRUPT CONFIGURE REGISTER 0

Offset: 0x200			Register Name: PL_EINT_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[4i+3:4i] (i=0~7)	R/W	0	EINT_CFG External INTn Mode (n = 0~7) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

3.20.3.20. PL EXTERNAL INTERRUPT CONFIGURE REGISTER 1

Offset: 0x204			Register Name: PL_EINT_CFG1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:4	/	/	/
[4i+3:4i] (i=0)	R/W	0	EINT_CFG External INTn Mode (n = 8) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level

			0x4: Double Edge (Positive/ Negative) Others: Reserved

3.20.3.21. PL EXTERNAL INTERRUPT CONFIGURE REGISTER 2

Offset: 0x208			Register Name: PL_EINT_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.20.3.22. PL EXTERNAL INTERRUPT CONFIGURE REGISTER 3

Offset: 0x20C			Register Name: PL_EINT_CFG3 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.20.3.23. PL EXTERNAL INTERRUPT CONFIGURE REGISTER

Offset: 0x210			Register Name: PL_EINT_CTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:9	/	/	/
[n] (n=0~8)	R/W	0	EINT_CTL External INTn Enable (n = 0~8) 0: Disable 1: Enable

3.20.3.24. PL EXTERNAL INTERRUPT STATUS REGISTER

Offset: 0x214			Register Name: PL_EINT_STATUS Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:9	/	/	/

[n] (n=0~8)	R/W	0	EINT_STATUS External INTn Pending Bit (n = 0~8) 0: No IRQ pending 1: IRQ pending Write '1' to clear

3.20.3.25. PL EXTERNAL INTERRUPT DEBOUNCE REGISTER

Offset: 0x218			Register Name: PL_EINT_DEB Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:7	/	/	/
6:4	R/W	0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32Khz 1: HOSC 24Mhz

3.20.3.26. PM EXTERNAL INTERRUPT CONFIGURE REGISTER 0

Offset: 0x220			Register Name: PM_EINT_CFG0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[4i+3:4i] (i=0~7)	R/W	0	EINT_CFG External INTn Mode (n = 0~7) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level

			0x4: Double Edge (Positive/ Negative) Others: Reserved

3.20.3.27. PM EXTERNAL INTERRUPT CONFIGURE REGISTER 1

Offset: 0x224			Register Name: PM_EINT_CFG1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.20.3.28. PM EXTERNAL INTERRUPT CONFIGURE REGISTER 2

Offset: 0x228			Register Name: PM_EINT_CFG2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.20.3.29. PM EXTERNAL INTERRUPT CONFIGURE REGISTER 3

Offset: 0x22C			Register Name: PM_EINT_CFG3 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

3.20.3.30. PM EXTERNAL INTERRUPT CONTROL REGISTER

Offset: 0x230			Register Name: PM_EINT_CTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
[n] (n=0~7)	R/W	0	EINT_CTL External INTn Enable (n = 0~7) 0: Disable 1: Enable

3.20.3.31. PM EXTERNAL INTERRUPT STATUS REGISTER

Offset: 0x234			Register Name: PM_EINT_STATUS Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
[n] (n=0~7)	R/W	0	EINT_STATUS External INTn Pending Bit (n = 0~7) 0: No IRQ pending 1: IRQ pending Write '1' to clear it

3.20.3.32. PM EXTERNAL INTERRUPT DEBOUNCE REGISTER

Offset: 0x238			Register Name: PM_EINT_DEB Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:7	/	/	/
6:4	R/W	0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32Khz 1: HOSC 24Mhz

4 MEMORY

This chapter describes the memory system of A31 from two sides:

- SDRAM controller
- NAND Flash controller

4.1. SDRAM CONTROLLER

4.1.1. OVERVIEW

The SDRAM Controller (DRAMC) provides a simple, flexible, burst-optimized interface to all industy-standard Low Power DDR1/2, normal DDR2 SDRAM and DDR3 SDRAM. It supports up to a 16G bits memory address space.

The DRAMC automatically handles memory management, initialization, and refresh operations. It gives the host CPU a simple command interface, hiding details of the required address, page, and burst handling procedures. All memory parameters are runtime-configurable, including timing, memory setting, SDRAM type, and Extended-Mode-Register settings.

The DRAMC features:

- Comply with LPDDR1/2, DDR2, DDR3 SDRAM JEDEC specification
- Support different memory device's power voltage of 1.2V, 1.35V, 1.5V and 1.8V
- Support memory capacity up to 16G bits(2G Bytes)
- Support 2 chip select signals per channel
- Support 16 address lines and 3 bank address lines per channel
- Support 2 SDRAM controllers
- Support LPDDR1/2, DDR2, DDR3 SDRAM
- Support 8/16/32 bits bus width per dram chip

4.1.2. SDRAM MASTER LIST

MASTER ID	MASTER NAME	BUS TYPE	MASTER DESCRIPTION
0	CPUx		

1	GPU		
2	GPU		
3	/		
4	/		
5	ATH		
6	EMAC		
7	SDC0		
8	SDC1		
9	SDC2		
10	SDC3		
11	USB		
12	/		
13	/		
14	/		
15	NFC1		
16	DMAC		
17	VE		
18	MP		
19	NFC0		
20	DRC0		
21	DRC1		
22	DEU0		
23	DEU1		
24	BE0		
25	FE0		
26	BE1		
27	FE1		
28	CSI0		
29	CSI1		

30	TS		
31	/		

Table 4-1 SDRAM Master List

4.2. NAND FLASH CONTROLLER

4.2.1. OVERVIEW

The NAND Flash Controller in A31 platform supports all SLC/MLC/TLC nand flash memory available in current market, and new flash can be supported by software re-configuration.

The NAND flash controller supports up to two channels to speedup NAND read and write operations. It also features On-the-fly error correction code (ECC) to enhance reliability, which can be disabled by software configuration. BCH is implemented, which can detect and correct up to 64 bits error per 512 or 1024 bytes data. The on-chip ECC and parity checking circuitry of NFC frees CPU for other tasks.

Data can be transferred by DMA or by CPU memory-mapped IO method. The NFC provides automatic timing control for reading or writing external flash. It also maintains proper relativity for CLE, CE# and ALE control signal lines. Up to three serial read access modes are supported: mode 0 is the conventional serial access, mode 1 is for EDO type, and mode 2 is for extension EDO type. NFC can monitor the status of R/B# signal line. Block management and wear leveling management are implemented in software.

The NFC features:

- Comply with ONFI 2.3 & toggle 1.0
- Support up to 2 channels
- Support up to 64bit ECC per 512B or 1024B
- Support 8bit/16bit data bus width
- Support 1K/2K/4K/8K/16K page size
- Support up to 4 CE and 2 RB
- Support hardware randomize engine
- Support booting from nand flash
- Support SLC/MLC/TLC nand and EF-NAND
- Support sdr/ddr nand interface
- Two 256x32bit RAM for pipeline procession.

4.2.2. NAND FLASH BLOCK DIAGRAM

The NAND Flash Controller (NFC) system block diagram is shown below:

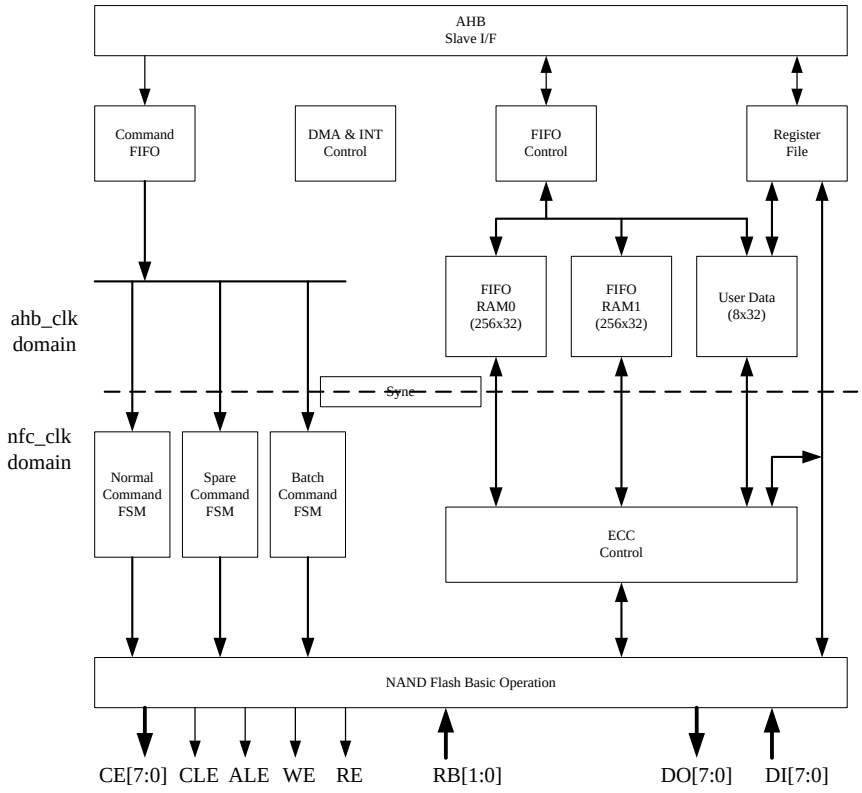


Figure 4-1 NAND Flash Block Diagram

4.2.3. NAND FLASH CONTROLLER TIMING DIAGRAM

Typically, there are two serial access methods: one is conventional method where data is fetched at the rise edge of NFC_RE# signal line, the other is EDO type where data is fetched at the next fall edge of NFC_RE# signal line.

Conventional Serial Access after Read Cycle (SAM0)

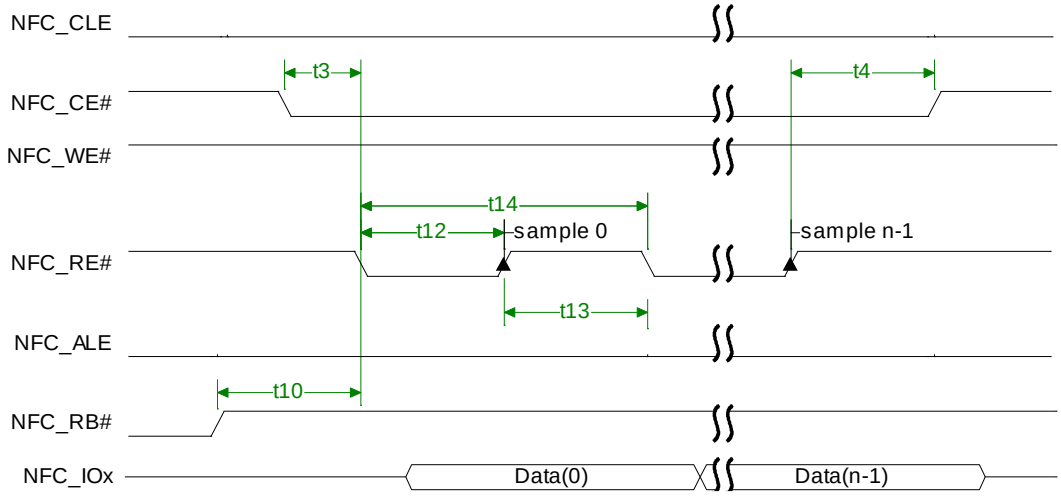


Figure 4-2 Conventional Serial Access Cycle Diagram (SAM0)

EDO type Serial Access after Read Cycle (SAM1)

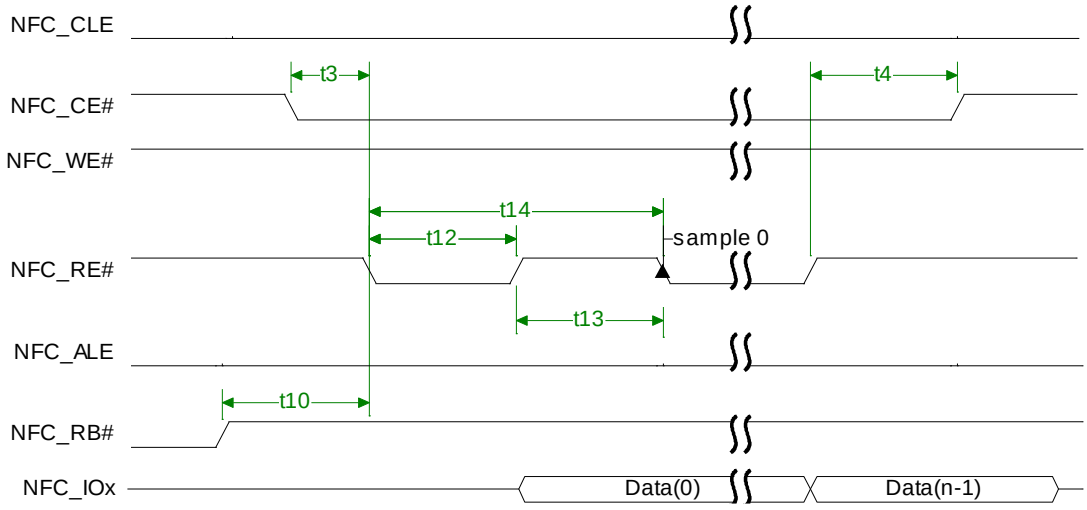


Figure 4-3 EDO type Serial Access after Read Cycle (SAM1)

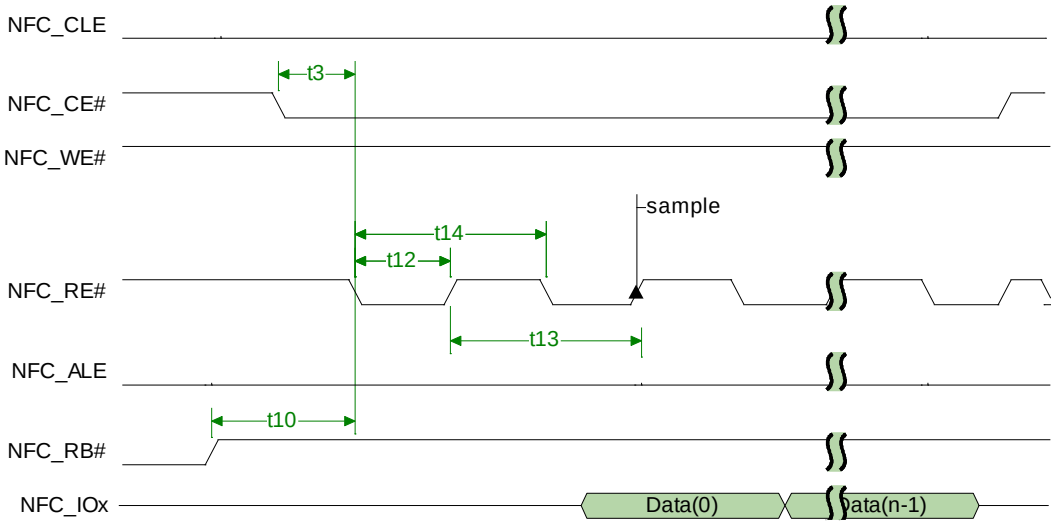


Figure 4-4 Extending EDO type Serial Access Mode (SAM2)

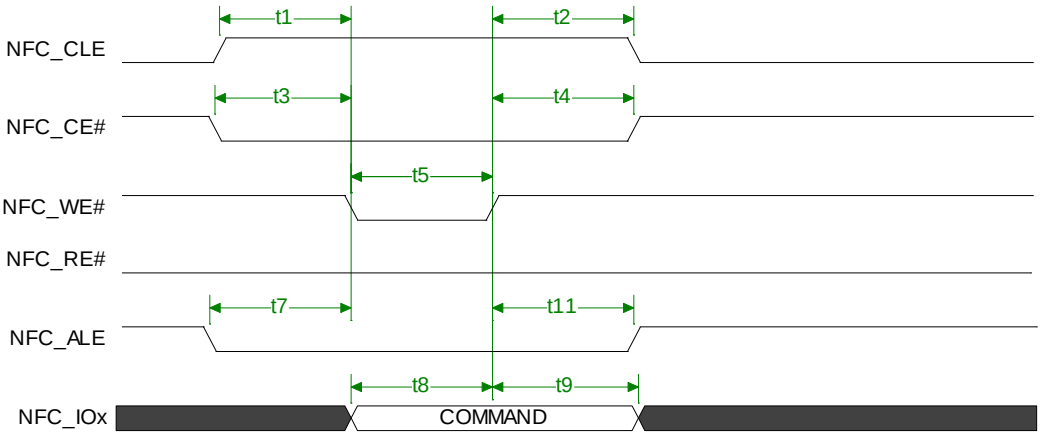


Figure 4-5 Command Latch Cycle

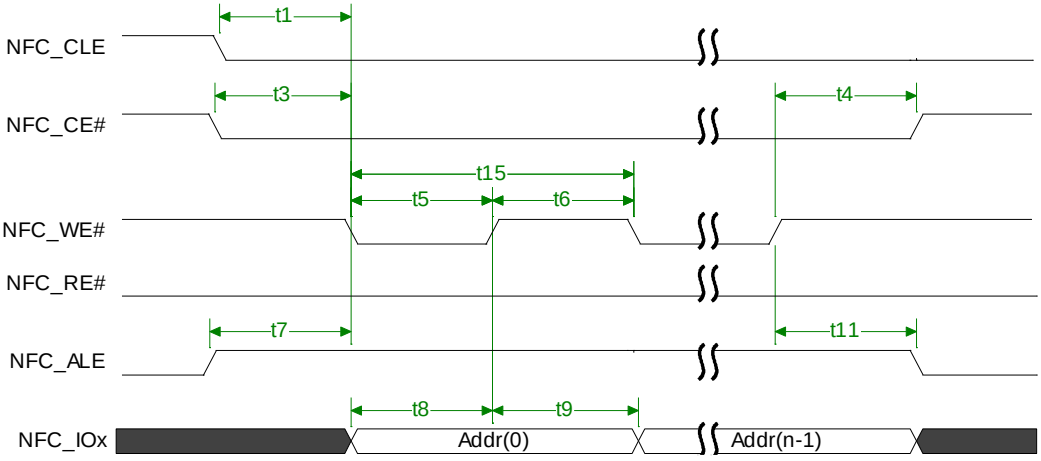


Figure 4-6 Address Latch Cycle

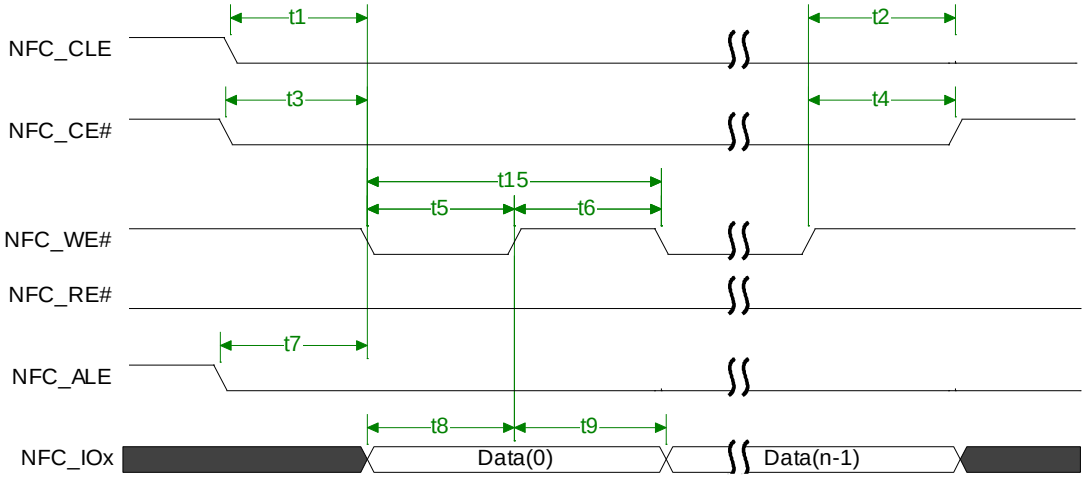


Figure 4-7 Write Data to Flash Cycle

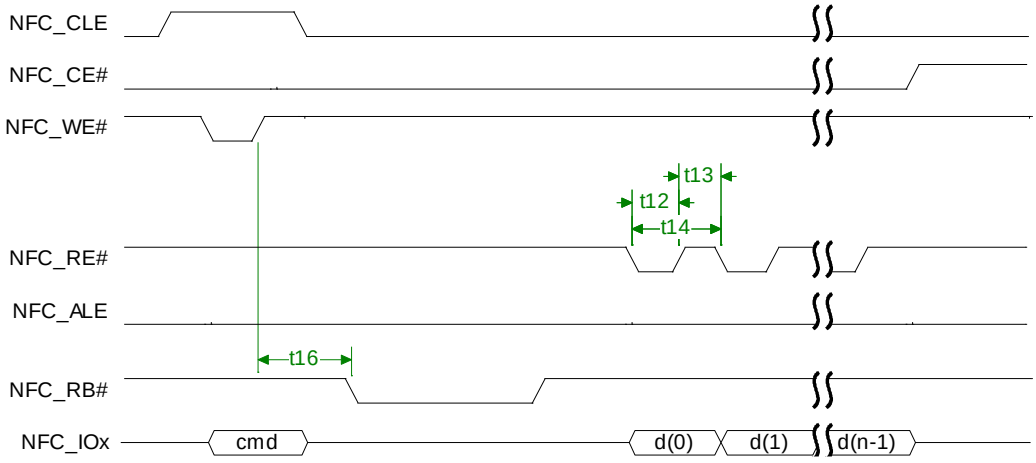


Figure 4-8 Waiting R/B# ready Diagram

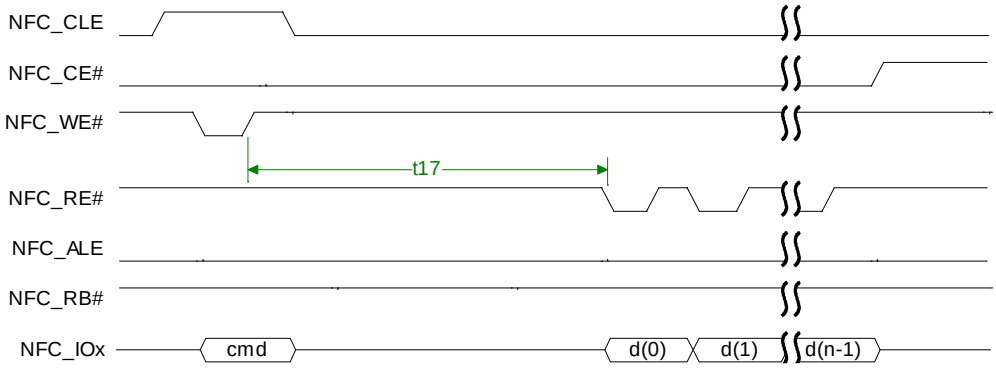


Figure 4-9 WE# high to RE# low Timing Diagram

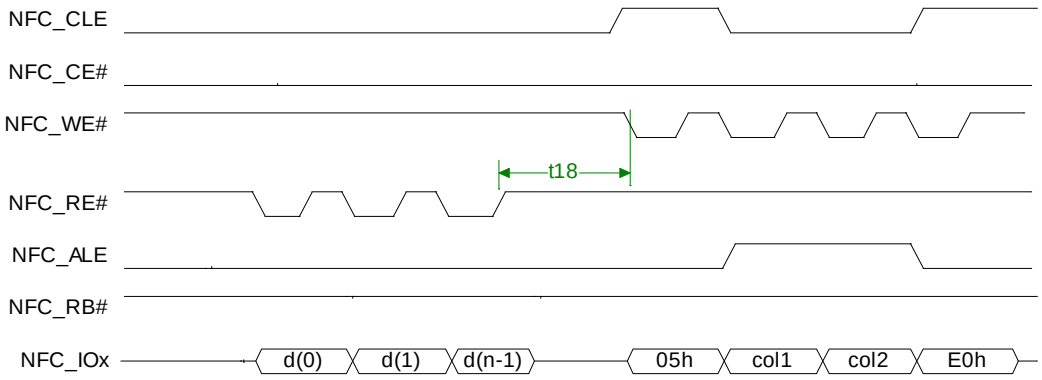


Figure 4-10 RE# high to WE# low Timing Diagram

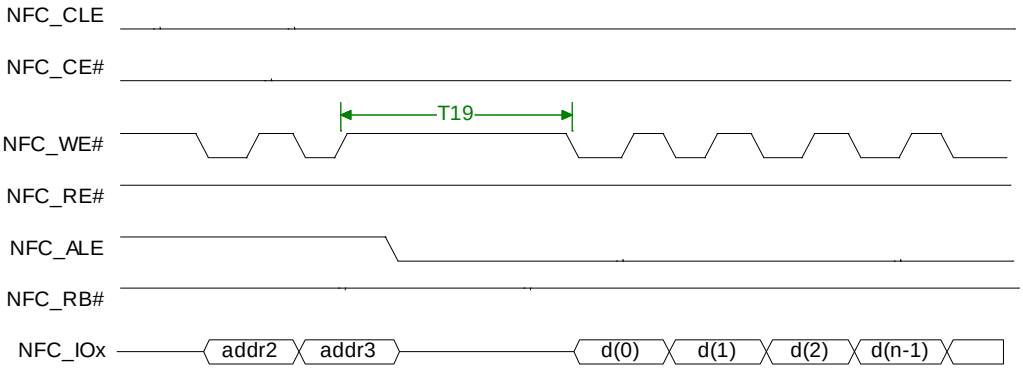


Figure 4-11 Address to Data Loading Timing Diagram

Timing Cycle List

ID	Parameter	Timing	Notes
T1	NFC_CLE setup time	T	
T2	NFC_CLE hold time	T	
T3	NFC_CE setup time	T	
T4	NFC_CE hold time	T	
T5	NFC_WE# pulse width	T	
T6	NFC_WE# hold time	T	
T7	NFC_ALE setup time	T	
T8	Data setup time	T	

T9	Data hold time	T	
T10	Ready to NFC_RE# low	3T	
T11	NFC_ALE hold time	T	
T12	NFC_RE# pulse width	T	
T13	NFC_RE# hold time	T	
T14	Read cycle time	2T	
T15	Write cycle time	2T	
T16	NFC_WE# high to R/B# busy	tWB	Specified by timing configure register(NFC_TIMING_CFG)
T17	NFC_WE# high to NFC_RE# low	tWHR	Specified by timing configure register(NFC_TIMING_CFG)
T18	NFC_RE# high to NFC_WE# low	tRHW	Specified by timing configure register(NFC_TIMING_CFG)
T19	Address to Data Loading time	tADL	Specified by timing configure register(NFC_TIMING_CFG)

Notes: T is the clock period duration of NFC_CLK (x2).

4.2.4. NAND FLASH CONTROLLER OPERATION GUIDE

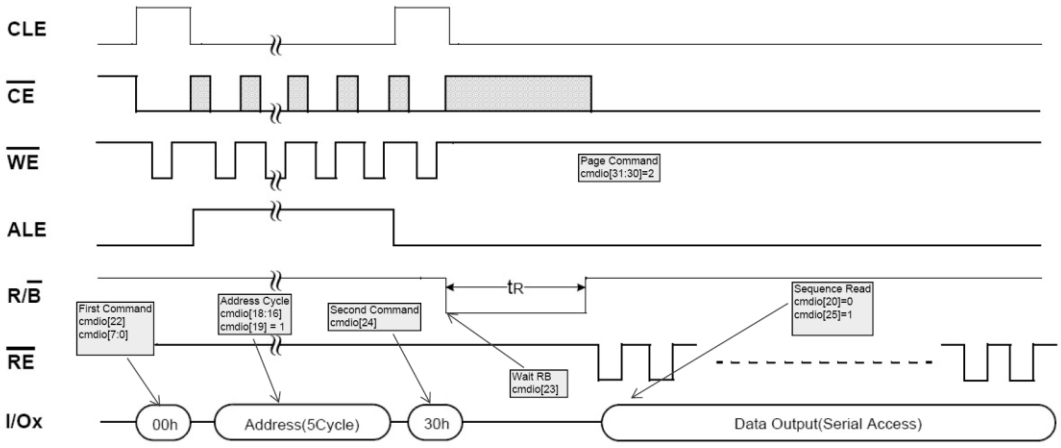


Figure 4-12 Page Read Command Diagram

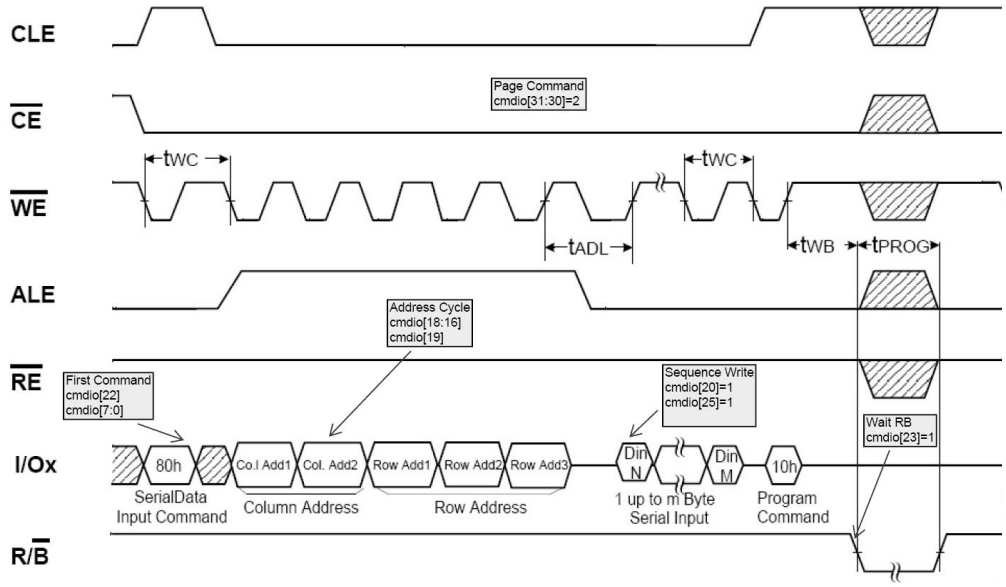


Figure 4-13 Page Program Diagram

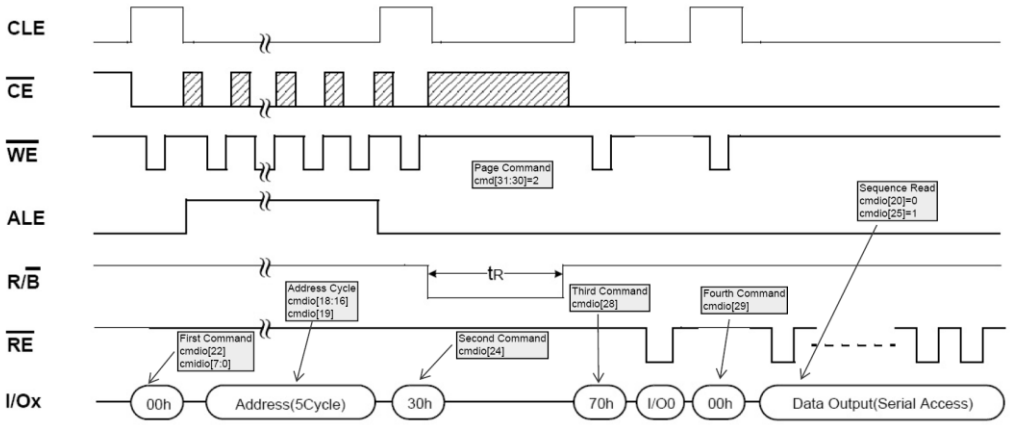


Figure 4-14 EF-NAND Page Read Diagram

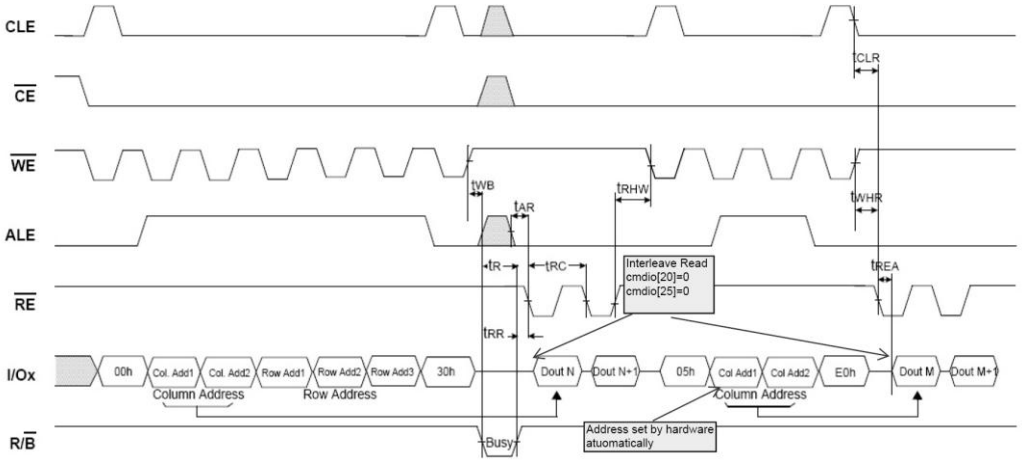


Figure 4-15 Interleave Page Read Diagram

5 GRAPHIC

This chapter introduces the graphic processing ability of A31 from following two perspectives:

- GPU
- MIXER PROCESSOR

5.1. GPU

A31 adopts the powerful SGX544 GPU that with eight logic cores. It features:

- Support Open GL ES 2.0 /Open VG 1.1 / Open CL 1.1 / DX 9.3 standard
- Polygon ability up to 100M/s, pixel ability up to 3G/s

5.2. MIXER PROCESSOR

5.2.1. OVERVIEW

The Mixer Processor features:

- Supported Color format
  - ARGB 8888/4444/1555
  - RGB565
  - MONO 1/2/4/8 bpp
  - Palette 1/2/4/8 bpp (input only)
  - YUV 444/422/420
- Support any format conversion
- Support buffer block size up to 8192x8192 pixels
- Support memory scan order option
- Support clipping
- ROP2
  - Line / Rectangle / Point
  - Block fill
- ROP3
  - bitblt
  - patblt
  - stretchblt
- ROP4
  - maskblt
- 90/180/270 rotation degree
- Support Mirror
- Alpha blending
  - Support Plane & Pixel alpha

- Output alpha configurable

- Support color key
- Scaling
  - 4x4 taps
  - 32 phase
- Support color space conversion
- Support command queue

5.2.2. MIXER PROCESSOR BLOCK DIAGRAM

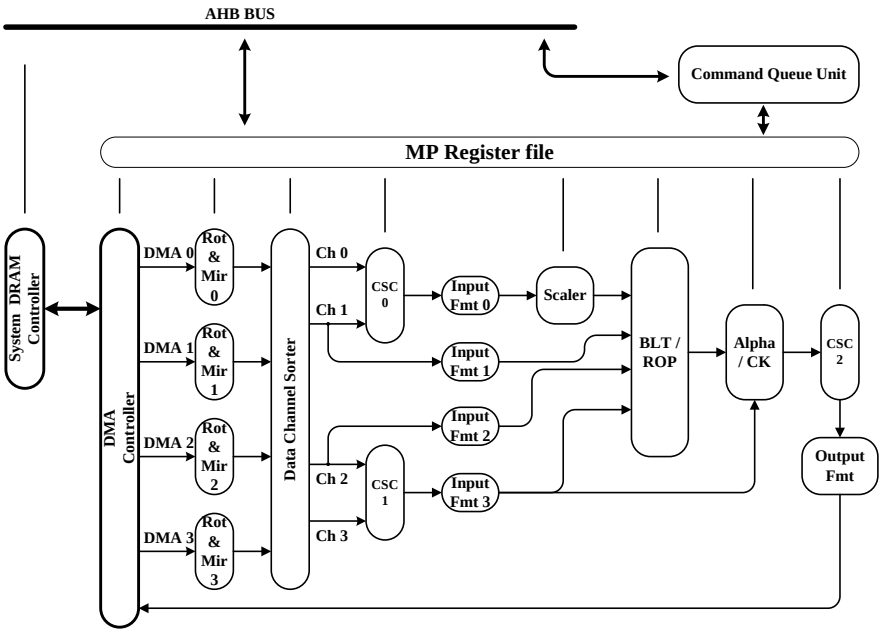


Figure 5-1 Mixer Processor Block Diagram

5.2.3. MIXER PROCESSOR REGISTER LIST

Module name	Base address

MP	0x01e80000

Register name	Offset	Description
MP_CTL_REG	0x0	Mixer control register
MP_STS_REG	0x4	Mixer Status register
MP_IDMAGLBCTL_REG	0x8	Input DMA globe control register
MP_IDMA_H4ADD_REG	0xC	Input DMA start address high 4bits register
MP_IDMA_L32ADD_REG	0x10 – 0x1C	Input DMA start address low 32bits register
MP_IDMALINEWIDTH_REG	0x20 – 0x2C	Input DMA line width register
MP_IDMASIZE_REG	0x30 – 0x3C	Input DMA memory block size register
MP_IDMACOOR_REG	0x40 – 0x4C	Input DMA memory block coordinate control register
MP_IDMASET_REG	0x50 – 0x5C	Input DMA setting register
MP_IDMAFILLCOLOR_REG	0x60 – 0x6C	Input DMA fill-color register
MP_CSC0CTL_REG	0x74	Color space converter 0 control register
MP_CSC1CTL_REG	0x78	Color space converter 1 control register
MP_SCACTL_REG	0x80	Scaler control register
MP_SCAOUTSIZE_REG	0x84	Scaling output size register
MP_SCAHORFCT_REG	0x88	Scaler horizontal scaling factor register
MP_SCAVERFCT_REG	0x8C	Scaler vertical scaling factor register
MP_SCAHORPHASE_REG	0x90	Scaler horizontal start phase setting register
MP_SCAVERPHASE_REG	0x94	Scaler vertical start phase setting register
MP_ROPCTL_REG	0xB0	ROP control register
MP_ROPIDX0CTL_REG	0xB8	ROP channel 3 index 0 control table setting register
MP_ROPIDX1CTL_REG	0xBC	ROP channel 3 index 1 control table setting register
MP_ALPHACKCTL_REG	0xC0	Alpha / Color key control register
MP_CKMIN_REG	0xC4	Color key min color register

MP_CKMAX_REG	0xC8	Color key max color register
MP_ROPOUTFILLCOLOR_REG	0xCC	Fill color of ROP output setting register
MP_CSC2CTL_REG	0xD0	Color space converter 2 control register
MP_OUTCTL_REG	0xE0	Output control register
MP_OUTSIZE_REG	0xE8	Output size register
MP_OUTH4ADD_REG	0xEC	Output address high 4bits register
MP_OUTL32ADD_REG	0xF0 – 0xF8	Output address low 32bits register
MP_OUTLINEWIDTH_REG	0x100 – 0x108	Output line width register
MP_OUTALPHACTL_REG	0x120	Output alpha control register
MP_MBCTL_REG	0x130 – 0x13c	MB control register
MP_ICSCYGCOEF_REG	0x180 – 0x188	CSC0/1 Y/G coefficient register
MP_ICSCYGCONS_REG	0x18C	CSC0/1 Y/G constant register
MP_ICSCURCOEF_REG	0x190 – 0x198	CSC0/1 U/R coefficient register
MP_ICSCURCONS_REG	0x19C	CSC0/1 U/R constant register
MP_ICSCVBCOEF_REG	0x1A0 – 0x1A8	CSC0/1 V/B coefficient register
MP_ICSCVBCONS_REG	0x1AC	CSC0/1 V/B constant register
MP_OCSCYGCOEF_REG	0x1C0 – 0x1C8	CSC2 Y/G coefficient register
MP_OCSCYGCONS_REG	0x1CC	CSC2 Y/G constant register
MP_OCSCURCOEF_REG	0x1D0 – 0x1D8	CSC2 U/R coefficient register
MP_OCSCURCONS_REG	0x1DC	CSC2 U/R constant register
MP_OCSCVBCOEF_REG	0x1E0 – 0x1E8	CSC2 V/B coefficient register
MP_OCSCVBCONS_REG	0x1EC	CSC2 V/B constant register
CMDQUECTL_REG	0x140	Command queue control register
CMDQUESTS _REG	0x148	Command queue status register
CMDQUEADD_REG	0x14c	Command queue storage start address register
Memories		
0x200 – 0x27C	Scaling horizontal filtering coefficient RAM block	
0x280 – 0x2FC	Scaling vertical filtering coefficient RAM block	
0x400 – 0x7FF	Palette table	

5.2.4. MIXER PROCESSOR REGISTER DESCRIPTION

5.2.4.1. MIXER CONTROL REGISTER

Offset: 0x0			Register Name: MP_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0	**HWERRIRQ_EN** Hardware error IRQ enable control 0:disable 1:enable
8	R/W	0	**FINISHIRQ_EN** Mission finish IRQ enable control 0:disable 1:enable
7:2	/	/	/
1	R/W	0	**START_CTL** Start control If the bit is set, the module will start 1 frame operation and stop auto.
0	R/W	0	**MP_EN** Enable control 0:disable 1:enable

5.2.4.2. MIXER STATUS REGISTER

Offset: 0x4			Register Name: MP_STS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/

13	R	0	**HWERR_FLAG** Hardware error status
12	R	0	**BUSY_FLAG** Module working status 0:idle 1:running
11:10	/	/	/
9	R/W	0	**HWERRIRQ_FLAG** Hardware error IRQ It will be set when hardware error occur, and cleared by writing 1.
8	R/W	0	**FINISHIRQ_FLAG** Mission finish IRQ It will be set when 1 frame operation accomplished, and cleared by writing 1.
7:0	/	/	/

5.2.4.3. INPUT DMA GLOBE CONTROL REGISTER

Offset: 0x8			**Register Name: MP_IDMAGLBCTL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0	**MEMSCANORDER** Memory scan order selection 0: Top to down Left to right 1: Top to down Right to left

			2: Down to top Left to right 3: Down to top Right to left Notes: ----Four input DMA channel use the same scan rule. ----The each output DMA channel should match the same memory scan order rule with the input DMA channel.
7:0	/	/	/

5.2.4.4. INPUT DMA START ADDRESS HIGH 4BITS REGISTER

Offset: 0xC			Register Name: MP_IDMA_H4ADD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0	**IDMA3_H4ADD** iDMA3 High 4bits address in bits
23:20	/	/	/
19:16	R/W	0	**IDMA2_H4ADD** iDMA2 High 4bits address in bits
15:12	/	/	/
11:8	R/W	0	**IDMA1_H4ADD** iDMA1 High 4bits address in bits
7:4	/	/	/

3:0	R/W	0	**IDMA0_H4ADD** iDMA0 High 4bits address in bits

5.2.4.5. INPUT DMA START ADDRESS LOW 32BITS REGISTER

Offset: **iDMA0:0x10** **iDMA1:0x14** **iDMA2:0x18** **iDMA3:0x1C**			**Register Name: MP_IDMA_L32ADD_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0	**IDMA_L32ADD** iDMA Low 32bits address in bits

5.2.4.6. INPUT DMA LINE WIDTH REGISTER

Offset: **iDMA0:0x20** **iDMA1:0x24** **iDMA2:0x28** **iDMA3:0x2C**			**Register Name: MP_IDMALINEWIDTH_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0	**IDMA_LINEWIDTH** iDMA Line width in bits

5.2.4.7. INPUT DMA MEMORY BLOCK SIZE REGISTER

Offset: **iDMA0:0x30**	**Register Name: MP_IDMASIZE_REG**

iDMA1:0x34 iDMA2:0x38 iDMA3:0x3C			
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0	**IDMA_HEIGHT** Memory block height in pixels The height = The value of these bits adds 1
15:13	/	/	/
12:0	R/W	0	**IDMA_WIDTH** Memory block width in pixels The width = The value of these bits adds 1

5.2.4.8. INPUT DMA MEMORY BLOCK COORDINATE CONTROL REGISTER

Offset: iDMA0:0x40 iDMA1:0x44 iDMA2:0x48 iDMA3:0x4C			Register Name: MP_IDMACOOR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0	**IDMA_YCOOR** Y coordinate Y is the left-top y coordinate of layer on output window in pixels The Y represents the two's complement
15:0	R/W	0	**IDMA_XCOOR** X coordinate X is left-top x coordinate of the layer on output window in pixels The X represents the two's complement

5.2.4.9. INPUT DMA SETTING REGISTER

Offset: iDMA0:0x50 iDMA1:0x54 iDMA2:0x58 iDMA3:0x5C			Register Name: MP_IDMASET_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0	**IDMA_GLBALPHA** Globe alpha value
23	/	/	/
22	R/W	0	**MBFMT** Micro block format enable 0: disable 1: enable
21:20	R/W	0	**MBSIZE** Micro block size in bytes 0: 16*16 1: 32*32 2: 64*64 3: 128*128
19:17	/	/	/
16	R/W	0	**IDMA_FCMODEN** Fill color mode enable control 0: disable 1: enable
15:12	R/W	0	**IDMA_PS** Input data pixel sequence Refer to input pixel sequence table
11:8	R/W	0	**IDMA_FMT**

			Input data format 0x0:32bpp – A8R8G8B8 or interleaved AYUV8888 0x1:16bpp – A4R4G4B4 0x2:16bpp – A1R5G5B5 0x3:16bpp – R5G6B5 0x4:16bpp – interleaved YUV422 0x5:16bpp – U8V8 0x6:8bpp – Y8 0x7:8bpp – MONO or palette 0x8:4bpp – MONO or palette 0x9:2bpp – MONO or palette 0xa:1bpp – MONO or palette Other: reserved Notes: if the input data format is 16 or 32bpp, and the work mode is palette mode, only the low 8 bits input data are valid.
7:4	R/W	0	**IDMA_ROTMIRCTL** Rotation and mirroring control 0:normal 1:X 2:Y 3:XY 4:A 5:AX 6:AY 7:AXY Other: reserved
3:2	R/W	0	**IDMA_ALPHACTL** Alpha control

			0:Ignore Output alpha value = pixels alpha, if no pixel alpha, the alpha value equal 0xff 1:Globe alpha enable Ignore pixel alpha value Output alpha value = globe alpha value 2: Globe alpha mix pixel alpha Output alpha value = globe alpha value * pixels alpha value 3:Reserved Notes: the output alpha value here means the input alpha value of the ALU following the DMA controller.
1	R/W	0	**IDMA_WORKMOD** Work mode selection 0: normal mode (non-palette mode) 1: palette mode
0	R/W	0	**IDMA_EN** Input DMA enable control 0:disable input DMA channel, the respective fill-color value will stead of the input data. 1:enable

5.2.4.10. INPUT DMA FILL-COLOR REGISTER

Offset: **iDMA0:0x60** **iDMA1:0x64** **iDMA2:0x68**	**Register Name: MP_IDMAFILLCOLOR_REG**

iDMA3:0x6C			
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0	**IDMA_FCALPHA** Alpha
23:16	R/W	0	**IDMA_FCRED** Red
15:8	R/W	0	**IDMA_FCGREEN** Green
7:0	R/W	0	**IDMA_FCBLUE** Blue

5.2.4.11. COLOR SPACE CONVERTER 0 CONTROL REGISTER

Offset: 0x74			Register Name: MP_CSC0CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:4	R/W	0	**CSC0_DATAMOD** Data mode control 0: Interleaved AYUV8888 mode 1: Interleaved YUV422 mode In mode 0 and mode 1, only the channel 0 data path is valid for this module, the channel 1 data flow will by-pass the csc0 module, and direct to input formatter 1. 2:Planar YUV422 mode (UV combined only) 3:Planar YUV420 mode (UV combined only) 4:Planar YUV411 mode (UV combined only)

			In mode 2/3/4, following rule: ----In this mode, the output data of the input formatter 1 will be stead of the respective fill-color value.
3:1	/	/	/
0	R/W	0	**CSC0_EN** Enable control 0: Disable color space function, ignore the control setting, and the data flow will by-pass the module. 1: Enable color space converting function.

5.2.4.12. COLOR SPACE CONVERTER 1 CONTROL REGISTER

Offset: 0x78			**Register Name: MP_CSC1CTL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:4	R/W	0	**CSC1_DATAMOD** Data mode control 0: Interleaved AYUV8888 mode 1: Interleaved YUV422 mode In mode 0 and mode 1, only the channel 3 data path is valid for this module, the channel 2 data flow will by-pass the csc1 module, and direct to input formatter 2. 2:Planar YUV422 mode (UV combined only)

			3:Planar YUV420 mode (UV combined only) 4:Planar YUV411 mode (UV combined only) In mode 2/3/4, following rule: ----In this mode, the output data of the input formatter 2 will be stead of the respective fill-color value.
3:1	/	/	/
0	R/W	0	**CSC1_EN** Enable control 0: Disable color space function, ignore the control setting, and the data flow will by-pass the module. 1: Enable color space converting function.

5.2.4.13. SCALER CONTROL REGISTER

Offset: 0x80			**Register Name: MP_SCACTL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:4	R/W	0	**SCA_ALGSEL** Scaling algorithm selection 0: bi-cubic(4 taps in vertical and horizontal) 1: linear in vertical and bi-linear in horizontal(2 taps in vertical and 4 taps in horizontal) 2: extractive in vertical and bi-linear in horizontal(1 tap in vertical and 4 taps in horizontal) 3: reserved
3:1	/	/	/
0	R/W	0	**SCA_EN**

			Enable control 0: Disable scaler, ignore the whole scaling setting, and the data flow will by-pass the module. 1: Enable scaling function.

5.2.4.14. SCALING OUTPUT SIZE REGISTER

Offset: 0x84			Register Name: MP_SCAOUTSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0	**SCA_OUTHEIGHT** Output height The output height = The value of these bits add 1 The minimum output height is 8 pixels.
15:13	/	/	/
12:0	R/W	0	**SCA_OUTWIDTH** Output width The output width = The value of these bits add 1 The minimum output width is 16 pixels.

5.2.4.15. SCALER HORIZONTAL SCALING FACTOR REGISTER

Offset: 0x88			Register Name: MP_SCAHORFCT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0	**SCA_HORINTFCT** The integer part of the horizontal scaling ratio

			the horizontal scaling ratio = input width/output width
15:00	R/W	0	**SCA_HORFRAFCT** The fractional part of the horizontal scaling ratio the horizontal scaling ratio = input width/output width The input width is the memory block width of respective iDMA channel.

5.2.4.16. SCALER VERTICAL SCALING FACTOR REGISTER

Offset: 0x8C			**Register Name: MP_SCAVERFCT_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0	**SCA_VERINTFCT** The integer part of the vertical scaling ratio the vertical scaling ratio = input height/output height
15:00	R/W	0	**SCA_VERFRAFCT** The fractional part of the vertical scaling ratio the vertical scaling ratio = input height /output height The input height is the memory block height of respective iDMA channel.

5.2.4.17. SCALER HORIZONTAL START PHASE SETTING REGISTER

Offset: 0x90			**Register Name: MP_SCAHORPHASE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:00	R/W	0	**SCA_HORPHASE** Start phase in horizontal (complement)

			This value equals to start phase * 2^{16}

5.2.4.18. SCALER VERTICAL START PHASE SETTING REGISTER

Offset: 0x94			Register Name: MP_SCAVERPHASE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:00	R/W	0	**SCA_VERPHASE** Start phase in vertical (complement) This value equals to start phase * 2^{16}

5.2.4.19. ROP CONTROL REGISTER

Offset: 0xB0			Register Name: MP_ROPCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:14	R/W	0	**ROP_ALPHABYPASSSEL** ROP output Alpha channel selection 0: channel 0 1: channel 1 2: channel 2 3:reserved Notes: the bit is only valid in by-pass mode of Alpha channel
13:12	R/W	0	**ROP_REDBYPASSSEL** ROP output Red channel selection 0: channel 0 1: channel 1 2: channel 2 3:reserved

			Notes: the bit is only valid in by-pass mode of Red channel
11:10	R/W	0	**ROP_GREENBYPASSSEL** ROP output Green channel selection 0: channel 0 1: channel 1 2: channel 2 3:reserved Notes: the bit is only valid in by-pass mode of Green channel
9:8	R/W	0	**ROP_BLUEBYPASSSEL** ROP output Blue channel selection 0: channel 0 1: channel 1 2: channel 2 3:reserved Notes: the bit is only valid in by-pass mode of Blue channel
7	R/W	0	**ROP_ALPHABYPASSEN** ROP Alpha channel by-pass enable control 0:pass through 1:by-pass
6	R/W	0	**ROP_REDBYPASSEN** ROP Red channel by-pass enable control 0:pass through 1:by-pass
5	R/W	0	**ROP_GREENBYPASSEN** ROP Green channel by-pass enable control 0:pass through 1:by-pass
4	R/W	0	**ROP_BLUEBYPASSEN**

			ROP Blue channel by-pass enable control 0:pass through 1:by-pass
3:1	/	/	/
0	R/W	0	**ROP_MOD** ROP type selection 0:ROP3 1:ROP4 ----In ROP3 mode, only the value of 'channel 3 index 0 control table setting register' will be selected. ----In ROP3 mode, the channel 3 data will by-pass the ROP module. ----In ROP3 mode, the channel 3 data will direct to Alpha/CK module. ----In ROP4 mode, the respective input DMA channel fill color of channel 3 will transfer to Alpha/CK module.

5.2.4.20. ROP CHANNEL 3 INDEX 0 CONTROL TABLE SETTING REGISTER

Offset: 0xB8			Register Name: MP_ROPIDX0CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0	**CH2IGN_EN** Channel 2 ignore mode enable control 0:disable 1:enable When ignore mode is enabled, the data of channel will be ignored, and the data ZERO will be instead of the channel into

			the ROP module.
17	R/W	0	**CH1IGN_EN** Channel 1 ignore mode enable control 0:disable 1:enable When ignore mode is enabled, the data of channel will be ignored, and the data ZERO will be instead of the channel into the ROP module.
16	R/W	0	**CH0IGN_EN** Channel 0 ignore mode enable control 0:disable 1:enable When ignore mode is enabled, the data of channel will be ignored, and the data ZERO will be instead of the channel into the ROP module.
15	R/W	0	**NOD7_CTL** Index 0 node7 setting (channel 0' and channel 1' and channel 2' mix not logic) 0:by-pass 1:not
14:11	R/W	0	**NOD6_CTL** Index 0 node6 setting (channel 0' and channel 1' and channel 2' mix logic) 0:and 1:or 2:xor 3:add in byte

			4:add in word (32bit) 5:multiply in byte 6:multiply in word (32bit) 7:channel 0' mix channel 1' then sub channel 2' in byte 8:channel 0' mix channel 1' then sub channel 2' in word (32bit) Other: Reserved
10	R/W	0	**NOD5_CTL** Index 0 node5 setting (channel 0' and channel 1' mix not logic) 0:by-pass 1:not
9:6	R/W	0	**NOD4_CTL** Index 0 node4 setting (channel 0' and channel 1' mix logic) 0:and 1:or 2:xor 3:add in byte 4:add in word (32bit) 5:multiply in byte 6:multiply in word (32bit) 7:channel 0' sub channel 1' in byte 8:channel 0' sub channel 1' in word (32bit) Other: Reserved
5	R/W	0	**NOD3_CTL** Index 0 node3 setting (channel 2' not logic) 0:by-pass 1:not
4	R/W	0	**NOD2_CTL** Index 0 node2 setting (channel 1' not logic)

			0:by-pass 1:not
3	R/W	0	**NOD1_CTL** Index 0 node1 setting (channel 0' not logic) 0:by-pass 1:not
2:0	R/W	0	**NOD0_CTL** Index 0 node0 setting (sorting control) 0:012 1:021 2:102 3:120 4:201 5:210 Other: Reserved

Notes: The result of the add or multiply operation will select the high 8 (byte operation) or 32bits (word operation).

5.2.4.21. ROP CHANNEL 3 INDEX 1 CONTROL TABLE SETTING REGISTER

Offset: 0xBC			Register Name: MP_ROPIDX1CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0	**CH2IGN_EN** Channel 2 ignore mode enable control 0:disable 1:enable When ignore mode is enabled, the data of channel will be ignored, and the data ZERO will be instead of the channel into

			the ROP module.
17	R/W	0	**CH1IGN_EN** Channel 1 ignore mode enable control 0:disable 1:enable When ignore mode is enabled, the data of channel will be ignored, and the data ZERO will be instead of the channel into the ROP module.
16	R/W	0	**CH0IGN_EN** Channel 0 ignore mode enable control 0:disable 1:enable When ignore mode is enabled, the data of channel will be ignored, and the data ZERO will be instead of the channel into the ROP module.
15	R/W	0	**NOD7_CTL** Index 1 node7 setting (channel 0' and channel 1' and channel 2' mix not logic) 0:by-pass 1:not
14:11	R/W	0	**NOD6_CTL** Index 1 node6 setting (channel 0' and channel 1' and channel 2' mix logic) 0:and 1:or 2:xor 3:add in byte

			4:add in word (32bit) 5:multiply in byte 6:multiply in word (32bit) 7:channel 0' mix channel 1' then sub channel 2' in byte 8:channel 0' mix channel 1' then sub channel 2' in word (32bit) Other: Reserved
10	R/W	0	**NOD5_CTL** Index 1 node5 setting (channel 0' and channel 1' mix not logic) 0:by-pass 1:not
9:6	R/W	0	**NOD4_CTL** Index 1 node4 setting (channel 0' and channel 1' mix logic) 0:and 1:or 2:xor 3:add in byte 4:add in word (32bit) 5:multiply in byte 6:multiply in word (32bit) 7:channel 0' sub channel 1' in byte 8:channel 0' sub channel 1' in word (32bit) Other: Reserved
5	R/W	0	**NOD3_CTL** Index 1 node3 setting (channel 2' not logic) 0:by-pass 1:not
4	R/W	0	**NOD2_CTL** Index 1 node2 setting (channel 1' not logic)

			0:by-pass 1:not
3	R/W	0	**NOD1_CTL** Index 1 node1 setting (channel 0' not logic) 0:by-pass 1:not
2:0	R/W	0	**NOD0_CTL** Index 1 node0 setting (sorting control) 0:012 1:021 2:102 3:120 4:201 5:210 Other: Reserved

Notes: The result of the add or multiply operation will select the high 8 (byte operation) or 32bits (word operation).

5.2.4.22. ALPHA / COLOR KEY CONTROL REGISTER

Offset: 0xC0			Register Name: MP_ALPHACKCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0	**CH3GALPHA** Ch3 globe alpha value of alpha / color key module
23:16	R/W	0	**ROPGALPHA** ROP globe alpha value of alpha / color key module
15:14	R/W	0	**CH3ALPHACTL** 0:Ignore Output alpha value = pixels alpha, the pixel alpha here means the mixed alpha value of Ch3 mixed alpha

			1:Ch3 globe alpha enable Ignore pixel alpha value Output alpha value = Ch3 globe alpha value 2: Globe alpha mix pixel alpha Output alpha value = Ch3 globe alpha value * pixels alpha value 3:Reserved Note: the output alpha value here means the input alpha value of Alpha CK module.
13:12	R/W	0	**ROPALPHACTL** 0:Ignore Output alpha value = pixels alpha, the pixel alpha here means the mixed alpha value of ROP module 1:ROP globe alpha enable Ignore pixel alpha value Output alpha value = ROP globe alpha value 2: Globe alpha mix pixel alpha Output alpha value = ROP globe alpha value * pixels alpha value 3:Reserved Note: the output alpha value here means the input alpha value of Alpha CK module.
11	/	/	/

10	R/W	0	**CK_REDCON** Red control condition 0: if (R value of ck min color) <= (R value of layer0) <= (R value of ck max color), The red control condition is true, else the condition is false. 1: if (R value of ck min color) > (R value of layer0) or (R value of layer0) > (R value of ck max color), The red control condition is true, else the condition is false.
9	R/W	0	**CK_GREENCON** Green control condition 0: if (G value of ck min color) <= (G value of layer0) <= (G value of ck max color), The green control condition is true, else the condition is false. 1: if (G value of ck min color) > (G value of layer0) or (G value of layer0) > (G value of ck max color), The green control condition is true, else the condition is false.
8	R/W	0	**CK_BLUECON** Blue control condition 0: if (B value of ck min color) <= (B value of layer0) <= (B value of ck max color), The blue control condition is true, else the condition is false. 1: if (B value of ck min color) > (B value of layer0) or (B value of layer0) > (B value of ck max color), The blue control condition is true, else the condition is false.
7	R/W	0	**ICH3_PREMUL** 0: normal data

			1: pre-multiply input data
6	R/W	0	**IROP_PREMUL** 0: normal data 1: pre-multiply input data
5	R/W	0	**O_PREMUL** 0: output normal data 1: output pre-multiply data
4	R/W	0	**PRI** Priority selection 0: ROP output channel is higher than channel 3 1: Channel 3 is higher than ROP output channel
3	/	/	/
2:1	R/W	0	**ALPHACK_MOD** Alpha / Color key mode selection 0: alpha mode 1: color key mode, using the high priority layer as matching condition, if it is true, the low priority layer pass. 2: color key mode, using the low priority layer as matching condition, if it is true, the high priority layer pass. 3: Reserved
0	R/W	0	**ALPHACK_EN** Enable control 0: the ROP data will by-pass the alpha/ck module 1: enable Note: if the module is disabled, the data of channel 3 will be ignored, and only the ROP data will pass through to CSC2 module.

5.2.4.23. COLOR KEY MIN COLOR REGISTER

Offset: 0xC4			Register Name: MP_CKMIN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0	**CKMIN_R** Red
15:8	R/W	0	**CKMIN_G** Green
7:0	R/W	0	**CKMIN_B** Blue

5.2.4.24. COLOR KEY MAX COLOR REGISTER

Offset: 0xC8			Register Name: MP_CKMAX_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0	**CKMAX_R** Red
15:8	R/W	0	**CKMAX_G** Green
7:0	R/W	0	**CKMAX_B** Blue

5.2.4.25. FILL COLOR OF ROP OUTPUT SETTING REGISTER

Offset: 0xCC			Register Name: MP_ROPOUTFILLCOLOR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0	**Alpha**
23:16	R/W	0	**Red**
15:8	R/W	0	**Green**
7:0	R/W	0	**Blue**

5.2.4.26. COLOR SPACE CONVERTER 2 CONTROL REGISTER

Offset: 0xD0			Register Name: MP_CSC2CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0	**CSC2_EN** Enable control 0: Disable color space function, ignore the control setting, and the data flow will by-pass the module. 1: Enable color space converting function.

5.2.4.27. OUTPUT CONTROL REGISTER

Offset: 0xE0			Register Name: MP_OUTCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:8	R/W	0	**OUT_PS** Output data pixel sequence Refer to the output pixel sequence table
7	R/W	0	**RND_EN** Round enable 0:disabled 1:enabled
6:4	/	/	/
3:0	R/W	0	**OUT_FMT** Output data format 0x0: 32bpp – A8R8G8B8 or interleaved AYUV8888 0x1: 16bpp – A4R4G4B4

			0x2: 16bpp – A1R5G5B5 0x3: 16bpp – R5G6B5 0x4: 16bpp – interleaved YUV422 0x5: planar YUV422 (UV combined) 0x6: planar YUV422 0x7: 8bpp – MONO 0x8: 4bpp – MONO 0x9: 2bpp – MONO 0xa: 1bpp – MONO 0xb: planar YUV420 (UV combined) 0xc: planar YUV420 0xd: planar YUV411 (UV combined) 0xe: planar YUV411 Other: reserved Note: In all YUV output data format, the CSC2 must be enabled, otherwise the output data mode will be 32bpp A8R8G8B8 mode.

Output data mode and output data ports mapping:

Output data mode	Output data channel selection		
	Channel 0	Channel 1	Channel 2
A8R8G8B8 or interleaved AYUV8888	ARGB or AYUV	Ignore	Ignore
A4R4G4B4	ARGB	Ignore	Ignore
A1R5G5B5	ARGB	Ignore	Ignore
R5G6B5	RGB	Ignore	Ignore
interleaved YUV422	YUV	Ignore	Ignore

planar YUV422 (UV combined)	Y	UV	Ignore
planar YUV422	Y	U	V
8bpp – MONO	MONO	Ignore	Ignore
4bpp – MONO	MONO	Ignore	Ignore
2bpp – MONO	MONO	Ignore	Ignore
1bpp – MONO	MONO	Ignore	Ignore
planar YUV420 (UV combined)	Y	UV	Ignore
planar YUV420	Y	U	V
planar YUV411 (UV combined)	Y	UV	Ignore
planar YUV411	Y	U	V

5.2.4.28. OUTPUT SIZE REGISTER

Offset: 0xE8			Register Name: MP_OUTSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0	**OUT_HEIGHT** Height The value plus 1 equals to the actual output image height
15:13	/	/	/
12:0	R/W	0	**OUT_WIDTH** Width The value plus 1 equals to the actual output image width

5.2.4.29. OUTPUT ADDRESS HIGH 4BITS REGISTER

Offset: 0xEC			Register Name: MP_OUTH4ADD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:16	R/W	0	**OUTCH2_H4ADD**

			Output channel 2 High 4bits address in bits
15:12	/	/	/
11:8	R/W	0	**OUTCH1_H4ADD** Output channel 1 High 4bits address in bits
7:4	/	/	/
3:0	R/W	0	**OUTCH0_H4ADD** Output channel 0 High 4bits address in bits

5.2.4.30. OUTPUT ADDRESS LOW 32BITS REGISTER

Offset: **Out channel 0:0xF0** **Out channel 1:0xF4** **Out channel 2:0xF8**			**Register Name: MP_OUTL32ADD_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0	**OUT_L32ADD** Output channel Low 32bits address in bits

5.2.4.31. OUTPUT LINE WIDTH REGISTER

Offset: **Out channel 0:0x100** **Out channel 1:0x104** **Out channel 2:0x108**			**Register Name: MP_OUTLINEWIDTH_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0	**OUT_LINEWIDTH** Output channel

			Line width in bits

5.2.4.32. OUTPUT ALPHA CONTROL REGISTER

Offset: 0x120			Register Name: MP_OUTALPHACTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0	**IMG_ALPHA** Output image area alpha value, the image area include A0,A1 and overlapping area A2.
23:16	R/W	0	**NONIMG_ALPHA** Output non-image area alpha value, the non-image area means the pure fill color area.
15:8	/	/	/
7:6	R/W	0	**A2ALPHACTL** A2 area alpha value control 0: using A0 self pixel alpha (A0pA) 1: using A1 self pixel alpha (A1pA) 2: Mixed alpha A (A0pA + A1pA * (1 - A0pA)) 3: using the Output image area alpha value (bit31:24)
5:4	R/W	0	**A3ALPHACTL** A3 area alpha value control 0: 0xff 1: using the Output non-image area alpha value (bit23:16) 2: Mixed alpha A Other: reserved
3:2	R/W	0	**A1ALPHACTL** A1 area alpha value control 0: using A1 self pixel alpha 1: using the Output image area alpha value (bit31:24) 2: Mixed alpha A

			Other: reserved
1:0	R/W	0	**A0ALPHACTL** A0 area alpha value control 0: using A0 self pixel alpha 1: using the Output image area alpha value (bit31:24) 2: Mixed alpha A Other: reserved

Description:

There is some area in output memory block:

The alpha / color key module is enabled:

Only the high priority image area is called A0

Only the low priority image area is called A1

The high priority and low priority mixed image area is called A2

The other area is called A3

And the A0,A1,A2 is called image area, the A3 is called non-image area.

The alpha / color key module is disabled:

Only the ROP output image area is called A0, A0 is called image area.

The other area is called A3, A3 is called non-image area.

Mixed alpha A: Reference can be made to Alpha / Color key description

Notes: the register setting is only valid in ARGB or AYUV mode.

5.2.4.33. MB CONTROL REGISTER

Offset: iDMA0:0X130 iDMA1:0X134	**Register Name: MP_MBCTL_REG**

iDMA2:0X138 iDMA3:0X13C			
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0	**Y_OFFSET** The y offset of the top-left point in the whole image
15:0	R/W	0	**X_OFFSET** The x offset of the top-left point in the whole image

5.2.4.34. CSC0/1 Y/G COEFFICIENT REGISTER

Offset: **G/Y component: 0x180** **R/U component: 0x184** **B/V component: 0x188**			**Register Name: MP_ICSCYGCOEF_REG**
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x4a7 0x1e6f 0x1cbf	**CSC1_YGCOEF** the Y/G coefficient for CSC1 the value equals to coefficient*2^{10}
15:13	/	/	/
12:00	R/W	0x4a7 0x1e6f 0x1cbf	**CSC0_YGCOEF** the Y/G coefficient for CSC0 the value equals to coefficient*2^{10}

5.2.4.35. CSC0/1 Y/G CONSTANT REGISTER

Offset: 0x18C			**Register Name: MP_ICSCYGCONS_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	0x877	**CSC1_YGCONS** the Y/G constant for CSC1

			the value equals to coefficient*2^4
15:14	/	/	/
13:00	R/W	0x877	**CSC0_YGCONS** the Y/G constant for CSC0 the value equals to coefficient*2^4

5.2.4.36. CSC0/1 U/R COEFFICIENT REGISTER

Offset: **G/Y component: 0x190** **R/U component: 0x194** **B/V component: 0x198**			**Register Name: MP_ICSCURCOEF_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x4a7 0x00 0x662	**CSC1_URCOEF** the U/R coefficient for CSC1 the value equals to coefficient*2^{10}
15:13	/	/	/
12:00	R/W	0x4a7 0x00 0x662	**CSC0_URCOEF** the U/R coefficient for CSC0 the value equals to coefficient*2^{10}

5.2.4.37. CSC0/1 U/R CONSTANT REGISTER

Offset: 0x19C			**Register Name: MP_ICSCURCONS_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	0x3211	**CSC1_URCONS** the U/R constant for CSC1 the value equals to coefficient*2^4
15:14	/	/	/

13:00	R/W	0x3211	**CSC0_URCONS** the U/R constant for CSC0 the value equals to coefficient*2^4

5.2.4.38. CSC0/1 V/B COEFFICIENT REGISTER

Offset: **G/Y component: 0x1A0** **R/U component: 0x1A4** **B/V component: 0x1A8**			**Register Name: MP_ICSCVBCOEF_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x4a7 0x812 0x00	**CSC1_VBCOEF** the V/B coefficient for CSC1 the value equals to coefficient*2^{10}
15:13	/	/	/
12:00	R/W	0x4a7 0x812 0x00	**CSC0_VBCOEF** the V/B coefficient for CSC0 the value equals to coefficient*2^{10}

5.2.4.39. CSC0/1 V/B CONSTANT REGISTER

Offset: 0x1AC			**Register Name: MP_ICSCVBCONS_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	0x2eb1	**CSC1_VBCONS** the V/B constant for CSC1 the value equals to coefficient*2^4
15:14	/	/	/
13:00	R/W	0x2eb1	**CSC0_VBCONS** the V/B constant for CSC0

			the value equals to coefficient*2^4

5.2.4.40. CSC2 Y/G COEFFICIENT REGISTER

Offset: G/Y component: 0x1C0 R/U component: 0x1C4 B/V component: 0x1C8			Register Name: MP_OCSCYGCOEF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:00	R/W	/	**CSC2_YGCOEF** the Y/G coefficient the value equals to coefficient*2^{10}

5.2.4.41. CSC2 Y/G CONSTANT REGISTER

Offset: 0x1CC			Register Name: MP_OCSCYGCONS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:00	R/W	/	**CSC2_YGCONS** the Y/G constant the value equals to coefficient*2^4

5.2.4.42. CSC2 U/R COEFFICIENT REGISTER

Offset: G/Y component: 0x1D0 R/U component: 0x1D4 B/V component: 0x1D8			Register Name: MP_OCSCURCOEF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:00	R/W		**CSC2_URCOEF**

			the U/R coefficient the value equals to coefficient*2^{10}

5.2.4.43. CSC2 U/R CONSTANT REGISTER

Offset: 0x1DC			Register Name: MP_OCSCURCONS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:00	R/W		**CSC2_URCONS** the U/R constant the value equals to coefficient*2^4

5.2.4.44. CSC2 V/B COEFFICIENT REGISTER

Offset: G/Y component: 0x1E0 R/U component: 0x1E4 B/V component: 0x1E8			Register Name: MP_OCSCVBCOEF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:00	R/W		**CSC2_VBCOEF** the V/B coefficient the value equals to coefficient*2^{10}

5.2.4.45. CSC2 V/B CONSTANT REGISTER

Offset: 0x1EC			Register Name: MP_OCSCVBCONS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:00	R/W		**CSC2_VBCONS** the V/B constant the value equals to coefficient*2^4

5.2.4.46. SCALING HORIZONTAL FILTERING COEFFICIENT RAM BLOCK

Offset: 0x200 – 0x27C			
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0	Horizontal tap3 coefficient The value equals to coefficient*2^6
23:16	R/W	0	Horizontal tap2 coefficient The value equals to coefficient*2^6
15:08	R/W	0	Horizontal tap1 coefficient The value equals to coefficient*2^6
07:00	R/W	0	Horizontal tap0 coefficient The value equals to coefficient*2^6

5.2.4.47. SCALING VERTICAL FILTERING COEFFICIENT RAM BLOCK

Offset: 0x280 – 0x2FC			
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0	Vertical tap3 coefficient The value equals to coefficient*2^6
23:16	R/W	0	Vertical tap2 coefficient The value equals to coefficient*2^6
15:08	R/W	0	Vertical tap1 coefficient The value equals to coefficient*2^6
07:00	R/W	0	Vertical tap0 coefficient The value equals to coefficient*2^6

5.2.4.48. PALETTE TABLE

Offset:	

0x400-0x7FF			
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	UDF	Alpha value
23:16	R/W	UDF	Red value
15:08	R/W	UDF	Green value
07:00	R/W	UDF	Blue value

5.2.4.49. COMMAND QUEUE CONTROL REGISTER

Offset: 0x1000			Register Name: CMDQUECTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0	**FINISHIRQ_EN** Mission finish IRQ enable control 0:disable 1:enable
7:2	/	/	/
1	R/W	0	**START_CTL** Start control If the bit is set, the module will start a operation sets and stop auto. The operation sets is stored in external memory.
0	R/W	0	**EN** Command queue function enable control 0:disable 1:enable

5.2.4.50. COMMAND QUEUE STATUS REGISTER

Offset: 0x1004			Register Name: CMDQUESTS _REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:13	/	/	/
12	R	0	**BUSY_FLAG** Module working status 0:idle 1:running
11:9	/	/	/
8	R/W	0	**FINISHIRQ_FLAG** Mission finish IRQ It will be set when 1 frame operation accomplished, and cleared by writing 1.
7:0	/	/	/

5.2.4.51. COMMAND QUEUE STORAGE START ADDRESS REGISTER

Offset: 0x1010			**Register Name: CMDQUEADD_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0	**STARTADD** Command queue start address in bytes

5.2.4.52. INPUT DATA PIXEL SEQUENCE TABLE

1-bpp mode

PS=xx00

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16
P15	P14	P13	P12	P11	P10	P09	P08	P07	P06	P05	P04	P03	P02	P01	P00
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=xx01

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P24	P25	P26	P27	P28	P29	P30	P31	P16	P17	P18	P19	P20	P21	P22	P23
P08	P09	P10	P11	P12	P13	P14	P15	P00	P01	P02	P03	P04	P05	P06	P07
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=xx10

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P07	P06	P05	P04	P03	P02	P01	P00	P15	P14	P13	P12	P11	P10	P09	P08
P23	P22	P21	P20	P19	P18	P17	P16	P31	P30	P29	P28	P27	P26	P25	P24
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=xx11

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P00	P01	P02	P03	P04	P05	P06	P07	P08	P09	P10	P11	P12	P13	P14	P15
P16	P17	P18	P19	P20	P21	P22	P23	P24	P25	P26	P27	P28	P29	P30	P31
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

2-bpp mode

PS=xx00

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P15		P14		P13		P12		P11		P10		P09		P08	
P07		P06		P05		P04		P03		P02		P01		P00	
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=xx01

Bit

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16
P12	P13	P14	P15	P08	P09	P10	P11
P04	P05	P06	P07	P00	P01	P02	P03
15 14	13 12	11 10	09 08	07 06	05 04	03 02	01 00

PS=xx10

Bit

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16
P03	P02	P01	P00	P07	P06	P05	P04
P11	P10	P09	P08	P15	P14	P13	P12
15 14	13 12	11 10	09 08	07 06	05 04	03 02	01 00

PS=xx11

Bit

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16
P00	P01	P02	P03	P04	P05	P06	P07
P08	P09	P10	P11	P12	P13	P14	P15
15 14	13 12	11 10	09 08	07 06	05 04	03 02	01 00

4-bpp mode

PS=xx00

Bit

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16
P07	P06	P05	P04
P03	P02	P01	P00
15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00

PS=xx01

Bit

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16
P06	P07	P04	P05
P02	P03	P00	P01
15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00

PS=xx10

Bit

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16
P01	P00	P03	P02
P05	P04	P07	P06
15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00

PS=xx11

Bit

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16
P00	P01	P02	P03
P04	P05	P06	P07
15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00

8-bpp mode

PS=xx00 / xx11

Bit

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16
P3	P2
P1	P0
15 14 13 12 11 10 09 08	07 06 05 04 03 02 01 00

PS=xx01 / xx10

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P0								P1							
P2								P3							
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

16-bpp @ A4R4G4B4 mode

PS=0x00

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
A1				R1				G1				B1			
A0				R0				G0				B0			
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=0x01

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
A0				R0				G0				B0			
A1				R1				G1				B1			
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=0x10

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B1				G1				R1				A1			
B0				G0				R0				A0			
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=0x11

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B0				G0				R0				A0			
B1				G1				R1				A1			
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=1xxx, the R component is swapped with B component

16-bpp @ A1R5G5B5 mode

PS=0x00

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
A1	R1					G1					B1				
A0	R0					G0					B0				
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=0x01

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
A0	R0					G0					B0				
A1	R1					G1					B1				
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=0x10

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B1				G1				R1				A1			
B0				G0				R0				A0			
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=0x11

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
B0					G0					R0					A0
B1					G1					R1					A1
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=1xxx, the R component is swapped with B component

16-bpp @ R5G6B5 mode

PS=0x00

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R1					G1						B1				
R0					G0						B0				
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=0x01

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R0					G0						B0				
R1					G1						B1				
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=1xxx, the R component is swapped with B component

16-bpp @ interleaved YUV422 mode

PS=xx00 / xx11

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
V0								Y1							
U0								Y0							

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

PS=xx01 / xx10

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

Y1	V0
Y0	U0

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

16-bpp @ U8V8 mode

PS=xxxx

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

V1	U1
V0	U0

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

32-bpp ARGB or AYUV mode

PS=xx00 / xx01

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

A	R (Y)
G (U)	B (V)

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

PS=xx10 / xx11

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

B (V)	G (U)

R (Y)	A

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

PS=1xxx, the R component is swapped with B component

5.2.4.53. OUTPUT DATA PIXEL SEQUENCE

32bpp – A8R8G8B8 or interleaved AYUV8888

16bpp – A4R4G4B4

16bpp – A1R5G5B5

16bpp – R5G6B5

16bpp – interleaved YUV422

Planar YUV422 (UV combined)

8bpp – MONO

4bpp – MONO

2bpp – MONO

1bpp – MONO

Planar YUV420 (UV combined)

Planar YUV411 (UV combined)

The above 13 kinds of output format is same as respective input format PS.

Planar YUV422

Planar YUV420

Planar YUV411

The above 3 output formats are the same as input 8bpp format PS.

6 IMAGE

This chapter details the image processing capability of A31 from following three sections:

- CSI 0
- CSI1
- MIPI CSI

The MIPI CSI interface is routed to CSI0 module, while normal CSI is routed to CSI1 module.

6.1. CSI 0

6.1.1. OVERVIEW

The MIPI CSI interface is routed to CSI0 module.

CSI0 module features:

- Support CMOS-sensor parallel interface with HREF and VSYNC
- Support CCIR656 protocol for NTSC and PAL
- Support multi-channel ITU-R BT.656 time-multiplexed format
- Support 8/10/12bit raw data input
- Support 8/10 bit yuv422 data input
- Pass raw data direct to memory or to ISP
- Parsing YUV data into planar or semi-planar output to memory
- Support CMOS-sensor and TV decoder
- Support up to 1080p@30fps or 5M@15fps using SOC CMOS-sensor with YUV format
- Support up to 1080p@60fps or 5M@30fps using CMOS-sensor with RAW format

6.1.2. CSI0 BLOCK DIAGRAM

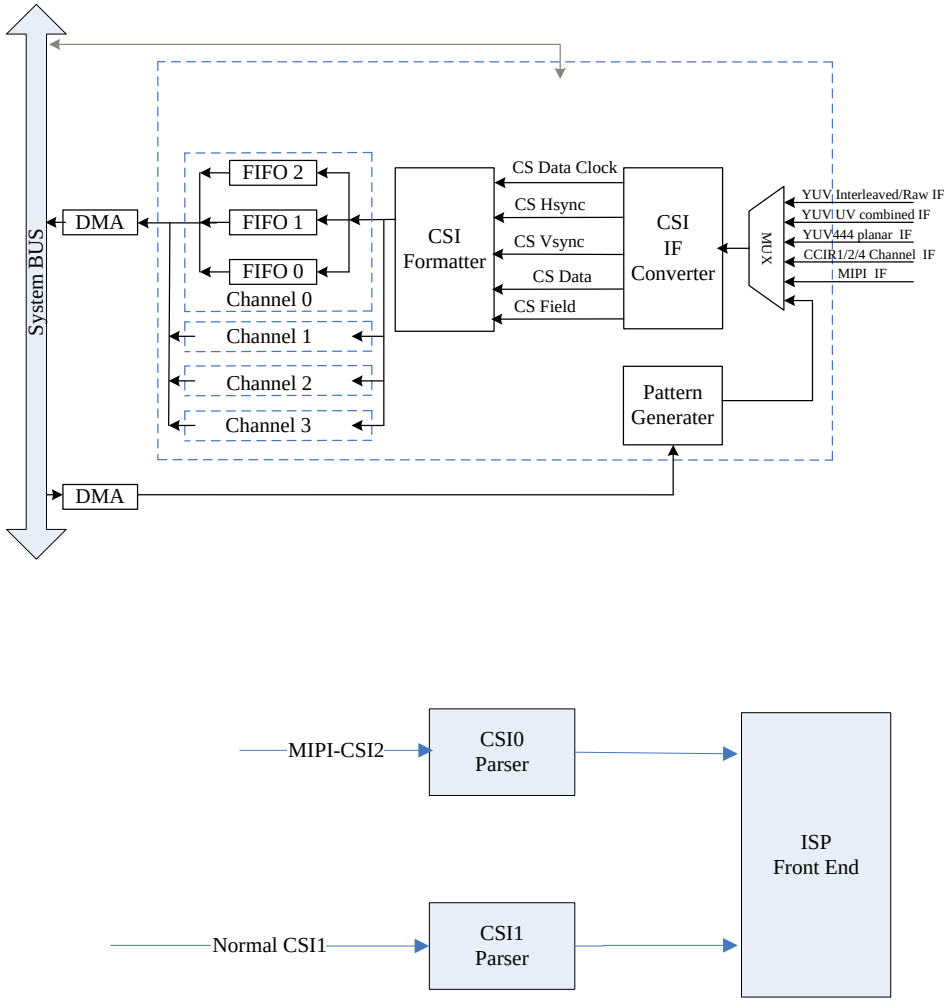


Figure 6-1 CSI0 Block Diagram

6.1.3. CSI0 DESCRIPTION

6.1.3.1. CSI FIFO DISTRIBUTION

Interface	YUYV422 Interleaved/RAW			YUV422 UV Combined	YUV444 Planar	YUV444 Planar to YUV422 UV Combined
Input format	YUV422		Raw	Raw	Raw	Raw
Output format	Planar	UV combined/	Raw/RGB	Raw	Raw	Raw

		MB	/PRGB			
CH0_FIFO0	Y pixel data	Y pixel data	All pixels data	Y pixel data	Y pixel data	Y pixel data
CH0_FIFO1	Cb (U) pixel data	Cb (U) Cr (V) pixel data	-	-	-	-
CH0_FIFO2	Cr (V) pixel data	-	-	-	-	-
CH1_FIFO0	-	-	-	Cb (U) Cr (V) pixel data	Cb (U) pixel data	Cb (U) Cr (V) pixel data
CH2_FIFO0	-	-	-	-	Cr(V) pixel data	-

Interface	**BT656 Interface**		**Channels**		
Input format	**YUV422**				
Output format	**Planar**	**UV combined/ MB**			
CH0_FIFO0	Y	Y	1	2	4
CH0_FIFO1	Cb (U)	CbCr (UV)			
CH0_FIFO2	Cr (V)	-			
CH1_FIFO0	Y	Y	-		
CH1_FIFO1	Cb (U)	CbCr (UV)			
CH1_FIFO2	Cr (V)	-			
CH2_FIFO0	Y	Y		-	
CH2_FIFO1	Cb (U)	CbCr (UV)			

CH2_FIFO2	Cr (V)	-			
CH3_FIFO0	Y	Y			
CH3_FIFO1	Cb (U)	CbCr (UV)			
CH3_FIFO2	Cr (V)	-			

Interface	**MIPI Interface**			**Channels**			
Input format	**YUV422/YUV420**		**Raw**				
Output format	**Planar**	**UV combined/MB**	**Pass-Through/Padding**				
CH0_FIFO0	Y	Y	All pixels data	1	2	3	4
CH0_FIFO1	Cb (U)	CbCr (UV)	-				
CH0_FIFO2	Cr (V)	-	-				
CH1_FIFO0	Y	Y	All pixels data	-			
CH1_FIFO1	Cb (U)	CbCr (UV)	-				
CH1_FIFO2	Cr (V)	-	-				
CH2_FIFO0	Y	Y	All pixels data		-		
CH2_FIFO1	Cb (U)	CbCr (UV)	-				
CH2_FIFO2	Cr (V)	-	-				
CH3_FIFO0	Y	Y	All pixels data			-	
CH3_FIFO1	Cb (U)	CbCr	-				

		(UV)					
CH3_FIFO2	Cr (V)	-	-				

6.1.3.2. PIXEL FORMAT ARRANGEMENT

RAW-10:

Dummy1[5:0]	Raw data 1[9:0]	Dummy 0[5:0]	Raw data 0[9:0]

MSB LSB

RAW-12:

Dummy1[3:0]	Raw data 1[11:0]	Dummy 0[3:0]	Raw data 0[11:0]

MSB LSB

YUV-10:

Y:

Dummy1[5:0]	Y1[9:0]	Dummy 0[5:0]	Y 0[9:0]

MSB LSB

UV Combined:

Dummy1[5:0]	V/U 0[9:0]	Dummy 0[5:0]	U/V 0[9:0]

MSB LSB

RGB888:

B1[7:0]	R0[7:0]	G0[7:0]	B0[7:0]
G2[7:0]	B2[7:0]	R1[7:0]	G1[7:0]
R3[7:0]	G3[7:0]	B3[7:0]	R2[7:0]

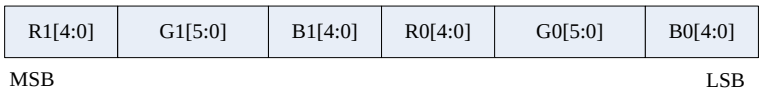
MSB

PRGB888:

PAD[7:0]	R0[7:0]	G0[7:0]	B0[7:0]

MSB LSB

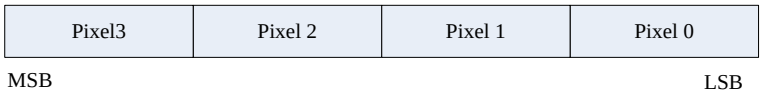
RGB565:



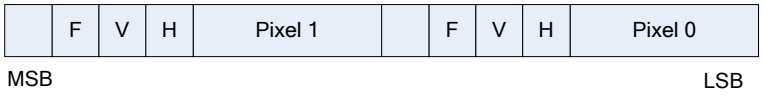
6.1.3.3. PATTERN GENERATING FORMAT

The pattern generated from DRAM is arranged as follow:

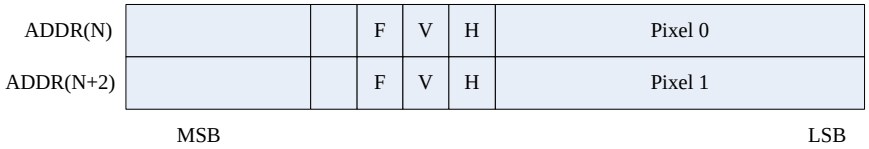
BT656 Interface:



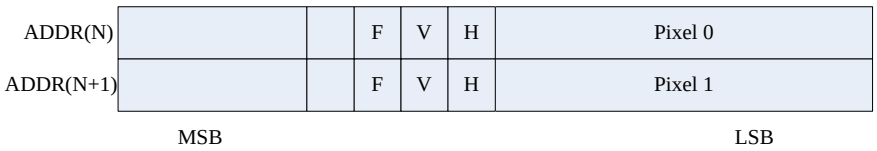
YUV422 Interleaved or RAW Interface:



YUV422 Interleaved or RAW Interface(10bit or 12 bit data bus):



YUV422 UV combined Interface:

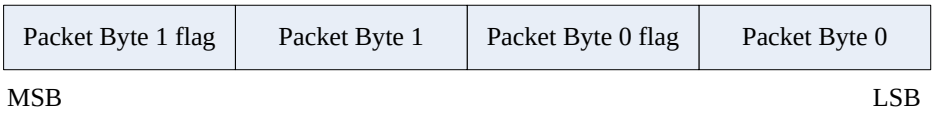


YUV444 Planar Interface:

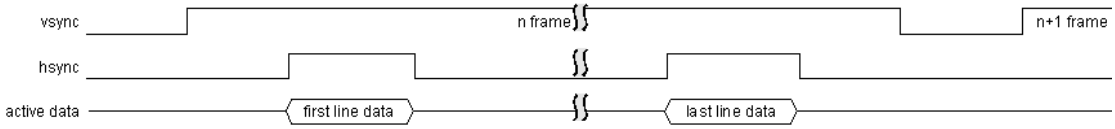
MIPI:

Packet byte flag is 0 indicates that the packet byte is the valid content.

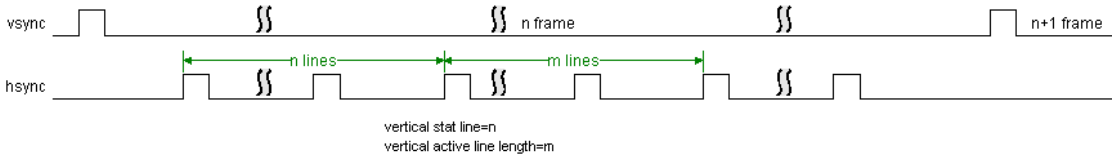
Packet byte flag is 1 indicates that the packet byte is the blanking.



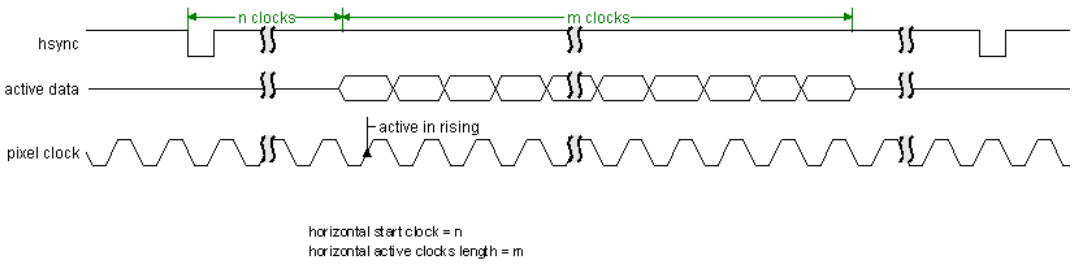
6.1.3.4. CSI0 TIMING DIAGRAM



Vref= positive; Href= positive

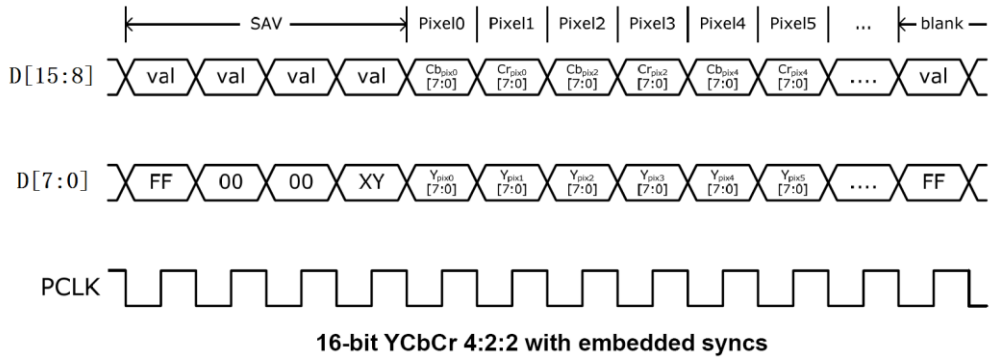


vertical size setting



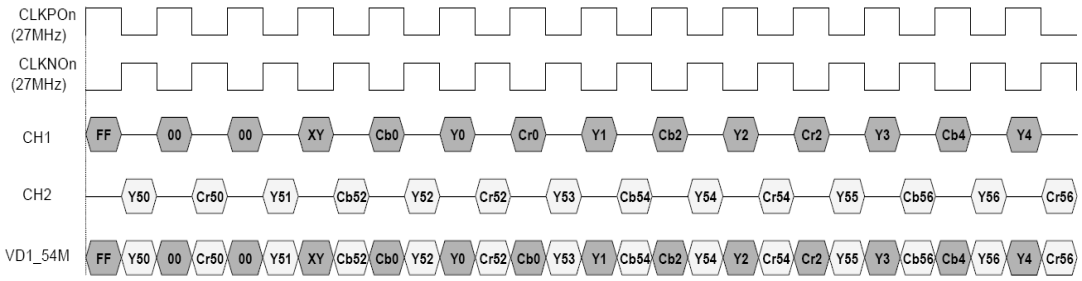
horizontal size setting and pixel clock timing(Href= positive)

16bit YUV422 Timing

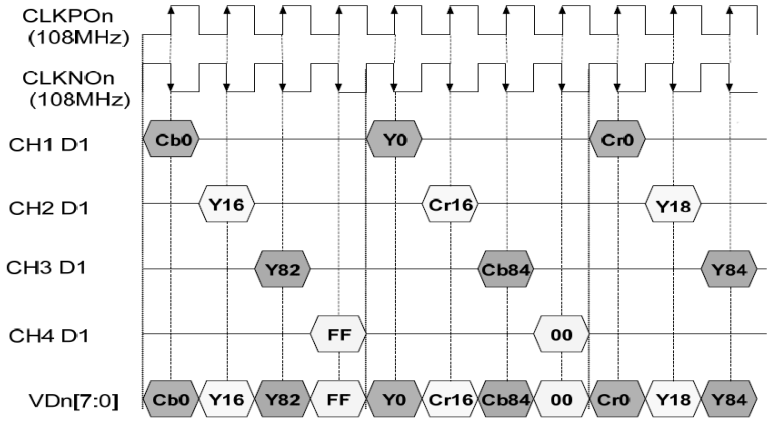


16-bit YCbCr 4:2:2 with embedded syncs

CCIR656 2 channel Timing



CCIR656 4 channel Timing



CCIR656 Header Code

CCIR656 Header Data Bit Definition

Data Bit	First Word(0xFF)	Second Word(0x00)	Third Word(0x00)	Fourth Word
CS D[9] (MSB)	1	0	0	1
CS D[8]	1	0	0	F
CS D[7]	1	0	0	V
CS D[6]	1	0	0	H
CS D[5]	1	0	0	P3
CS D[4]	1	0	0	P2
CS D[3]	1	0	0	P1
CS D[2]	1	0	0	P0
CS D[1]	x	x	x	x
CS D[0]	x	x	x	x

For compatibility with an 8-bit interface, CS D[1] and CS D[0] are not defined.

Decode	F	V	H	P3	P2	P1	P0
Field 1 start of active video (SAV)	0	0	0	0	0	0	0
Field 1 end of active video (EAV)	0	0	1	1	1	0	1
Field 1 SAV (digital blanking)	0	1	0	1	0	1	1
Field 1 EAV (digital blanking)	0	1	1	0	1	1	0
Field 2 SAV	1	0	0	0	1	1	1
Field 2 EAV	1	0	1	1	0	1	0
Field 2 SAV (digital blanking)	1	1	0	1	1	0	0
Field 2 EAV (digital blanking)	1	1	1	0	0	0	1

Multi-Channel:

Condition			656 FVH Value			SAV-EAV Code						
									Fourth			
Field	V-time	H-time	F	V	H	First	Second	Third	Ch1	Ch2	Ch3	Ch4
EVEN	BLANK	EAV	1	1	1	0xFF	0x00	0x00	0xF0	0xF1	0xF2	0xF3
EVEN	BLANK	SAV	1	1	0	0xFF	0x00	0x00	0xE0	0xE1	0xE2	0xE3
EVEN	ACTIVE	EAV	1	0	1	0xFF	0x00	0x00	0xD0	0xD1	0xD2	0xD3
EVEN	ACTIVE	SAV	1	0	0	0xFF	0x00	0x00	0xC0	0xC1	0xC2	0xC3
ODD	BLANK	EAV	0	1	1	0xFF	0x00	0x00	0xB0	0xB1	0xB2	0xB3
ODD	BLANK	SAV	0	1	0	0xFF	0x00	0x00	0xA0	0xA1	0xA2	0xA3
ODD	ACTIVE	EAV	0	0	1	0xFF	0x00	0x00	0x90	0x91	0x92	0x93
ODD	ACTIVE	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x81	0x82	0x83

6.1.3.5. OFFSET / SCALE / FLIP FUNCTION

Interface will do these three functions in sequence.

6.1.3.6. OFFSET DEFINITION

Offset in horizontal and vertical can be added when receiving image. Unit is pixel.

For YUV422 format, pixel unit is a YU/YV combination.

For YUV420 format, pixel unit is a YU/YV combination in YC line, and only a Y in Y line.

For Bayer_raw format, pixel unit is a R/G/B single component.

For RGB565, pixel unit is a two bytes of RGB565 package.

For RGB888, pixel unit is a three bytes of RGB combination.

6.1.3.7. SCALE DEFINITION

All channel input image can be decimated to its quarter size if **QUART_EN** is set to 1.

When using this function, horizontal input components should be multiples of the components in a unit, and vertical lines should be multiples of the height of a unit.

Specific components and lines will be dropped except the **blue** ones as follows.

Component sequence in a unit may changed, but unit dropping position will not changed.

BAYER_RAW(raw_8/raw_10/raw_12):

GRGRGRGR…

BGBGBGBG…

GRGRGRGR…

BGBGBGBG…

GRGRGRGR…

BGBGBGBG…

GRGRGRGR…

BGBGBGBG…

RGB888:

RGBRGB…

RGBRGB…

RGB565:

565565…

565565…

YUV422(8bit/10bit in field mode):

YUYVYUYV…

YUYVYUYV…

YUYVYUYV…

YUYVYUYV…

YUV422(8bit/10bit in frame mode):

YUYVYUYV…→odd field

YUYVYUYV…→even field

YUYVYUYV…

YUYVYUYV…

YUV420(8bit/10bit):

YC line: **YUYVYUYV…**

Y line: **YYYY…**

YC line: **YUYVYUYV…**

Y line: **YYYY…**

6.1.3.8. FLIP DEFINITION

Both horizontal and vertical flip are supported at the same time. This function is implemented **in the process of each FIFO writing data to memory, only flipping the data of separate FIFO, not changing component to FIFO distribution**.

If horizontal flip is enabled, one or more pixels will be took as a unit:

For YUV format, a unit of $Y_0U_0Y_1V_1$ will parser and flip the Y component in one channel, and UV will be treated as a whole. In planar output mode, U and V will be flipped separately. In UV combined output mode, UV will be flipped as a whole. So, a sequence of $Y_1U_0Y_0V_1$ will be.

For Bayer_raw format, situation is much like. A GR/BG sequence will be changed to BG/RG. A unit of square has four pixels.

For RGB565/RGB888, one unit of two/three bytes of component will be flipped with original sequence.

6.1.4. CSI0 REGISTER LIST

Module Name	Base Address
CSI0	0x01CB0000

Register Name	Offset	Register name
CSI0_EN_REG	0X000	CSI enable register

CSI0_IF_CFG_REG	0X004	CSI Interface Configuration Register
CSI0_CAP_REG	0X008	CSI Capture Register
CSI0_SYNC_CNT_REG	0X00C	CSI Synchronization Counter Register
CSI0_FIFO_THRS_REG	0X010	CSI FIFO Threshold Register
CSI0_PTN_LEN_REG	0X030	CSI Pattern Generation Length register
CSI0_PTN_ADDR_REG	0X034	CSI Pattern Generation Address register
CSI0_VER_REG	0X03C	CSI Version Register
CSI0_C0_CFG_REG	0X044	CSI Channel_0 configuration register
CSI0_C0_SCALE_REG	0X04C	CSI Channel_0 scale register
CSI0_C0_F0_BUFA_REG	0X050	CSI Channel_0 FIFO 0 output buffer-A address register
CSI0_C0_F1_BUFA_REG	0X058	CSI Channel_0 FIFO 1 output buffer-A address register
CSI0_C0_F2_BUFA_REG	0X060	CSI Channel_0 FIFO 2 output buffer-A address register
CSI0_C0_CAP_STA_REG	0X06C	CSI Channel_0 status register
CSI0_C0_INT_EN_REG	0X070	CSI Channel_0 interrupt enable register
CSI0_C0_INT_STA_REG	0X074	CSI Channel_0 interrupt status register
CSI0_C0_HSIZE_REG	0X080	CSI Channel_0 horizontal size register
CSI0_C0_VSIZE_REG	0X084	CSI Channel_0 vertical size register
CSI0_C0_BUF_LEN_REG	0X088	CSI Channel_0 line buffer length register
CSI0_C0_FLIP_SIZE_REG	0X08C	CSI Channel_0 flip size register
CSI0_C0_FRM_CLK_CNT_REG	0X090	CSI Channel_0 frame clock counter register
CSI0_C0_ACC_ITNL_CLK_CNT_REG	0X094	CSI Channel_0 accumulated and internal clock counter register
CSI0_C1_CFG_REG	0X144	CSI Channel_1 configuration register
CSI0_C1_SCALE_REG	0X14C	CSI Channel_1 scale register
CSI0_C1_F0_BUFA_REG	0X150	CSI Channel_1 FIFO 0 output buffer-A address

		register
CSI0_C1_F1_BUFA_REG	0X158	CSI Channel_1 FIFO 1 output buffer-A address register
CSI0_C1_F2_BUFA_REG	0X160	CSI Channel_1 FIFO 2 output buffer-A address register
CSI0_C1_CAP_STA_REG	0X16C	CSI Channel_1 status register
CSI0_C1_INT_EN_REG	0X170	CSI Channel_1 interrupt enable register
CSI0_C1_INT_STA_REG	0X174	CSI Channel_1 interrupt status register
CSI0_C1_HSIZE_REG	0X180	CSI Channel_1 horizontal size register
CSI0_C1_VSIZE_REG	0X184	CSI Channel_1 vertical size register
CSI0_C1_BUF_LEN_REG	0X188	CSI Channel_1 line buffer length register
CSI0_C1_FLIP_SIZE_REG	0X18C	CSI Channel_1 flip size register
CSI0_C1_FRM_CLK_CNT_REG	0X190	CSI Channel_1 frame clock counter register
CSI0_C1_ACC_ITNL_CLK_CNT_REG	0X194	CSI Channel_1 accumulated and internal clock counter register
CSI0_C2_CFG_REG	0X244	CSI Channel_2 configuration register
CSI0_C2_SCALE_REG	0X24C	CSI Channel_2 scale register
CSI0_C2_F0_BUFA_REG	0X250	CSI Channel_2 FIFO 0 output buffer-A address register
CSI0_C2_F1_BUFA_REG	0X258	CSI Channel_2 FIFO 1 output buffer-A address register
CSI0_C2_F2_BUFA_REG	0X260	CSI Channel_2 FIFO 2 output buffer-A address register
CSI0_C2_CAP_STA_REG	0X26C	CSI Channel_2 status register
CSI0_C2_INT_EN_REG	0X270	CSI Channel_2 interrupt enable register
CSI0_C2_INT_STA_REG	0X274	CSI Channel_2 interrupt status register
CSI0_C2_HSIZE_REG	0X280	CSI Channel_2 horizontal size register
CSI0_C2_VSIZE_REG	0X284	CSI Channel_2 vertical size register

CSI0_C2_BUF_LEN_REG	0X288	CSI Channel_2 line buffer length register
CSI0_C2_FLIP_SIZE_REG	0X28C	CSI Channel_2 flip size register
CSI0_C2_FRM_CLK_CNT_REG	0X290	CSI Channel_2 frame clock counter register
CSI0_C2_ACC_ITNL_CLK_CNT_REG	0X294	CSI Channel_2 accumulated and internal clock counter register
CSI0_C3_CFG_REG	0X344	CSI Channel_3 configuration register
CSI0_C3_SCALE_REG	0X34C	CSI Channel_3 scale register
CSI0_C3_F0_BUFA_REG	0X350	CSI Channel_3 FIFO 0 output buffer-A address register
CSI0_C3_F1_BUFA_REG	0X358	CSI Channel_3 FIFO 1 output buffer-A address register
CSI0_C3_F2_BUFA_REG	0X360	CSI Channel_3 FIFO 2 output buffer-A address register
CSI0_C3_C AP_STA_REG	0X36C	CSI Channel_3 status register
CSI0_C3_INT_EN_REG	0X370	CSI Channel_3 interrupt enable register
CSI0_C3_INT_STA_REG	0X374	CSI Channel_3 interrupt status register
CSI0_C3_HSIZE_REG	0X380	CSI Channel_3 horizontal size register
CSI0_C3_VSIZE_REG	0X384	CSI Channel_3 vertical size register
CSI0_C3_BUF_LEN_REG	0X388	CSI Channel_3 line buffer length register
CSI0_C3_FLIP_SIZE_REG	0X38C	CSI Channel_3 flip size register
CSI0_C3_FRM_CLK_CNT_REG	0X390	CSI Channel_3 frame clock counter register
CSI0_C3_ACC_ITNL_CLK_CNT_REG	0X394	CSI Channel_3 accumulated and internal clock counter register

6.1.5. CSI0 REGISTER DESCRIPTION

6.1.5.1. CSI ENABLE REGISTER

Offset Address: 0x0000	Register Name: CSI0_EN_REG

Bit	Read/ Write	Default/Hex	Description
31	/	/	/
30	R/W	0x0	**VER_EN** CSI Version Register Read Enable: 0: Disable 1: Enable
29:24	/	/	/
23:16	R/W	0x00	PTN_CYCLE Pattern generating cycle counter. The pattern in dram will be generated in cycles of PTN_CYCLE+1.
15:5	/	/	/
4	R/W	0x0	PTN_START CSI Pattern Generating Start 0: Finish other: Start Software write this bit to“1” to start pattern generating from DRAM. When finished, the hardware will clear this bit to“0”automatically. Generating cycles depends on PTN_CYCLE.
3	R/W	0	CLK_CNT_SPL Sampling time for clk counter per frame 0: Sampling clock counter every frame done 1: Sampling clock counter every vsync
2	R/W	0	CLK_CNT clk count per frame
1	R/W	0	PTN_GEN_EN Pattern Generation Enable
0	R/W	0	CSI_EN

			Enable 0: Reset and disable the CSI module 1: Enable the CSI module

6.1.5.2. CSI INTERFACE CONFIGURATION REGISTER

Offset Address: 0x0004			Register Name: CSI0_IF_CFG_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	/	/	/
23	R/W	0	CSI_SRC_SWAP 0: normal 1: swap src Normally, Csi0/1 parser the h/v and data to Csi0/1 interface; Enable this bit will swap the signals after Csi1/0 parser to Csi0/1 interface.
22	/	/	/
21	R/W	0	SRC_TYPE Source type 0: Progressed 1: Interlaced
20	R/W	0	FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames
19	R/W	0	FIELD For YUV HV timing, Field polarity 0: negative(field=0 indicate odd, field=1 indicate even) 1: positive(field=1 indicate odd, field=0 indicate even)

			For BT656 timing, Field sequence 0: Normal sequence (field 0 first) 1: Inverse sequence (field 1 first)
18	R/W	1	VREF_POL Vref polarity 0: negative 1: positive This register is not apply to CCIR656 interface.
17	R/W	0	HERF_POL Href polarity 0: negative 1: positive This register is not apply to CCIR656 interface.
16	R/W	1	CLK_POL Data clock type 0: active in falling edge 1: active in rising edge
15:12	/	/	/
11:10	R/W	0	IF_BUS_SEQ
9:8	R/W	0	IF_DATA_WIDTH 00: 8 bit data bus 01: 10 bit data bus 10: 12 bit data bus Others: Reserved
7	R/W	0	MIPI_IF MIPI Interface Enable: 0: CSI 1: MIPI

6:5	/	/	/
4:0	R/W	0	CSI_IF YUV: 00000: YUYV422 Interleaved or RAW (All data in one data bus) 00001: / 00010: / 00011:/ CCIR656: 00100: YUYV422 Interleaved or RAW (All data in one data bus) 00101:/ 00110:/ 00111: / 01100: CCIR656 2 channels (All data interleaved in one data bus) 01101: CCIR656 4 channels (All data interleaved in one data bus) Others: Reserved

6.1.5.3. CSI CAPTURE REGISTER

Offset: 0x0008			Register Name: CSI0_CAP_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:26	R/W	0x00	CH3_CAP_MASK Vsync number masked before capture.
25	R/W	0	CH3_VCAP_ON Video capture control: Capture the video image data stream on

			channel 3. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
24	R/W	0	CH3_SCAP_ON Still capture control: Capture a single still image frame on channel 3. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self clearing and always reads as a 0.
23:22	/	/	/
21:18	R/W	0x00	CH2_CAP_MASK Vsync number masked before capture.
17	R/W	0	CH2_VCAP_ON Video capture control: Capture the video image data stream on channel 2. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
16	R/W	0	CH2_SCAP_ON Still capture control: Capture a single still image frame on channel 2.

			0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self clearing and always reads as a 0.
15:14	/	/	/
13:10	R/W	0x00	CH1_CAP_MASK Vsync number masked before capture.
09	R/W	0	CH1_VCAP_ON Video capture control: Capture the video image data stream on channel 1. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
08	R/W	0	CH1_SCAP_ON Still capture control: Capture a single still image frame on channel 1. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self clearing and always reads as a 0.
07:06	/	/	/
05:02	R/W	0x00	CH0_CAP_MASK Vsync number masked before capture.
01	R/W	0	CH0_VCAP_ON

			Video capture control: Capture the video image data stream on channel 0. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
00	R/W	0	CH0_SCAP_ON Still capture control: Capture a single still image frame on channel 0. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self clearing and always reads as a 0.

6.1.5.4. CSI SYNCHRONIZATION COUNTER REGISTER

Offset Address: 0x000c			Register Name: CSI0_SYNC_CNT_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:00	R	0	SYNC_CNT The counter value between vsync of Csi0 channel 0 and vsync of Csi1 channel 0 , using 24MHz.

6.1.5.5. CSI FIFO THRESHOLD REGISTER

Offset Address: 0x0010			Register Name: CSI0_FIFO_THRS_REG
Bit	**Read/**	**Default/Hex**	**Description**

	Write		
31:24	/	/	/
23:16	R/W	0x0f	PTN_GEN_DLY Clocks delayed before pattern generating start.
15:12	/	/	/
11:00	R/W	0x400	FIFO_THRS When CSI0 FIFO occupied memory exceed the threshold, dram frequency can not change.

6.1.5.6. CSI PATTERN GENERATION LENGTH REGISTER

Offset: 0x0030			Register Name: CSI0_PTN_LEN_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	PTN_LEN The pattern length in byte when generating pattern.

6.1.5.7. CSI PATTERN GENERATION ADDRESS REGISTER

Offset: 0x0034			Register Name: CSI0_PTN_ADDR_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	PTN_ADDR The pattern DRAM address when generating pattern.

6.1.5.8. CSI VERSION REGISTER

Offset: 0x003C			Register Name: CSI0_VER_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:0	R/W	/	VER

			Version of hardware circuit. Only can be read when version register read enable is on.

6.1.5.9. CSI CHANNEL_0 CONFIGURATION REGISTER

Offset Address: 0X0044			**Register Name: CSI0_C0_CFG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00~0xff
23:20	R/W	3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved
19:16	R/W	0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: field-raw-8 0001: field-raw-10 0010: field-raw-12 0011: reserved 0100: field-rgb565 0101: field-rgb888 0110: field-prgb888 0111: field-uv-combined

			1000: frame-raw-8 1001: frame-raw-10 1010: frame-raw-12 1011: reserved 1100: frame-rgb565 1101: frame-rgb888 1110: frame-prgb888 1111: frame-uv-combined When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: frame planar YCbCr 422 UV combined 1000: field MB YCbCr 422 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: frame MB YCbCr 422 1100: field planar YCbCr 422 10bit UV combined 1101: field planar YCbCr 420 10bit UV combined 1110: Reserved 1111: Reserved When the input format is set YUV420 0000: Reserved

			0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: Reserved 0100: Reserved 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: Reserved 1000: Reserved 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: Reserved 1100: Reserved 1101: field planar YCbCr 420 10bit UV combined 1110: Reserved 1111: Reserved Others: reserved
15:14	/	/	/
13	R/W	0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0:Disable 1:Enable
12	R/W	0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0:Disable 1:Enable

11:10	R/W	0	FIELD_SEL Field selection. 00: capturing with field 1. 01: capturing with field 2. 10: capturing with either field. 11: reserved
09:08	R/W	2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU
07:00	/	/	/

6.1.5.10. CSI CHANNEL_0 SCALE REGISTER

Offset Address: 0X004C			**Register Name: CSI0_C0_SCALE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:01	/	/	/
00	R/W	0	QUART_EN When this bit is set to 1, input image will be decimated to quarter size. All input format are supported.

6.1.5.11. CSI CHANNEL_0 FIFO 0 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0050			Register Name: CSI0_C0_F0_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C0F0_BUFA FIFO 0 output buffer-A address

6.1.5.12. CSI CHANNEL_0 FIFO 1 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0058			Register Name: CSI0_C0_F1_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C0F1_BUFA FIFO 1 output buffer-A address

6.1.5.13. CSI CHANNEL_0 FIFO 2 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0060			Register Name: CSI0_C0_F2_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C0F2_BUFA FIFO 2 output buffer-A address

6.1.5.14. CSI CHANNEL_0 STATUS REGISTER

Offset Address: 0X006C			Register Name: CSI0_C0_CAP_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:03	/	/	/
02	R	0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
01	R	0	VCAP_STA

			Video capture in progress Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabling video capture. When software disables video capture, it clears itself after the last pixel of the current frame is captured.
00	R	0	SCAP_STA Still capture in progress Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabling still frame capture. It clears itself after the last pixel of the first frame is captured. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means filed end.

6.1.5.15. CSI CHANNEL_0 INTERRUPT ENABLE REGISTER

Offset Address: 0X0070			**Register Name: CSI0_C0_INT_EN_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:08	/	/	/
07	R/W	0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
06	R/W	0	HB_OF_INT_EN Hblank FIFO overflow The bit is set when 3 FIFOs still overflow after the hblank.
05	R/W	0	MUL_ERR_INT_EN

			Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
04	R/W	0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
03	R/W	0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.
02	R/W	0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
01	R/W	0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is written to buffer as long as video capture remains enabled.
00	R/W	0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been written to buffer. For video capture, the bit is set when the last frame has been written to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

6.1.5.16. CSI CHANNEL_0 INTERRUPT STATUS REGISTER

Offset Address: 0X0074			Register Name: CSI0_C0_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:08	/	/	/
07	R/W	0	VS_PD vsync flag
06	R/W	0	HB_OF_PD Hblank FIFO overflow
05	R/W	0	MUL_ ERR_PD Multi-channel writing error
04	R/W	0	FIFO2_OF_PD FIFO 2 overflow
03	R/W	0	FIFO1_OF_PD FIFO 1 overflow
02	R/W	0	FIFO0_OF_PD FIFO 0 overflow
01	R/W	0	FD_PD Frame done
00	R/W	0	CD_PD Capture done

6.1.5.17. CSI CHANNEL_0 HORIZONTAL SIZE REGISTER

Offset Address: 0X0080			Register Name: CSI0_C0_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	500	HOR_LEN Horizontal pixel clock length. Valid pixel clocks of a line.
15:13	/	/	/

12:00	R/W	0	HOR_START Horizontal pixel unit start. Pixel is valid from this unit.

6.1.5.18. CSI CHANNEL_0 VERTICAL SIZE REGISTER

Offset Address: 0X0084			**Register Name: CSI0_C0_VSIZE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	1E0	VER_LEN Vertical line length. Valid line number of a frame.
15:13	/	/	/
12:00	R/W	0	VER_START Vertical line start. Data is valid from this line.

6.1.5.19. CSI CHANNEL_0 BUFFER LENGTH REGISTER

Offset Address: 0X0088			**Register Name: CSI0_C0_BUF_LEN_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	140	BUF_LEN_C Buffer length of chroma C in a line. Unit is byte.
15:13	/	/	/
12:00	R/W	280	BUF_LEN Buffer length of luminance Y in a line. Unit is byte.

6.1.5.20. CSI CHANNEL_0 FLIP SIZE REGISTER

Offset Address: 0X008C			**Register Name: CSI0_C0_FLIP_SIZE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	1E0	VER_LEN

			Vertical line number when in vflip mode.
15:13	/	/	/
12:00	R/W	280	VALID_LEN Valid components of a line when in flip mode.

6.1.5.21. CSI CHANNEL_0 FRAME CLOCK COUNTER REGISTER

Offset Address: 0x0090			Register Name: CSI0_C0_FRM_CLK_CNT_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:00	R	0	FRM_CLK_CNT Counter value between every frame. For instant hardware frame rate statics. The internal counter is added by one every 24MHz clock cycle. When frame done or vsync comes, the internal counter value is sampled to FRM_CLK_CNT, and cleared to 0.

6.1.5.22. CSI CHANNEL_0 ACCUMULATED AND INTERNAL CLOCK COUNTER REGISTER

Offset Address: 0x0094			Register Name: CSI0_C0_ACC_ITNL_CLK_CNT_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	R/W	0	ACC_CLK_CNT The accumulated value of FRM_CLK_CNT for software frame rate statics. Every interrupt of frame done, the software check this accumulated value and clear it to 0. If the ACC_CLK_CNT is larger than 1, the software has lost frame.

			When frame done or vsync comes, ACC_CLK_CNT = ACC_CLK_CNT + 1, and cleared to 0 when writing 0 to this register.
23:00	R	0	ITNL_CLK_CNT The instant value of internal frame clock counter. When frame done interrupt comes, the software can query this counter for judging whether it is the time for updating the double buffer address registers.

6.1.5.23. CSI CHANNEL_1 CONFIGURATION REGISTER

Offset Address: 0X0144			**Register Name: CSI0_C1_CFG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00~0xff
23:20	R/W	3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved
19:16	R/W	0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: field-raw-8 0001: field-raw-10

			0010: field-raw-12 0011: reserved 0100: field-rgb565 0101: field-rgb888 0110: field-prgb888 0111: field-uv-combined 1000: frame-raw-8 1001: frame-raw-10 1010: frame-raw-12 1011: reserved 1100: frame-rgb565 1101: frame-rgb888 1110: frame-prgb888 1111: frame-uv-combined When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: frame planar YCbCr 422 UV combined 1000: field MB YCbCr 422 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: frame MB YCbCr 422 1100: field planar YCbCr 422 10bit UV combined

			1101: field planar YCbCr 420 10bit UV combined 1110: Reserved 1111: Reserved When the input format is set YUV420 0000: Reserved 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: Reserved 0100: Reserved 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: Reserved 1000: Reserved 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: Reserved 1100: Reserved 1101: field planar YCbCr 420 10bit UV combined 1110: Reserved 1111: Reserved Others: reserved
15:14	/	/	/
13	R/W	0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0:Disable 1:Enable

12	R/W	0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0:Disable 1:Enable
11:10	R/W	0	FIELD_SEL Field selection. 00: capturing with field 1. 01: capturing with field 2. 10: capturing with either field. 11: reserved
09:08	R/W	2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU
07:00	/	/	/

6.1.5.24. CSI CHANNEL_1 SCALE REGISTER

Offset Address: 0X014C			Register Name: CSI0_C1_SCALE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:01	/	/	/
00	R/W	0	QUART_EN When this bit is set to 1, input image will be decimated to quarter size. All input format are supported.

6.1.5.25. CSI CHANNEL_1 FIFO 0 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0150			Register Name: CSI0_C1_F0_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C1F0_BUFA FIFO 0 output buffer-A address

6.1.5.26. CSI CHANNEL_1 FIFO 1 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0158			Register Name: CSI0_C1_F1_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C1F1_BUFA FIFO 1 output buffer-A address

6.1.5.27. CSI CHANNEL_1 FIFO 2 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0160			Register Name: CSI0_C1_F2_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C1F2_BUFA FIFO 2 output buffer-A address

6.1.5.28. CSI CHANNEL_1 STATUS REGISTER

Offset Address: 0X016C			Register Name: CSI0_C1_CAP_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:03	/	/	/
02	R	0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
01	R	0	VCAP_STA Video capture in progress Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabling video capture. When software disables video capture, it clears itself after the last pixel of the current frame is captured.
00	R	0	SCAP_STA Still capture in progress Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabling still frame capture. It clears itself after the last pixel of the first frame is captured. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means filed end.

6.1.5.29. CSI CHANNEL_1 INTERRUPT ENABLE REGISTER

Offset Address: 0X0170			Register Name: CSI0_C1_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:08	/	/	/

07	R/W	0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
06	R/W	0	HB_OF_INT_EN Hblank FIFO overflow The bit is set when 3 FIFOs still overflow after the hblank.
05	R/W	0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
04	R/W	0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
03	R/W	0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.
02	R/W	0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
01	R/W	0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is written to buffer as long as video capture remains enabled.
00	R/W	0	CD_INT_EN

			Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been written to buffer. For video capture, the bit is set when the last frame has been written to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

6.1.5.30. CSI CHANNEL_1 INTERRUPT STATUS REGISTER

Offset Address: 0X0174			**Register Name: CSI0_C1_INT_STA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:08	/	/	/
07	R/W	0	VS_PD vsync flag
06	R/W	0	HB_OF_PD Hblank FIFO overflow
05	R/W	0	MUL_ ERR_PD Multi-channel writing error
04	R/W	0	FIFO2_OF_PD FIFO 2 overflow
03	R/W	0	FIFO1_OF_PD FIFO 1 overflow
02	R/W	0	FIFO0_OF_PD FIFO 0 overflow
01	R/W	0	FD_PD Frame done

00	R/W	0	CD_PD Capture done

6.1.5.31. CSI CHANNEL_1 HORIZONTAL SIZE REGISTER

Offset Address: 0X0180			Register Name: CSI0_C1_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	500	HOR_LEN Horizontal pixel clock length. Valid pixel clocks of a line.
15:13	/	/	/
12:00	R/W	0	HOR_START Horizontal pixel clock start.Pixel data is valid from this clock.

6.1.5.32. CSI CHANNEL_1 VERTICAL SIZE REGISTER

Offset Address: 0X0184			Register Name: CSI0_C1_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	1E0	VER_LEN Vertical line length. Valid line number of a frame.
15:13	/	/	/
12:00	R/W	0	VER_START Vertical line start. data is valid from this line.

6.1.5.33. CSI CHANNEL_1 BUFFER LENGTH REGISTER

Offset Address: 0X0188			Register Name: CSI0_C1_BUF_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	140	BUF_LEN_C

			Buffer length of chroma C in a line. Unit is byte.
15:13	/	/	/
12:00	R/W	280	BUF_LEN Buffer length of luminance Y in a line. Unit is byte.

6.1.5.34. CSI CHANNEL_1 FLIP SIZE REGISTER

Offset Address: 0X018C			**Register Name: CSI0_C1_FLIP_SIZE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	1E0	VER_LEN Vertical line number when in vflip mode.
15:13	/	/	/
12:00	R/W	280	VALID_LEN Valid components of a line when in flip mode.

6.1.5.35. CSI CHANNEL_1 FRAME CLOCK COUNTER REGISTER

Offset Address: 0x0190			**Register Name: CSI0_C1_FRM_CLK_CNT_REG**
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:00	R	0	FRM_CLK_CNT Counter value between every frame. For instant hardware frame rate statics. The internal counter is added by one every 24MHz clock cycle. When frame done or vsync comes, the internal counter value is sampled to FRM_CLK_CNT, and cleared to 0. Then the FRM_CLK_CNT is added to ACC_CLK_CNT.

6.1.5.36. CSI CHANNEL_1 ACCUMULATED AND INTERNAL CLOCK COUNTER REGISTER

Offset Address: 0x0194			Register Name: CSI0_C1_ACC_ITNL_CLK_CNT_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	R/W	0	ACC_CLK_CNT The accumulated value of FRM_CLK_CNT for software frame rate statics. Every interrupt of frame done, the software check this accumulated value and clear it to 0. If the ACC_CLK_CNT is larger than 1, the software has lost frame. When frame done or vsync comes, ACC_CLK_CNT = ACC_CLK_CNT + 1, and cleared to 0 when writing 0 to this register.
23:00	R	0	ITNL_CLK_CNT The instant value of internal frame clock counter. When frame done interrupt comes, the software can query this counter for judging whether it is the time for updating the double buffer address registers.

6.1.5.37. CSI CHANNEL_2 CONFIGURATION REGISTER

Offset Address: 0X0244			Register Name: CSI0_C2_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00~0xff
23:20	R/W	3	INPUT_FMT Input data format 0000: RAW stream

			0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved
19:16	R/W	0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: field-raw-8 0001: field-raw-10 0010: field-raw-12 0011: reserved 0100: field-rgb565 0101: field-rgb888 0110: field-prgb888 0111: field-uv-combined 1000: frame-raw-8 1001: frame-raw-10 1010: frame-raw-12 1011: reserved 1100: frame-rgb565 1101: frame-rgb888 1110: frame-prgb888 1111: frame-uv-combined When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420

			0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: frame planar YCbCr 422 UV combined 1000: field MB YCbCr 422 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: frame MB YCbCr 422 1100: field planar YCbCr 422 10bit UV combined 1101: field planar YCbCr 420 10bit UV combined 1110: Reserved 1111: Reserved When the input format is set YUV420 0000: Reserved 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: Reserved 0100: Reserved 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: Reserved 1000: Reserved 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: Reserved 1100: Reserved 1101: field planar YCbCr 420 10bit UV combined

			1110: Reserved 1111: Reserved Others: reserved
15:14	/	/	/
13	R/W	0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0:Disable 1:Enable
12	R/W	0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0:Disable 1:Enable
11:10	R/W	0	FIELD_SEL Field selection. 00: capturing with field 1. 01: capturing with field 2. 10: capturing with either field. 11: reserved
09:08	R/W	2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV

			01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU
07:00	/	/	/

6.1.5.38. CSI CHANNEL_2 SCALE REGISTER

Offset Address: 0X024C			Register Name: CSI0_C2_SCALE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:01	/	/	/
00	R/W	0	QUART_EN When this bit is set to 1, input image will be decimated to quarter size. All input format are supported.

6.1.5.39. CSI CHANNEL_2 FIFO 0 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0250			Register Name: CSI0_C2_F0_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C2F0_BUFA FIFO 0 output buffer-A address

6.1.5.40. CSI CHANNEL_2 FIFO 1 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0258			Register Name: CSI0_C2_F1_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C2F1_BUFA FIFO 1 output buffer-A address

6.1.5.41. CSI CHANNEL_2 FIFO 2 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0260			Register Name: CSI0_C2_F2_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C2F2_BUFA FIFO 2 output buffer-A address

6.1.5.42. CSI CHANNEL_2 STATUS REGISTER

Offset Address: 0X026C			Register Name: CSI0_C2_CAP_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:03	/	/	/
02	R	0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
01	R	0	VCAP_STA Video capture in progress Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabling video capture. When software disables video capture, it clears itself after the last pixel of the current frame is captured.
00	R	0	SCAP_STA Still capture in progress Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabling still frame capture. It clears itself after the last pixel of the first frame is captured. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other

			frame end means filed end.

6.1.5.43. CSI CHANNEL_2 INTERRUPT ENABLE REGISTER

Offset Address: 0X0270			**Register Name: CSI0_C2_INT_EN_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:08	/	/	/
07	R/W	0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
06	R/W	0	HB_OF_INT_EN Hblank FIFO overflow The bit is set when 3 FIFOs still overflow after the hblank.
05	R/W	0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
04	R/W	0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
03	R/W	0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.
02	R/W	0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
01	R/W	0	FD_INT_EN

			Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is written to buffer as long as video capture remains enabled.
00	R/W	0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been written to buffer. For video capture, the bit is set when the last frame has been written to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

6.1.5.44. CSI CHANNEL_2 INTERRUPT STATUS REGISTER

Offset Address: 0X0274			**Register Name: CSI0_C2_INT_STA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:08	/	/	/
07	R/W	0	VS_PD vsync flag
06	R/W	0	HB_OF_PD Hblank FIFO overflow
05	R/W	0	MUL_ ERR_PD Multi-channel writing error
04	R/W	0	FIFO2_OF_PD FIFO 2 overflow

03	R/W	0	FIFO1_OF_PD FIFO 1 overflow
02	R/W	0	FIFO0_OF_PD FIFO 0 overflow
01	R/W	0	FD_PD Frame done
00	R/W	0	CD_PD Capture done

6.1.5.45. CSI CHANNEL_2 HORIZONTAL SIZE REGISTER

Offset Address: 0X0280			**Register Name: CSI0_C2_HSIZE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	500	HOR_LEN Horizontal pixel clock length. Valid pixel clocks of a line.
15:13	/	/	/
12:00	R/W	0	HOR_START Horizontal pixel clock start. Pixel data is valid from this clock.

6.1.5.46. CSI CHANNEL_2 VERTICAL SIZE REGISTER

Offset Address: 0X0284			**Register Name: CSI0_C2_VSIZE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	1E0	VER_LEN Vertical line length. Valid line number of a frame.
15:13	/	/	/
12:00	R/W	0	VER_START Vertical line start. data is valid from this line.

6.1.5.47. CSI CHANNEL_2 BUFFER LENGTH REGISTER

Offset Address: 0X0288			Register Name: CSI0_C2_BUF_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	140	BUF_LEN_C Buffer length of chroma C in a line. Unit is byte.
15:13	/	/	/
12:00	R/W	280	BUF_LEN Buffer length of luminance Y in a line. Unit is byte.

6.1.5.48. CSI CHANNEL_2 FLIP SIZE REGISTER

Offset Address: 0X028C			Register Name: CSI0_C2_FLIP_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	1E0	VER_LEN Vertical line number when in vflip mode.
15:13	/	/	/
12:00	R/W	280	VALID_LEN Valid components of a line when in flip mode.

6.1.5.49. CSI CHANNEL_2 FRAME CLOCK COUNTER REGISTER

Offset Address: 0x0290			Register Name: CSI0_C2_FRM_CLK_CNT_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:00	R	0	FRM_CLK_CNT Counter value between every frame. For instant hardware frame rate

			statics. The internal counter is added by one every 24MHz clock cycle. When frame done or vsync comes, the internal counter value is sampled to FRM_CLK_CNT, and cleared to 0. Then the FRM_CLK_CNT is added to ACC_CLK_CNT.

6.1.5.50. CSI CHANNEL_2 ACCUMULATED AND INTERNAL CLOCK COUNTER REGISTER

Offset Address: 0x0294			Register Name: CSI0_C2_ACC_ITNL_CLK_CNT_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	R/W	0	ACC_CLK_CNT The accumulated value of FRM_CLK_CNT for software frame rate statics. Every interrupt of frame done, the software check this accumulated value and clear it to 0. If the ACC_CLK_CNT is larger than 1, the software has lost frame. When frame done or vsync comes, ACC_CLK_CNT = ACC_CLK_CNT + 1, and cleared to 0 when writing 0 to this register.
23:00	R	0	ITNL_CLK_CNT The instant value of internal frame clock counter. When frame done interrupt comes, the software can query this counter for judging whether it is the time for updating the double buffer address registers.

6.1.5.51. CSI CHANNEL_3 CONFIGURATION REGISTER

Offset Address: 0X0344	Register Name: CSI0_C3_CFG_REG

Bit	Read/Write	Default/Hex	Description
31:24	R/W	0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00~0xff
23:20	R/W	3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved
19:16	R/W	0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: field-raw-8 0001: field-raw-10 0010: field-raw-12 0011: reserved 0100: field-rgb565 0101: field-rgb888 0110: field-prgb888 0111: field-uv-combined 1000: frame-raw-8 1001: frame-raw-10 1010: frame-raw-12 1011: reserved 1100: frame-rgb565 1101: frame-rgb888

			1110: frame-prgb888 1111: frame-uv-combined When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: frame planar YCbCr 422 UV combined 1000: field MB YCbCr 422 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: frame MB YCbCr 422 1100: field planar YCbCr 422 10bit UV combined 1101: field planar YCbCr 420 10bit UV combined 1110: Reserved 1111: Reserved When the input format is set YUV420 0000: Reserved 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: Reserved 0100: Reserved 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined

			0111: Reserved 1000: Reserved 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: Reserved 1100: Reserved 1101: field planar YCbCr 420 10bit UV combined 1110: Reserved 1111: Reserved Others: reserved
15:14	/	/	/
13	R/W	0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0:Disable 1:Enable
12	R/W	0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0:Disable 1:Enable
11:10	R/W	0	FIELD_SEL Field selection. 00: capturing with field 1. 01: capturing with field 2. 10: capturing with either field.

			11: reserved
09:08	R/W	2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU
07:00	/	/	/

6.1.5.52. CSI CHANNEL_3 SCALE REGISTER

Offset Address: 0X034C			**Register Name: CSI0_C3_SCALE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:01	/	/	/
00	R/W	0	QUART_EN When this bit is set to 1, input image will be decimated to quarter size. All input format are supported.

6.1.5.53. CSI CHANNEL_3 FIFO 0 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0350			**Register Name: CSI0_C3_F0_BUFA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C3F0_BUFA

			FIFO 0 output buffer-A address

6.1.5.54. CSI CHANNEL_3 FIFO 1 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0358			**Register Name: CSI0_C3_F1_BUFA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C3F1_BUFA FIFO 1 output buffer-A address

6.1.5.55. CSI CHANNEL_3 FIFO 2 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0360			**Register Name: CSI0_C3_F2_BUFA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C3F2_BUFA FIFO 2 output buffer-A address

6.1.5.56. CSI CHANNEL_3 STATUS REGISTER

Offset Address: 0X036C			**Register Name: CSI0_C3_CAP_STA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:03	/	/	/
02	R	0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
01	R	0	VCAP_STA Video capture in progress Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabling video capture. When software disables video capture, it clears

			itself after the last pixel of the current frame is captured.
00	R	0	SCAP_STA Still capture in progress Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabling still frame capture. It clears itself after the last pixel of the first frame is captured. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means filed end.

6.1.5.57. CSI CHANNEL_3 INTERRUPT ENABLE REGISTER

Offset Address: 0X0370			**Register Name: CSI0_C3_INT_EN_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:08	/	/	/
07	R/W	0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
06	R/W	0	HB_OF_INT_EN Hblank FIFO overflow The bit is set when 3 FIFOs still overflow after the hblank.
05	R/W	0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
04	R/W	0	FIFO2_OF_INT_EN

			FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
03	R/W	0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.
02	R/W	0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
01	R/W	0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is written to buffer as long as video capture remains enabled.
00	R/W	0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been written to buffer. For video capture, the bit is set when the last frame has been written to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

6.1.5.58. CSI CHANNEL_3 INTERRUPT STATUS REGISTER

Offset Address: 0X0374			**Register Name: CSI0_C3_INT_STA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**

31:08	/	/	/
07	R/W	0	VS_PD vsync flag
06	R/W	0	HB_OF_PD Hblank FIFO overflow
05	R/W	0	MUL_ ERR_PD Multi-channel writing error
04	R/W	0	FIFO2_OF_PD FIFO 2 overflow
03	R/W	0	FIFO1_OF_PD FIFO 1 overflow
02	R/W	0	FIFO0_OF_PD FIFO 0 overflow
01	R/W	0	FD_PD Frame done
00	R/W	0	CD_PD Capture done

6.1.5.59. CSI CHANNEL_3 HORIZONTAL SIZE REGISTER

Offset Address: 0X0380			**Register Name: CSI0_C3_HSIZE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	500	HOR_LEN Horizontal pixel clock length. Valid pixel clocks of a line.
15:13	/	/	/
12:00	R/W	0	HOR_START Horizontal pixel clock start.Pixel data is valid from this clock.

6.1.5.60. CSI CHANNEL_3 VERTICAL SIZE REGISTER

Offset Address: 0X0384			Register Name: CSI0_C3_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	1E0	VER_LEN Vertical line length. Valid line number of a frame.
15:13	/	/	/
12:00	R/W	0	VER_START Vertical line start. data is valid from this line.

6.1.5.61. CSI CHANNEL_3 BUFFER LENGTH REGISTER

Offset Address: 0X0388			Register Name: CSI0_C3_BUF_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	140	BUF_LEN_C Buffer length of chroma C in a line. Unit is byte.
15:13	/	/	/
12:00	R/W	280	BUF_LEN Buffer length of luminance Y in a line. Unit is byte.

6.1.5.62. CSI CHANNEL_3 FLIP SIZE REGISTER

Offset Address: 0X038C			Register Name: CSI0_C3_FLIP_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	1E0	VER_LEN Vertical line number when in vflip mode.
15:13	/	/	/
12:00	R/W	280	VALID_LEN

			Valid components of a line when in flip mode.

6.1.5.63. CSI CHANNEL_3 FRAME CLOCK COUNTER REGISTER

Offset Address: 0x0390			Register Name: CSI0_C3_FRM_CLK_CNT_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:00	R	0	FRM_CLK_CNT Counter value between every frame. For instant hardware frame rate statics. The internal counter is added by one every 24MHz clock cycle. When frame done or vsync comes, the internal counter value is sampled to FRM_CLK_CNT, and cleared to 0. Then the FRM_CLK_CNT is added to ACC_CLK_CNT.

6.1.5.64. CSI CHANNEL_3 ACCUMULATED AND INTERNAL CLOCK COUNTER REGISTER

Offset Address: 0x0394			Register Name: CSI0_C3_ACC_ITNL_CLK_CNT_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	R/W	0	ACC_CLK_CNT The accumulated value of FRM_CLK_CNT for software frame rate statics. Every interrupt of frame done, the software check this accumulated value and clear it to 0. If the ACC_CLK_CNT is larger than 1, the software has lost frame. When frame done or vsync comes, ACC_CLK_CNT =

			ACC_CLK_CNT + 1, and cleared to 0 when writing 0 to this register.
23:00	R	0	ITNL_CLK_CNT The instant value of internal frame clock counter. When frame done interrupt comes, the software can query this counter for judging whether it is the time for updating the double buffer address registers.

6.2. CSI1

6.2.1. OVERVIEW

Normal CSI is routed to CSI1 module.

CSI1 module features:

- Support CMOS-sensor parallel interface with HREF and VSYNC
- Support CCIR656 protocol for NTSC and PAL
- Support multi-channel ITU-R BT.656 time-multiplexed format
- Support 8/10/12bit raw data input
- Support 8/10 bit yuv422 data input
- Pass raw data direct to memory or to ISP
- Parsing YUV data into planar or semi-planar output to memory
- Support CMOS-sensor and TV decoder
- Support up to 1080p@30fps or 5M@15fps using SOC CMOS-sensor with YUV format
- Support up to 1080p@60fps or 5M@30fps using CMOS-sensor with RAW format

6.2.2. CSI 1 BLOCK DIAGRAM

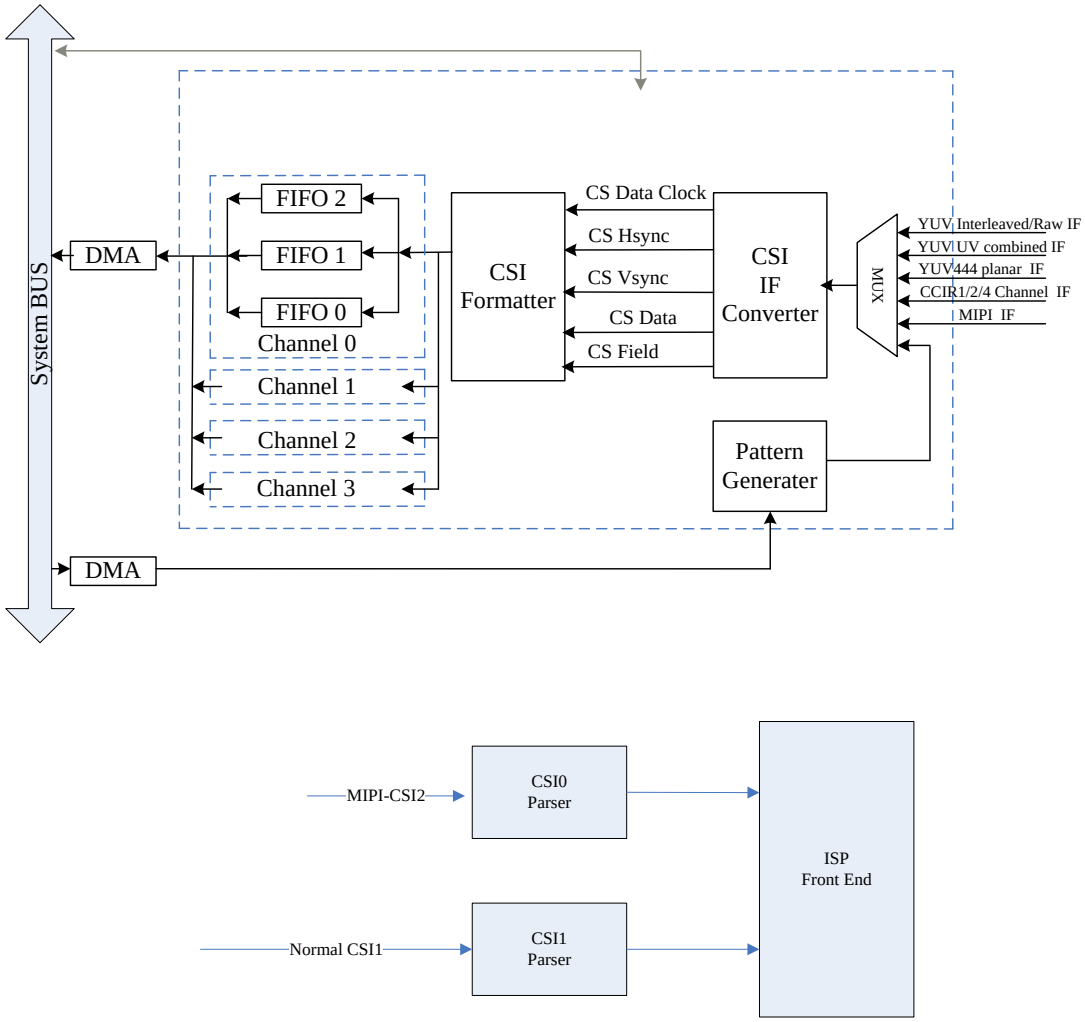


Figure 6-2 CSI1 Block Diagram

6.2.3. CSI1 MODULE DESCRIPTION

6.2.3.1. CSI FIFO DISTRIBUTION

Interface	YUYV422 Interleaved/RAW			YUV422 UV Combined	YUV444 Planar	YUV444 Planar to YUV422 UV Combined
Input format	YUV422		Raw	Raw	Raw	Raw
Output format	Planar	UV combined/ MB	Raw/RGB /PRGB	Raw	Raw	Raw
CH0_FIFO0	Y pixel data	Y pixel data	All pixels data	Y pixel data	Y pixel data	Y pixel data
CH0_FIFO1	Cb (U) pixel data	Cb (U) Cr (V) pixel data	-	-	-	-

CH0_FIFO2	Cr (V) pixel data	-	-	-	-	-
CH1_FIFO0	-	-	-	Cb (U) Cr (V) pixel data	Cb (U) pixel data	Cb (U) Cr (V) pixel data
CH2_FIFO0	-	-	-	-	Cr(V) pixel data	-

Interface	**BT656 Interface**		**Channels**		
Input format	YUV422				
Output format	Planar	UV combined/ MB			
CH0_FIFO0	Y	Y	1	2	4
CH0_FIFO1	Cb (U)	CbCr (UV)			
CH0_FIFO2	Cr (V)	-			
CH1_FIFO0	Y	Y	-		
CH1_FIFO1	Cb (U)	CbCr (UV)			
CH1_FIFO2	Cr (V)	-			
CH2_FIFO0	Y	Y		-	
CH2_FIFO1	Cb (U)	CbCr (UV)			
CH2_FIFO2	Cr (V)	-			
CH3_FIFO0	Y	Y			
CH3_FIFO1	Cb (U)	CbCr (UV)			
CH3_FIFO2	Cr (V)	-			

Interface	**MIPI Interface**			**Channels**			
Input format	YUV422/YUV420		Raw				
Output format	Planar	UV combined/ MB	Pass-Through /Padding				
CH0_FIFO0	Y	Y	All pixels data	1	2	3	4
CH0_FIFO1	Cb (U)	CbCr (UV)	-				
CH0_FIFO2	Cr (V)	-	-				

CH1_FIFO0	Y	Y	All pixels data	-			
CH1_FIFO1	Cb (U)	CbCr (UV)	-				
CH1_FIFO2	Cr (V)	-	-				
CH2_FIFO0	Y	Y	All pixels data		-		
CH2_FIFO1	Cb (U)	CbCr (UV)	-				
CH2_FIFO2	Cr (V)	-	-				
CH3_FIFO0	Y	Y	All pixels data			-	
CH3_FIFO1	Cb (U)	CbCr (UV)	-				
CH3_FIFO2	Cr (V)	-	-				

6.2.3.2. PIXEL FORMAT ARRANGEMENT

RAW-10:

Dummy1[5:0]	Raw data 1[9:0]	Dummy 0[5:0]	Raw data 0[9:0]

MSB LSB

RAW-12:

Dummy1[3:0]	Raw data 1[11:0]	Dummy 0[3:0]	Raw data 0[11:0]

MSB LSB

YUV-10:

Y:

Dummy1[5:0]	Y1[9:0]	Dummy 0[5:0]	Y 0[9:0]

MSB LSB

UV Combined:

Dummy1[5:0]	V/U 0[9:0]	Dummy 0[5:0]	U/V 0[9:0]

MSB LSB

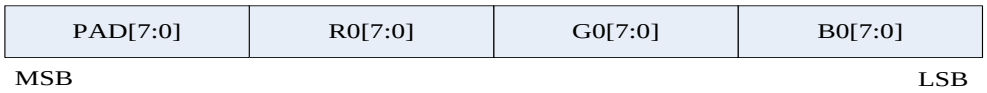
RGB8

88:

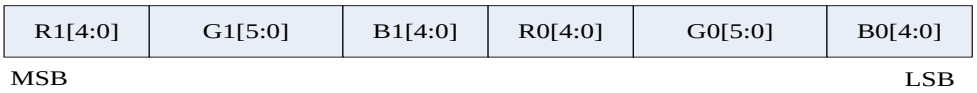
B1[7:0]	R0[7:0]	G0[7:0]	B0[7:0]
G2[7:0]	B2[7:0]	R1[7:0]	G1[7:0]
R3[7:0]	G3[7:0]	B3[7:0]	R2[7:0]

MSB

PRGB888:



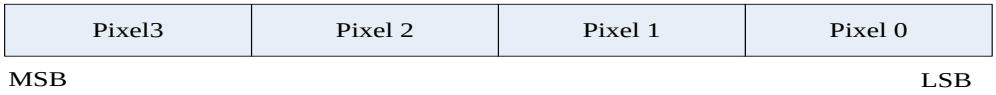
RGB565:



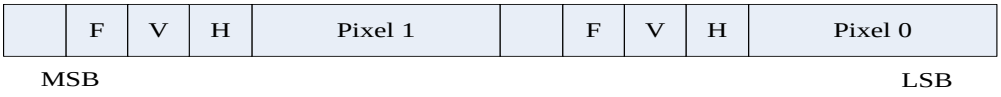
6.2.3.3. PATTERN GENERATING FORMAT

The pattern generated from DRAM is arranged as followed:

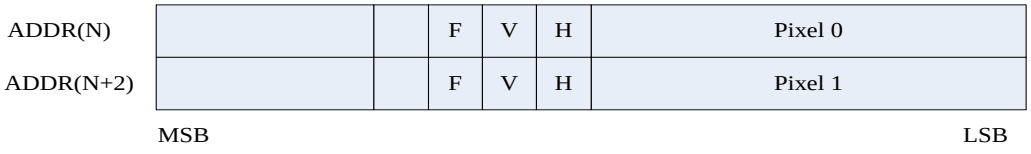
BT656 Interface:



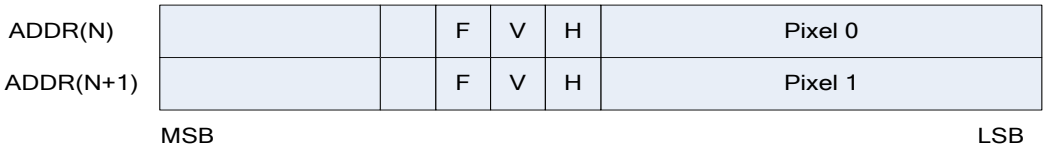
YUV422 Interleaved or RAW Interface:



YUV422 Interleaved or RAW Interface(10bit or 12 bit data bus):



YUV422 UV combined Interface:



YUV444 Planar Interface:

MIPI:

Packet byte flag is 0 indicates that the packet byte is the valid content.

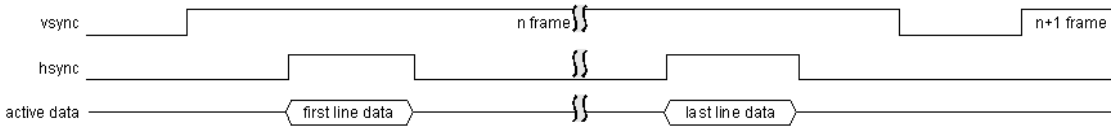
Packet byte flag is 1 indicates that the packet byte is the blanking.

Packet Byte 1 flag	Packet Byte 1	Packet Byte 0 flag	Packet Byte 0

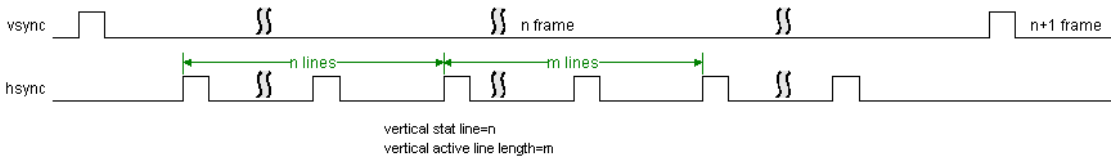
MSB LSB

6.2.3.4. TIMING

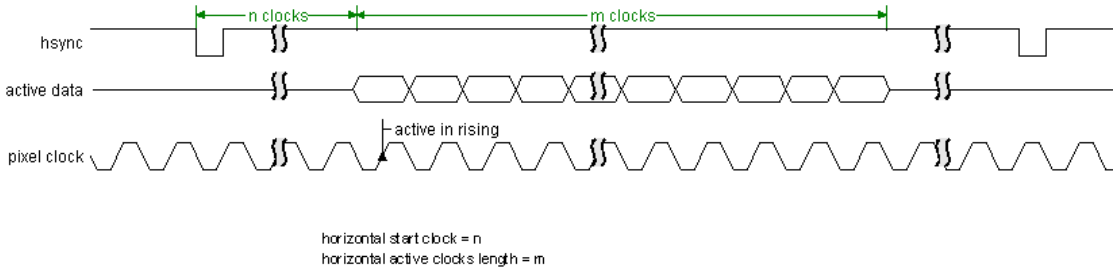
CSI timing



Vref= positive; Href= positive

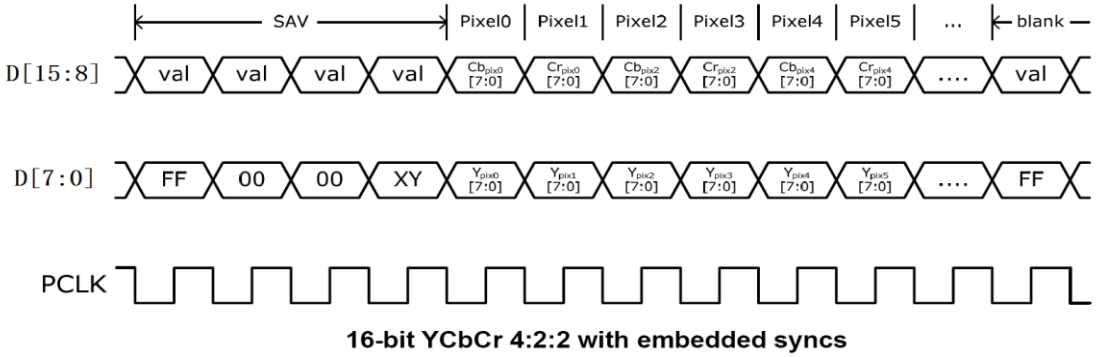


vertical size setting



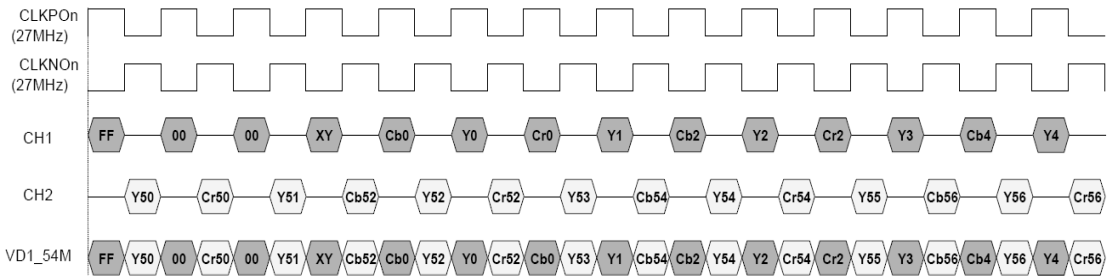
horizontal size setting and pixel clock timing(Href= positive)

16bit YUV422 Timing

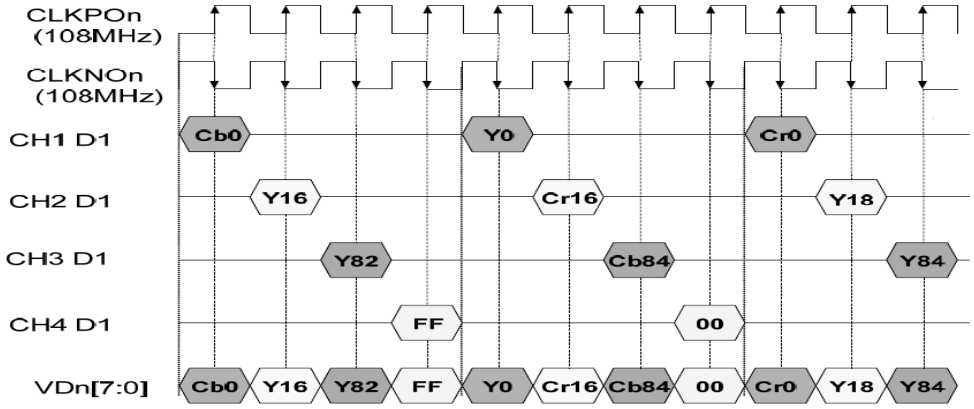


16-bit YCbCr 4:2:2 with embedded syncs

CCIR656 2 channel Timing



CCIR656 4 channel Timing



CCIR656 Header Code

CCIR656 Header Data Bit Definition

Data Bit	First Word(0xFF)	Second Word(0x00)	Third Word(0x00)	Fourth Word
CS D[9] (MSB)	**1**	**0**	**0**	**1**
CS D[8]	**1**	**0**	**0**	**F**

CS D[7]	**1**	**0**	**0**	**V**
CS D[6]	**1**	**0**	**0**	**H**
CS D[5]	**1**	**0**	**0**	**P3**
CS D[4]	**1**	**0**	**0**	**P2**
CS D[3]	**1**	**0**	**0**	**P1**
CS D[2]	**1**	**0**	**0**	**P0**
CS D[1]	**x**	**x**	**x**	**x**
CS D[0]	**x**	**x**	**x**	**x**

For compatibility with an 8-bit interface, CS D[1] and CS D[0] are not defined.

Decode	F	V	H	P3	P2	P1	P0
Field 1 start of active video (SAV)	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Field 1 end of active video (EAV)	**0**	**0**	**1**	**1**	**1**	**0**	**1**
Field 1 SAV (digital blanking)	**0**	**1**	**0**	**1**	**0**	**1**	**1**
Field 1 EAV (digital blanking)	**0**	**1**	**1**	**0**	**1**	**1**	**0**
Field 2 SAV	**1**	**0**	**0**	**0**	**1**	**1**	**1**
Field 2 EAV	**1**	**0**	**1**	**1**	**0**	**1**	**0**
Field 2 SAV (digital blanking)	**1**	**1**	**0**	**1**	**1**	**0**	**0**
Field 2 EAV (digital blanking)	**1**	**1**	**1**	**0**	**0**	**0**	**1**

Multi-Channel:

Condition			656 FVH Value			SAV-EAV Code						
									Fourth			
Field	V-time	H-time	F	V	H	First	Second	Third	Ch1	Ch2	Ch3	Ch4
EVEN	BLANK	EAV	1	1	1	0xFF	0x00	0x00	0xF0	0xF1	0xF2	0xF3
EVEN	BLANK	SAV	1	1	0	0xFF	0x00	0x00	0xE0	0xE1	0xE2	0xE3
EVEN	ACTIVE	EAV	1	0	1	0xFF	0x00	0x00	0xD0	0xD1	0xD2	0xD3
EVEN	ACTIVE	SAV	1	0	0	0xFF	0x00	0x00	0xC0	0xC1	0xC2	0xC3
ODD	BLANK	EAV	0	1	1	0xFF	0x00	0x00	0xB0	0xB1	0xB2	0xB3
ODD	BLANK	SAV	0	1	0	0xFF	0x00	0x00	0xA0	0xA1	0xA2	0xA3
ODD	ACTIVE	EAV	0	0	1	0xFF	0x00	0x00	0x90	0x91	0x92	0x93
ODD	ACTIVE	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x81	0x82	0x83

6.2.3.5. OFFSET / SCALE / FLIP FUNCTION

Interface will do these three functions in sequence.

6.2.3.6. OFFSET DEFINITION

Offset in horizontal and vertical can be added when receiving image. Unit is pixel.

For YUV422 format, pixel unit is a YU/YV combination.

For YUV420 format, pixel unit is a YU/YV combination in YC line, and only a Y in Y line.
For Bayer_raw format, pixel unit is a R/G/B single component.
For RGB565, pixel unit is a two bytes of RGB565 package.
For RGB888, pixel unit is a three bytes of RGB combination.

6.2.3.7. SCALE DEFINITION

All channel input image can be decimated to its quarter size if **QUART_EN** is set to 1.

When using this function, horizontal input components should be multiples of the components in a unit, and vertical lines should be multiples of the height of a unit.

Specific components and lines will be dropped except the blue ones as follows.
Component sequence in a unit may changed, but unit dropping position will not changed.

BAYER_RAW(raw_8/raw_10/raw_12):
GRGRGRGR…
BGBGBGBG…
GRGRGRGR…
BGBGBGBG…
GRGRGRGR…
BGBGBGBG…
GRGRGRGR…
BGBGBGBG…

RGB888:
RGBRGB…
RGBRGB…

RGB565:
565565…
565565…

YUV422(8bit/10bit in field mode):
YUYVYUYV…
YUYVYUYV…
YUYVYUYV…
YUYVYUYV…

YUV422(8bit/10bit in frame mode):

YUYVYUYV…→odd field

YUYVYUYV…→even field

YUYVYUYV…

YUYVYUYV…

YUV420(8bit/10bit):

YC line: **YUYVYUYV…**

Y line: **YYYY…**

YC line: **YUYVYUYV…**

Y line: **YYYY…**

6.2.3.8. FLIP DEFINITION

Both horizontal and vertical flip are supported at the same time. This function is implemented in the process of each FIFO writing data to memory, only flipping the data of separate FIFO, not changing component to FIFO distribution.

If horizontal flip is enabled, one or more pixels will be took as a unit:

For YUV format, a unit of $Y_0U_0Y_1V_1$ will parser and flip the Y component in one channel, and UV will be treated as a whole. In planar output mode, U and V will be flipped separately. In UV combined output mode, UV will be flipped as a whole. So, a sequence of $Y_1U_0Y_0V_1$ will be.

For Bayer_raw format, situation is much like. A GR/BG sequence will be changed to BG/RG. A unit of square has four pixels.

For RGB565/RGB888, one unit of two/three bytes of component will be flipped with original sequence.

6.2.4. CSI1 REGISTER LIST

Module Name	Base Address
CSI1	0x01CB3000

Register Name	Offset	Description
CSI1_EN_REG	0X000	CSI enable register
CSI1_IF_CFG_REG	0X004	CSI Interface Configuration Register

CSI1_CAP_REG	0X008	CSI Capture Register
CSI1_SYNC_CNT_REG	0X00C	CSI Synchronization Counter Register
CSI1_FIFO_THRS_REG	0X010	CSI FIFO Threshold Register
CSI1_PTN_LEN_REG	0X030	CSI Pattern Generation Length register
CSI1_PTN_ADDR_REG	0X034	CSI Pattern Generation Address register
CSI1_VER_REG	0X03C	CSI Version Register
CSI1_C0_CFG_REG	0X044	CSI Channel_0 configuration register
CSI1_C0_SCALE_REG	0X04C	CSI Channel_0 scale register
CSI1_C0_F0_BUFA_REG	0X050	CSI Channel_0 FIFO 0 output buffer-A address register
CSI1_C0_F1_BUFA_REG	0X058	CSI Channel_0 FIFO 1 output buffer-A address register
CSI1_C0_F2_BUFA_REG	0X060	CSI Channel_0 FIFO 2 output buffer-A address register
CSI1_C0_CAP_STA_REG	0X06C	CSI Channel_0 status register
CSI1_C0_INT_EN_REG	0X070	CSI Channel_0 interrupt enable register
CSI1_C0_INT_STA_REG	0X074	CSI Channel_0 interrupt status register
CSI1_C0_HSIZE_REG	0X080	CSI Channel_0 horizontal size register
CSI1_C0_VSIZE_REG	0X084	CSI Channel_0 vertical size register
CSI1_C0_BUF_LEN_REG	0X088	CSI Channel_0 line buffer length register
CSI1_C0_FLIP_SIZE_REG	0X08C	CSI Channel_0 flip size register
CSI1_C0_FRM_CLK_CNT_REG	0X090	CSI Channel_0 frame clock counter register
CSI1_C0_ACC_ITNL_CLK_CNT_REG	0X094	CSI Channel_0 accumulated and internal clock counter register
CSI1_C1_CFG_REG	0X144	CSI Channel_1 configuration register
CSI1_C1_SCALE_REG	0X14C	CSI Channel_1 scale register
CSI1_C1_F0_BUFA_REG	0X150	CSI Channel_1 FIFO 0 output buffer-A address register
CSI1_C1_F1_BUFA_REG	0X158	CSI Channel_1 FIFO 1 output buffer-A address register
CSI1_C1_F2_BUFA_REG	0X160	CSI Channel_1 FIFO 2 output buffer-A address register
CSI1_C1_CAP_STA_REG	0X16C	CSI Channel_1 status register
CSI1_C1_INT_EN_REG	0X170	CSI Channel_1 interrupt enable register
CSI1_C1_INT_STA_REG	0X174	CSI Channel_1 interrupt status register
CSI1_C1_HSIZE_REG	0X180	CSI Channel_1 horizontal size register
CSI1_C1_VSIZE_REG	0X184	CSI Channel_1 vertical size register

CSI1_C1_BUF_LEN_REG	0X188	CSI Channel_1 line buffer length register
CSI1_C1_FLIP_SIZE_REG	0X18C	CSI Channel_1 flip size register
CSI1_C1_FRM_CLK_CNT_REG	0X190	CSI Channel_1 frame clock counter register
CSI1_C1_ACC_ITNL_CLK_CNT_REG	0X194	CSI Channel_1 accumulated and internal clock counter register
CSI1_C2_CFG_REG	0X244	CSI Channel_2 configuration register
CSI1_C2_SCALE_REG	0X24C	CSI Channel_2 scale register
CSI1_C2_F0_BUFA_REG	0X250	CSI Channel_2 FIFO 0 output buffer-A address register
CSI1_C2_F1_BUFA_REG	0X258	CSI Channel_2 FIFO 1 output buffer-A address register
CSI1_C2_F2_BUFA_REG	0X260	CSI Channel_2 FIFO 2 output buffer-A address register
CSI1_C2_CAP_STA_REG	0X26C	CSI Channel_2 status register
CSI1_C2_INT_EN_REG	0X270	CSI Channel_2 interrupt enable register
CSI1_C2_INT_STA_REG	0X274	CSI Channel_2 interrupt status register
CSI1_C2_HSIZE_REG	0X280	CSI Channel_2 horizontal size register
CSI1_C2_VSIZE_REG	0X284	CSI Channel_2 vertical size register
CSI1_C2_BUF_LEN_REG	0X288	CSI Channel_2 line buffer length register
CSI1_C2_FLIP_SIZE_REG	0X28C	CSI Channel_2 flip size register
CSI1_C2_FRM_CLK_CNT_REG	0X290	CSI Channel_2 frame clock counter register
CSI1_C2_ACC_ITNL_CLK_CNT_REG	0X294	CSI Channel_2 accumulated and internal clock counter register
CSI1_C3_CFG_REG	0X344	CSI Channel_3 configuration register
CSI1_C3_SCALE_REG	0X34C	CSI Channel_3 scale register
CSI1_C3_F0_BUFA_REG	0X350	CSI Channel_3 FIFO 0 output buffer-A address register
CSI1_C3_F1_BUFA_REG	0X358	CSI Channel_3 FIFO 1 output buffer-A address register
CSI1_C3_F2_BUFA_REG	0X360	CSI Channel_3 FIFO 2 output buffer-A address register
CSI1_C3_CAP_STA_REG	0X36C	CSI Channel_3 status register
CSI1_C3_INT_EN_REG	0X370	CSI Channel_3 interrupt enable register
CSI1_C3_INT_STA_REG	0X374	CSI Channel_3 interrupt status register
CSI1_C3_HSIZE_REG	0X380	CSI Channel_3 horizontal size register
CSI1_C3_VSIZE_REG	0X384	CSI Channel_3 vertical size register
CSI1_C3_BUF_LEN_REG	0X388	CSI Channel_3 line buffer length register

CSI1_C3_FLIP_SIZE_REG	0X38C	CSI Channel_3 flip size register
CSI1_C3_FRM_CLK_CNT_REG	0X390	CSI Channel_3 frame clock counter register
CSI1_C3_ACC_ITNL_CLK_CNT_REG	0X394	CSI Channel_3 accumulated and internal clock counter register

6.2.5. CSI1 REGISTER DESCRIPTION

6.2.5.1. CSI ENABLE REGISTER

Offset Address: 0x0000			Register Name: CSI1_EN_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	**VER_EN** CSI Version Register Read Enable: 0: Disable 1: Enable
29:24	/	/	/
23:16	R/W	0x00	PTN_CYCLE Pattern generating cycle counter. The pattern in dram will be generated in cycles of PTN_CYCLE+1.
15:5	/	/	/
4	R/W	0x0	PTN_START CSI Pattern Generating Start 0: Finish other: Start Software write this bit to“1” to start pattern generating from DRAM. When finished, the hardware will clear this bit to“0”automatically. Generating cycles depends on PTN_CYCLE.
3	R/W	0	CLK_CNT_SPL Sampling time for clk counter per frame 0: Sampling clock counter every frame done 1: Sampling clock counter every vsync
2	R/W	0	CLK_CNT clk count per frame
1	R/W	0	PTN_GEN_EN Pattern Generation Enable
0	R/W	0	CSI_EN

			Enable 0: Reset and disable the CSI module 1: Enable the CSI module

6.2.5.2. CSI INTERFACE CONFIGURATION REGISTER

Offset Address: 0x0004			Register Name: CSI1_IF_CFG_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	/	/	/
23	R/W	0	CSI_SRC_SWAP 0: normal 1: swap src Normally, Csi0/1 parser the h/v and data to Csi0/1 interface; Enable this bit will swap the signals after Csi1/0 parser to Csi0/1 interface.
22	/	/	/
21	R/W	0	SRC_TYPE Source type 0: Progressed 1: Interlaced
20	R/W	0	FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames
19	R/W	0	FIELD For YUV HV timing, Field polarity 0: negative(field=0 indicate odd, field=1 indicate even) 1: positive(field=1 indicate odd, field=0 indicate even) For BT656 timing, Field sequence 0: Normal sequence (field 0 first) 1: Inverse sequence (field 1 first)
18	R/W	1	VREF_POL Vref polarity 0: negative 1: positive This register is not apply to CCIR656 interface.
17	R/W	0	HERF_POL Href polarity

			0: negative 1: positive This register is not apply to CCIR656 interface.
16	R/W	1	CLK_POL Data clock type 0: active in falling edge 1: active in rising edge
15:12	/	/	/
11:10	R/W	0	IF_BUS_SEQ
9:8	R/W	0	IF_DATA_WIDTH 00: 8 bit data bus 01: 10 bit data bus 10: 12 bit data bus Others: Reserved
7	R/W	0	MIPI_IF MIPI Interface Enable: 0: CSI 1: MIPI
6:5	/	/	/
4:0	R/W	0	CSI_IF YUV: 00000: YUYV422 Interleaved or RAW (All data in one data bus) 00001: / 00010: / 00011: / CCIR656: 00100: YUYV422 Interleaved or RAW (All data in one data bus) 00101: / 00110: / 00111: / 01100: CCIR656 2 channels (All data interleaved in one data bus) 01101: CCIR656 4 channels (All data interleaved in one data bus) Others: Reserved

6.2.5.3. CSI CAPTURE REGISTER

Offset: 0x0008			Register Name: CSI1_CAP_REG
Bit	Read/ Write	Default/Hex	Description
31:30	/	/	/
29:26	R/W	0x00	CH3_CAP_MASK Vsync number masked before capture.
25	R/W	0	CH3_VCAP_ON Video capture control: Capture the video image data stream on channel 3. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
24	R/W	0	CH3_SCAP_ON Still capture control: Capture a single still image frame on channel 3. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self clearing and always reads as a 0.
23:22	/	/	/
21:18	R/W	0x00	CH2_CAP_MASK Vsync number masked before capture.
17	R/W	0	CH2_VCAP_ON Video capture control: Capture the video image data stream on channel 2. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
16	R/W	0	CH2_SCAP_ON Still capture control: Capture a single still image frame on channel 2. 0: Disable still capture.

			1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self clearing and always reads as a 0.
15:14	/	/	/
13:10	R/W	0x00	CH1_CAP_MASK Vsync number masked before capture.
09	R/W	0	CH1_VCAP_ON Video capture control: Capture the video image data stream on channel 1. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
08	R/W	0	CH1_SCAP_ON Still capture control: Capture a single still image frame on channel 1. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self clearing and always reads as a 0.
07:06	/	/	/
05:02	R/W	0x00	CH0_CAP_MASK Vsync number masked before capture.
01	R/W	0	CH0_VCAP_ON Video capture control: Capture the video image data stream on channel 0. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
00	R/W	0	CH0_SCAP_ON Still capture control: Capture a single still image frame on channel 0. 0: Disable still capture.

			1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self clearing and always reads as a 0.

6.2.5.4. CSI SYNCHRONIZATION COUNTER REGISTER

Offset Address: 0x000c			Register Name: CSI1_SYNC_CNT_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:00	R	0	SYNC_CNT The counter value between vsync of Csi0 channel 0 and vsync of Csi1 channel 0 , using 24MHz.

6.2.5.5. CSI FIFO THRESHOLD REGISTER

Offset Address: 0x0010			Register Name: CSI1_FIFO_THRS_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0f	PTN_GEN_DLY Clocks delayed before pattern generating start.
15:12	/	/	/
11:00	R/W	0x400	FIFO_THRS When CSI1 FIFO occupied memory exceeds the threshold, dram frequency can not change.

6.2.5.6. CSI PATTERN GENERATION LENGTH REGISTER

Offset: 0x0030			Register Name: CSI1_PTN_LEN_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	PTN_LEN The pattern length in byte when generating pattern.

6.2.5.7. CSI PATTERN GENERATION ADDRESS REGISTER

Offset: 0x0034			Register Name: CSI1_PTN_ADDR_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**

31:0	R/W	0x0	PTN_ADDR The pattern DRAM address when generating pattern.

6.2.5.8. CSI VERSION REGISTER

Offset: 0x003C			Register Name: CSI1_VER_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:0	R/W	/	VER Version of hardware circuit. Only can be read when version register read enable is on.

6.2.5.9. CSI CHANNEL_0 CONFIGURATION REGISTER

Offset Address: 0X0044			Register Name: CSI1_C0_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00~0xff
23:20	R/W	3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved
19:16	R/W	0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: field-raw-8 0001: field-raw-10 0010: field-raw-12 0011: reserved 0100: field-rgb565 0101: field-rgb888 0110: field-prgb888 0111: field-uv-combined 1000: frame-raw-8

			1001: frame-raw-10 1010: frame-raw-12 1011: reserved 1100: frame-rgb565 1101: frame-rgb888 1110: frame-prgb888 1111: frame-uv-combined When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: frame planar YCbCr 422 UV combined 1000: field MB YCbCr 422 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: frame MB YCbCr 422 1100: field planar YCbCr 422 10bit UV combined 1101: field planar YCbCr 420 10bit UV combined 1110: Reserved 1111: Reserved When the input format is set YUV420 0000: Reserved 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: Reserved 0100: Reserved 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: Reserved 1000: Reserved 1001: field MB YCbCr 420 1010: frame MB YCbCr 420

			1011: Reserved 1100: Reserved 1101: field planar YCbCr 420 10bit UV combined 1110: Reserved 1111: Reserved Others: reserved
15:14	/	/	/
13	R/W	0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0:Disable 1:Enable
12	R/W	0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0:Disable 1:Enable
11:10	R/W	0	FIELD_SEL Field selection. 00: capturing with field 1. 01: capturing with field 2. 10: capturing with either field. 11: reserved
09:08	R/W	2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU

07:00	/	/	/

6.2.5.10. CSI CHANNEL_0 SCALE REGISTER

Offset Address: 0X004C			Register Name: CSI1_C0_SCALE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:01	/	/	/
00	R/W	0	QUART_EN When this bit is set to 1, input image will be decimated to quarter size. All input format are supported.

6.2.5.11. CSI CHANNEL_0 FIFO 0 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0050			Register Name: CSI1_C0_F0_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C0F0_BUFA FIFO 0 output buffer-A address

6.2.5.12. CSI CHANNEL_0 FIFO 1 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0058			Register Name: CSI1_C0_F1_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C0F1_BUFA FIFO 1 output buffer-A address

6.2.5.13. CSI CHANNEL_0 FIFO 2 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0060			Register Name: CSI1_C0_F2_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C0F2_BUFA FIFO 2 output buffer-A address

6.2.5.14. CSI CHANNEL_0 STATUS REGISTER

Offset Address: 0X006C			Register Name: CSI1_C0_CAP_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:03	/	/	/
02	R	0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
01	R	0	VCAP_STA

			Video capture in progress Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabling video capture. When software disables video capture, it clears itself after the last pixel of the current frame is captured.
00	R	0	SCAP_STA Still capture in progress Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabling still frame capture. It clears itself after the last pixel of the first frame is captured. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means filed end.

6.2.5.15. CSI CHANNEL_0 INTERRUPT ENABLE REGISTER

Offset Address: 0X0070			**Register Name: CSI1_C0_INT_EN_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:08	/	/	/
07	R/W	0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
06	R/W	0	HB_OF_INT_EN Hblank FIFO overflow The bit is set when 3 FIFOs still overflow after the hblank.
05	R/W	0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
04	R/W	0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
03	R/W	0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.
02	R/W	0	FIFO0_OF_INT_EN

			FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
01	R/W	0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is written to buffer as long as video capture remains enabled.
00	R/W	0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been written to buffer. For video capture, the bit is set when the last frame has been written to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

6.2.5.16. CSI CHANNEL_0 INTERRUPT STATUS REGISTER

Offset Address: 0X0074			**Register Name: CSI1_C0_INT_STA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:08	/	/	/
07	R/W	0	VS_PD vsync flag
06	R/W	0	HB_OF_PD Hblank FIFO overflow
05	R/W	0	MUL_ ERR_PD Multi-channel writing error
04	R/W	0	FIFO2_OF_PD FIFO 2 overflow
03	R/W	0	FIFO1_OF_PD FIFO 1 overflow
02	R/W	0	FIFO0_OF_PD FIFO 0 overflow
01	R/W	0	FD_PD Frame done

00	R/W	0	CD_PD Capture done

6.2.5.17. CSI CHANNEL_0 HORIZONTAL SIZE REGISTER

Offset Address: 0X0080			Register Name: CSI1_C0_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	500	HOR_LEN Horizontal pixel clock length. Valid pixel clocks of a line.
15:13	/	/	/
12:00	R/W	0	HOR_START Horizontal pixel unit start. Pixel is valid from this unit.

6.2.5.18. CSI CHANNEL_0 VERTICAL SIZE REGISTER

Offset Address: 0X0084			Register Name: CSI1_C0_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	1E0	VER_LEN Vertical line length. Valid line number of a frame.
15:13	/	/	/
12:00	R/W	0	VER_START Vertical line start. data is valid from this line.

6.2.5.19. CSI CHANNEL_0 BUFFER LENGTH REGISTER

Offset Address: 0X0088			Register Name: CSI1_C0_BUF_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	140	BUF_LEN_C Buffer length of chroma C in a line. Unit is byte.
15:13	/	/	/
12:00	R/W	280	BUF_LEN Buffer length of luminance Y in a line. Unit is byte.

6.2.5.20. CSI CHANNEL_0 FLIP SIZE REGISTER

Offset Address: 0X008C			Register Name: CSI1_C0_FLIP_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:29	/	/	/
28:16	R/W	1E0	VER_LEN Vertical line number when in vflip mode.
15:13	/	/	/
12:00	R/W	280	VALID_LEN Valid components of a line when in flip mode.

6.2.5.21. CSI CHANNEL_0 FRAME CLOCK COUNTER REGISTER

Offset Address: 0x0090			Register Name: CSI1_C0_FRM_CLK_CNT_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:00	R	0	FRM_CLK_CNT Counter value between every frame. For instant hardware frame rate statics. The internal counter is added by one every 24MHz clock cycle. When frame done or vsync comes, the internal counter value is sampled to FRM_CLK_CNT, and cleared to 0.

6.2.5.22. CSI CHANNEL_0 ACCUMULATED AND INTERNAL CLOCK COUNTER REGISTER

Offset Address: 0x0094			Register Name: CSI1_C0_ACC_ITNL_CLK_CNT_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	R/W	0	ACC_CLK_CNT The accumulated value of FRM_CLK_CNT for software frame rate statics. Every interrupt of frame done, the software check this accumulated value and clear it to 0. If the ACC_CLK_CNT is larger than 1, the software has lost frame. When frame done or vsync comes, ACC_CLK_CNT = ACC_CLK_CNT + 1, and cleared to 0 when writing 0 to this register.
23:00	R	0	ITNL_CLK_CNT The instant value of internal frame clock counter. When frame done interrupt comes, the software can query this counter for judging whether it is the time for updating the double buffer address

			registers.

6.2.5.23. CSI CHANNEL_1 CONFIGURATION REGISTER

Offset Address: 0X0144			Register Name: CSI1_C1_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00~0xff
23:20	R/W	3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved
19:16	R/W	0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: field-raw-8 0001: field-raw-10 0010: field-raw-12 0011: reserved 0100: field-rgb565 0101: field-rgb888 0110: field-prgb888 0111: field-uv-combined 1000: frame-raw-8 1001: frame-raw-10 1010: frame-raw-12 1011: reserved 1100: frame-rgb565 1101: frame-rgb888 1110: frame-prgb888 1111: frame-uv-combined When the input format is set YUV422 0000: field planar YCbCr 422

			0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: frame planar YCbCr 422 UV combined 1000: field MB YCbCr 422 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: frame MB YCbCr 422 1100: field planar YCbCr 422 10bit UV combined 1101: field planar YCbCr 420 10bit UV combined 1110: Reserved 1111: Reserved When the input format is set YUV420 0000: Reserved 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: Reserved 0100: Reserved 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: Reserved 1000: Reserved 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: Reserved 1100: Reserved 1101: field planar YCbCr 420 10bit UV combined 1110: Reserved 1111: Reserved Others: reserved
15:14	/	/	/
13	R/W	0	VFLIP_EN Vertical flip enable

			When enabled, the received data will be arranged in vertical flip. 0:Disable 1:Enable
12	R/W	0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0:Disable 1:Enable
11:10	R/W	0	FIELD_SEL Field selection. 00: capturing with field 1. 01: capturing with field 2. 10: capturing with either field. 11: reserved
09:08	R/W	2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU
07:00	/	/	/

6.2.5.24. CSI CHANNEL_1 SCALE REGISTER

Offset Address: 0X014C			**Register Name: CSI1_C1_SCALE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:01	/	/	/
00	R/W	0	QUART_EN When this bit is set to 1, input image will be decimated to quarter size. All input format are supported.

6.2.5.25. CSI CHANNEL_1 FIFO 0 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0150			Register Name: CSI1_C1_F0_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C1F0_BUFA FIFO 0 output buffer-A address

6.2.5.26. CSI CHANNEL_1 FIFO 1 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0158			Register Name: CSI1_C1_F1_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C1F1_BUFA FIFO 1 output buffer-A address

6.2.5.27. CSI CHANNEL_1 FIFO 2 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0160			Register Name: CSI1_C1_F2_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C1F2_BUFA FIFO 2 output buffer-A address

6.2.5.28. CSI CHANNEL_1 STATUS REGISTER

Offset Address: 0X016C			Register Name: CSI1_C1_CAP_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:03	/	/	/
02	R	0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
01	R	0	VCAP_STA Video capture in progress Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabling video capture. When software disables video capture, it clears itself after the last pixel of the current frame is captured.
00	R	0	SCAP_STA Still capture in progress Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabling still frame capture. It clears itself after the last pixel of the first frame is

			captured. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means filed end.

6.2.5.29. CSI CHANNEL_1 INTERRUPT ENABLE REGISTER

Offset Address: 0X0170			**Register Name: CSI1_C1_INT_EN_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:08	/	/	/
07	R/W	0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
06	R/W	0	HB_OF_INT_EN Hblank FIFO overflow The bit is set when 3 FIFOs still overflow after the hblank.
05	R/W	0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
04	R/W	0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
03	R/W	0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.
02	R/W	0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
01	R/W	0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is written to buffer as long as video capture remains enabled.
00	R/W	0	CD_INT_EN Capture done

			Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been written to buffer. For video capture, the bit is set when the last frame has been written to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

6.2.5.30. CSI CHANNEL_1 INTERRUPT STATUS REGISTER

Offset Address: 0X0174			**Register Name: CSI1_C1_INT_STA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:08	/	/	/
07	R/W	0	VS_PD vsync flag
06	R/W	0	HB_OF_PD Hblank FIFO overflow
05	R/W	0	MUL_ ERR_PD Multi-channel writing error
04	R/W	0	FIFO2_OF_PD FIFO 2 overflow
03	R/W	0	FIFO1_OF_PD FIFO 1 overflow
02	R/W	0	FIFO0_OF_PD FIFO 0 overflow
01	R/W	0	FD_PD Frame done
00	R/W	0	CD_PD Capture done

6.2.5.31. CSI CHANNEL_1 HORIZONTAL SIZE REGISTER

Offset Address: 0X0180	**Register Name: CSI1_C1_HSIZE_REG**

Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	500	HOR_LEN Horizontal pixel clock length. Valid pixel clocks of a line.
15:13	/	/	/
12:00	R/W	0	HOR_START Horizontal pixel clock start.Pixel data is valid from this clock.

6.2.5.32. CSI CHANNEL_1 VERTICAL SIZE REGISTER

Offset Address: 0X0184			Register Name: CSI1_C1_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	1E0	VER_LEN Vertical line length. Valid line number of a frame.
15:13	/	/	/
12:00	R/W	0	VER_START Vertical line start. data is valid from this line.

6.2.5.33. CSI CHANNEL_1 BUFFER LENGTH REGISTER

Offset Address: 0X0188			Register Name: CSI1_C1_BUF_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	140	BUF_LEN_C Buffer length of chroma C in a line. Unit is byte.
15:13	/	/	/
12:00	R/W	280	BUF_LEN Buffer length of luminance Y in a line. Unit is byte.

6.2.5.34. CSI CHANNEL_1 FLIP SIZE REGISTER

Offset Address: 0X018C			Register Name: CSI1_C1_FLIP_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	1E0	VER_LEN Vertical line number when in vflip mode.
15:13	/	/	/
12:00	R/W	280	VALID_LEN

			Valid components of a line when in flip mode.

6.2.5.35. CSI CHANNEL_1 FRAME CLOCK COUNTER REGISTER

Offset Address: 0x0190			Register Name: CSI1_C1_FRM_CLK_CNT_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:00	R	0	FRM_CLK_CNT Counter value between every frame. For instant hardware frame rate statics. The internal counter is added by one every 24MHz clock cycle. When frame done or vsync comes, the internal counter value is sampled to FRM_CLK_CNT, and cleared to 0. Then the FRM_CLK_CNT is added to ACC_CLK_CNT.

6.2.5.36. CSI CHANNEL_1 ACCUMULATED AND INTERNAL CLOCK COUNTER REGISTER

Offset Address: 0x0194			Register Name: CSI1_C1_ACC_ITNL_CLK_CNT_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	R/W	0	ACC_CLK_CNT The accumulated value of FRM_CLK_CNT for software frame rate statics. Every interrupt of frame done, the software check this accumulated value and clear it to 0. If the ACC_CLK_CNT is larger than 1, the software has lost frame. When frame done or vsync comes, ACC_CLK_CNT = ACC_CLK_CNT + 1, and cleared to 0 when writing 0 to this register.
23:00	R	0	ITNL_CLK_CNT The instant value of internal frame clock counter. When frame done interrupt comes, the software can query this counter for judging whether it is the time for updating the double buffer address registers.

6.2.5.37. CSI CHANNEL_2 CONFIGURATION REGISTER

Offset Address: 0X0244	Register Name: CSI1_C2_CFG_REG

Bit	Read/Write	Default/Hex	Description
31:24	R/W	0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00~0xff
23:20	R/W	3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved
19:16	R/W	0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: field-raw-8 0001: field-raw-10 0010: field-raw-12 0011: reserved 0100: field-rgb565 0101: field-rgb888 0110: field-prgb888 0111: field-uv-combined 1000: frame-raw-8 1001: frame-raw-10 1010: frame-raw-12 1011: reserved 1100: frame-rgb565 1101: frame-rgb888 1110: frame-prgb888 1111: frame-uv-combined When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined

			0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: frame planar YCbCr 422 UV combined 1000: field MB YCbCr 422 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: frame MB YCbCr 422 1100: field planar YCbCr 422 10bit UV combined 1101: field planar YCbCr 420 10bit UV combined 1110: Reserved 1111: Reserved When the input format is set YUV420 0000: Reserved 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: Reserved 0100: Reserved 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: Reserved 1000: Reserved 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: Reserved 1100: Reserved 1101: field planar YCbCr 420 10bit UV combined 1110: Reserved 1111: Reserved Others: reserved
15:14	/	/	/
13	R/W	0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0:Disable 1:Enable
12	R/W	0	HFLIP_EN

			Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0:Disable 1:Enable
11:10	R/W	0	FIELD_SEL Field selection. 00: capturing with field 1. 01: capturing with field 2. 10: capturing with either field. 11: reserved
09:08	R/W	2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU
07:00	/	/	/

6.2.5.38. CSI CHANNEL_2 SCALE REGISTER

Offset Address: 0X024C			Register Name: CSI1_C2_SCALE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:01	/	/	/
00	R/W	0	QUART_EN When this bit is set to 1, input image will be decimated to quarter size. All input format are supported.

6.2.5.39. CSI CHANNEL_2 FIFO 0 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0250			Register Name: CSI1_C2_F0_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:00	R/W	0	C2F0_BUFA FIFO 0 output buffer-A address

6.2.5.40. CSI CHANNEL_2 FIFO 1 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0258			**Register Name: CSI1_C2_F1_BUFA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C2F1_BUFA FIFO 1 output buffer-A address

6.2.5.41. CSI CHANNEL_2 FIFO 2 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0260			**Register Name: CSI1_C2_F2_BUFA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C2F2_BUFA FIFO 2 output buffer-A address

6.2.5.42. CSI CHANNEL_2 STATUS REGISTER

Offset Address: 0X026C			**Register Name: CSI1_C2_CAP_STA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:03	/	/	/
02	R	0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
01	R	0	VCAP_STA Video capture in progress Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabling video capture. When software disables video capture, it clears itself after the last pixel of the current frame is captured.
00	R	0	SCAP_STA Still capture in progress Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabling still frame capture. It clears itself after the last pixel of the first frame is captured. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means filed end.

6.2.5.43. CSI CHANNEL_2 INTERRUPT ENABLE REGISTER

Offset Address: 0X0270			Register Name: CSI1_C2_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:08	/	/	/
07	R/W	0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
06	R/W	0	HB_OF_INT_EN Hblank FIFO overflow The bit is set when 3 FIFOs still overflow after the hblank.
05	R/W	0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
04	R/W	0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
03	R/W	0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.
02	R/W	0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
01	R/W	0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is written to buffer as long as video capture remains enabled.
00	R/W	0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been written to buffer. For video capture, the bit is set when the last frame has been

			written to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

6.2.5.44. CSI CHANNEL_2 INTERRUPT STATUS REGISTER

Offset Address: 0X0274			Register Name: CSI1_C2_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:08	/	/	/
07	R/W	0	VS_PD vsync flag
06	R/W	0	HB_OF_PD Hblank FIFO overflow
05	R/W	0	MUL_ ERR_PD Multi-channel writing error
04	R/W	0	FIFO2_OF_PD FIFO 2 overflow
03	R/W	0	FIFO1_OF_PD FIFO 1 overflow
02	R/W	0	FIFO0_OF_PD FIFO 0 overflow
01	R/W	0	FD_PD Frame done
00	R/W	0	CD_PD Capture done

6.2.5.45. CSI CHANNEL_2 HORIZONTAL SIZE REGISTER

Offset Address: 0X0280			Register Name: CSI1_C2_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	500	HOR_LEN Horizontal pixel clock length. Valid pixel clocks of a line.
15:13	/	/	/
12:00	R/W	0	HOR_START Horizontal pixel clock start. Pixel data is valid from this clock.

6.2.5.46. CSI CHANNEL_2 VERTICAL SIZE REGISTER

Offset Address: 0X0284			Register Name: CSI1_C2_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	1E0	VER_LEN Vertical line length. Valid line number of a frame.
15:13	/	/	/
12:00	R/W	0	VER_START Vertical line start. data is valid from this line.

6.2.5.47. CSI CHANNEL_2 BUFFER LENGTH REGISTER

Offset Address: 0X0288			Register Name: CSI1_C2_BUF_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	140	BUF_LEN_C Buffer length of chroma C in a line. Unit is byte.
15:13	/	/	/
12:00	R/W	280	BUF_LEN Buffer length of luminance Y in a line. Unit is byte.

6.2.5.48. CSI CHANNEL_2 FLIP SIZE REGISTER

Offset Address: 0X028C			Register Name: CSI1_C2_FLIP_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	1E0	VER_LEN Vertical line number when in vflip mode.
15:13	/	/	/
12:00	R/W	280	VALID_LEN Valid components of a line when in flip mode.

6.2.5.49. CSI CHANNEL_2 FRAME CLOCK COUNTER REGISTER

Offset Address: 0x0290			Register Name: CSI1_C2_FRM_CLK_CNT_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:00	R	0	FRM_CLK_CNT Counter value between every frame. For instant hardware frame rate

			statics. The internal counter is added by one every 24MHz clock cycle. When frame done or vsync comes, the internal counter value is sampled to FRM_CLK_CNT, and cleared to 0. Then the FRM_CLK_CNT is added to ACC_CLK_CNT.

6.2.5.50. CSI CHANNEL_2 ACCUMULATED AND INTERNAL CLOCK COUNTER REGISTER

Offset Address: 0x0294			Register Name: CSI1_C2_ACC_ITNL_CLK_CNT_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	R/W	0	ACC_CLK_CNT The accumulated value of FRM_CLK_CNT for software frame rate statics. Every interrupt of frame done, the software check this accumulated value and clear it to 0. If the ACC_CLK_CNT is larger than 1, the software has lost frame. When frame done or vsync comes, ACC_CLK_CNT = ACC_CLK_CNT + 1, and cleared to 0 when writing 0 to this register.
23:00	R	0	ITNL_CLK_CNT The instant value of internal frame clock counter. When frame done interrupt comes, the software can query this counter for judging whether it is the time for updating the double buffer address registers.

6.2.5.51. CSI CHANNEL_3 CONFIGURATION REGISTER

Offset Address: 0X0344			Register Name: CSI1_C3_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00~0xff
23:20	R/W	3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved

			0011: YUV422 0100: YUV420 Others: reserved
19:16	R/W	0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: field-raw-8 0001: field-raw-10 0010: field-raw-12 0011: reserved 0100: field-rgb565 0101: field-rgb888 0110: field-prgb888 0111: field-uv-combined 1000: frame-raw-8 1001: frame-raw-10 1010: frame-raw-12 1011: reserved 1100: frame-rgb565 1101: frame-rgb888 1110: frame-prgb888 1111: frame-uv-combined When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: frame planar YCbCr 422 UV combined 1000: field MB YCbCr 422 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: frame MB YCbCr 422 1100: field planar YCbCr 422 10bit UV combined 1101: field planar YCbCr 420 10bit UV combined

			1110: Reserved 1111: Reserved When the input format is set YUV420 0000: Reserved 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: Reserved 0100: Reserved 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: Reserved 1000: Reserved 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: Reserved 1100: Reserved 1101: field planar YCbCr 420 10bit UV combined 1110: Reserved 1111: Reserved Others: reserved
15:14	/	/	/
13	R/W	0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0:Disable 1:Enable
12	R/W	0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0:Disable 1:Enable
11:10	R/W	0	FIELD_SEL Field selection. 00: capturing with field 1. 01: capturing with field 2.

			10: capturing with either field. 11: reserved
09:08	R/W	2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU
07:00	/	/	/

6.2.5.52. CSI CHANNEL_3 SCALE REGISTER

Offset Address: 0X034C			**Register Name: CSI1_C3_SCALE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:01	/	/	/
00	R/W	0	QUART_EN When this bit is set to 1, input image will be decimated to quarter size. All input format are supported.

6.2.5.53. CSI CHANNEL_3 FIFO 0 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0350			**Register Name: CSI1_C3_F0_BUFA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C3F0_BUFA FIFO 0 output buffer-A address

6.2.5.54. CSI CHANNEL_3 FIFO 1 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0358			**Register Name: CSI1_C3_F1_BUFA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C3F1_BUFA FIFO 1 output buffer-A address

6.2.5.55. CSI CHANNEL_3 FIFO 2 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0360			Register Name: CSI1_C3_F2_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0	C3F2_BUFA FIFO 2 output buffer-A address

6.2.5.56. CSI CHANNEL_3 STATUS REGISTER

Offset Address: 0X036C			Register Name: CSI1_C3_CAP_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:03	/	/	/
02	R	0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
01	R	0	VCAP_STA Video capture in progress Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabling video capture. When software disables video capture, it clears itself after the last pixel of the current frame is captured.
00	R	0	SCAP_STA Still capture in progress Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabling still frame capture. It clears itself after the last pixel of the first frame is captured. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means filed end.

6.2.5.57. CSI CHANNEL_3 INTERRUPT ENABLE REGISTER

Offset Address: 0X0370			Register Name: CSI1_C3_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:08	/	/	/
07	R/W	0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer

			address for the coming frame. So after this irq come, change the buffer address could only effect next frame
06	R/W	0	HB_OF_INT_EN Hblank FIFO overflow The bit is set when 3 FIFOs still overflow after the hblank.
05	R/W	0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
04	R/W	0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
03	R/W	0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.
02	R/W	0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
01	R/W	0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is written to buffer as long as video capture remains enabled.
00	R/W	0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been written to buffer. For video capture, the bit is set when the last frame has been written to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

6.2.5.58. CSI CHANNEL_3 INTERRUPT STATUS REGISTER

Offset Address: 0X0374			**Register Name: CSI1_C3_INT_STA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**

31:08	/	/	/
07	R/W	0	VS_PD vsync flag
06	R/W	0	HB_OF_PD Hblank FIFO overflow
05	R/W	0	MUL_ ERR_PD Multi-channel writing error
04	R/W	0	FIFO2_OF_PD FIFO 2 overflow
03	R/W	0	FIFO1_OF_PD FIFO 1 overflow
02	R/W	0	FIFO0_OF_PD FIFO 0 overflow
01	R/W	0	FD_PD Frame done
00	R/W	0	CD_PD Capture done

6.2.5.59. CSI CHANNEL_3 HORIZONTAL SIZE REGISTER

Offset Address: 0X0380			**Register Name: CSI1_C3_HSIZE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	500	HOR_LEN Horizontal pixel clock length. Valid pixel clocks of a line.
15:13	/	/	/
12:00	R/W	0	HOR_START Horizontal pixel clock start.Pixel data is valid from this clock.

6.2.5.60. CSI CHANNEL_3 VERTICAL SIZE REGISTER

Offset Address: 0X0384			**Register Name: CSI1_C3_VSIZE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	1E0	VER_LEN Vertical line length. Valid line number of a frame.
15:13	/	/	/
12:00	R/W	0	VER_START Vertical line start. data is valid from this line.

6.2.5.61. CSI CHANNEL_3 BUFFER LENGTH REGISTER

Offset Address: 0X0388			Register Name: CSI1_C3_BUF_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	140	BUF_LEN_C Buffer length of chroma C in a line. Unit is byte.
15:13	/	/	/
12:00	R/W	280	BUF_LEN Buffer length of luminance Y in a line. Unit is byte.

6.2.5.62. CSI CHANNEL_3 FLIP SIZE REGISTER

Offset Address: 0X038C			Register Name: CSI1_C3_FLIP_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	1E0	VER_LEN Vertical line number when in vflip mode.
15:13	/	/	/
12:00	R/W	280	VALID_LEN Valid components of a line when in flip mode.

6.2.5.63. CSI CHANNEL_3 FRAME CLOCK COUNTER REGISTER

Offset Address: 0x0390			Register Name: CSI1_C3_FRM_CLK_CNT_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:00	R	0	FRM_CLK_CNT Counter value between every frame. For instant hardware frame rate statics. The internal counter is added by one every 24MHz clock cycle. When frame done or vsync comes, the internal counter value is sampled to FRM_CLK_CNT, and cleared to 0. Then the FRM_CLK_CNT is added to ACC_CLK_CNT.

6.2.5.64. CSI CHANNEL_3 ACCUMULATED AND INTERNAL CLOCK COUNTER REGISTER

Offset Address: 0x0394			Register Name: CSI1_C3_ACC_ITNL_CLK_CNT_REG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	R/W	0	ACC_CLK_CNT The accumulated value of FRM_CLK_CNT for software frame rate statics. Every interrupt of frame done, the software check this accumulated value and clear it to 0. If the ACC_CLK_CNT is larger than 1, the software has lost frame. When frame done or vsync comes, ACC_CLK_CNT = ACC_CLK_CNT + 1, and cleared to 0 when writing 0 to this register.
23:00	R	0	ITNL_CLK_CNT The instant value of internal frame clock counter. When frame done interrupt comes, the software can query this counter for judging whether it is the time for updating the double buffer address registers.

6.3. MIPI CSI

6.3.1. OVERVIEW

The MIPI CSI module features:

- Comply with MIPI SPEC for D-PHY v0.90.00
- Comply with MIPI SPEC for Camera Serial Interface 2(CSI-2) v1.01.00
- 1/2/3/4 Data Lanes Configuration
- Up to 1Gbps per Lane in HS Transmission at 1 or 2 data lane mode
- Up to 600Mbps per lane in HS Transmission at 4 data lane mode
- SupportYUV422-8bit/10bit,YUV420-8bit/10bit,RAW-8,RAW-10,RAW-12,RGB888,RGB565 formats
- Support up to 12M CMOS-sensor
- Up to 720p@30fps or 1080p@15fps with one data Lane
- Up to 1080p@30fps or 5M@15fps with two data Lanes
- Up to 1080p@60fps or 5M@30fps with four data Lanes
- Maximum to 4 data type interleaving in one channel
- Maximum to 4 virtual channel interleaving with one data type

6.3.2. MIPI CSI BLOCK DIAGRAM

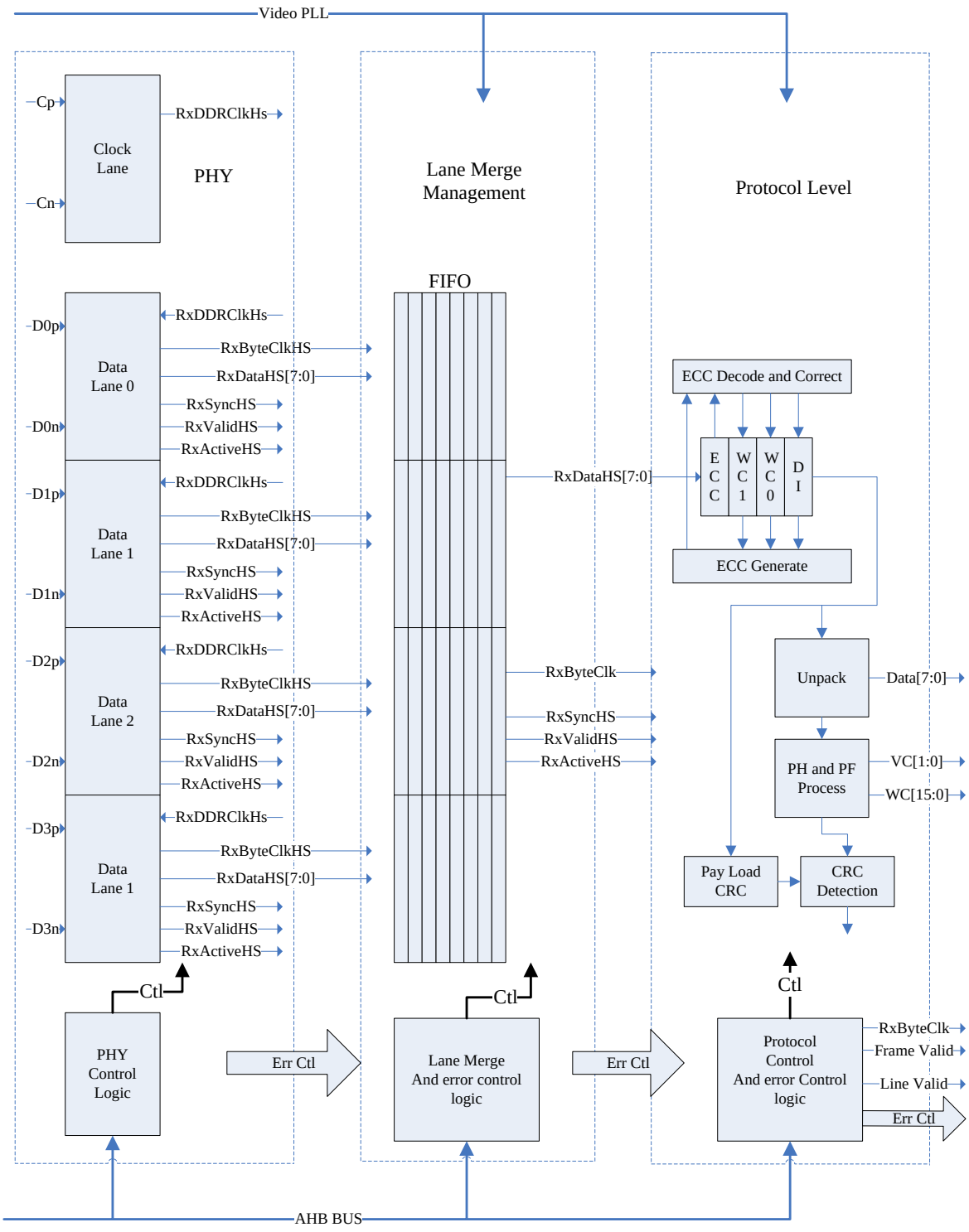


Figure 6-3 MIPI CSI Block Diagram

6.3.3. MIPI CSI DESCRIPTION

6.3.3.1. SUPPORTED DATA TYPE

Data Type	Description	Packet Type	Note
0x00	Frame Start Code	S	
0x01	Frame End Code	S	
0x02	Line Start Code	S	
0x03	Line End Code	S	
0x08~0x0F	Generic Short Packet Data	S	Information for the opening/closing of shutters, triggering of flashes, etc within the data stream.
0x10	Null	L	
0x11	Blanking Data	L	
0x12	Embedded Data	L	
0x18	YUV 420 8-bit	L	
0x19	YUV 420 10-bit	L	
0x1C	YUV 420 8-bit CSP	L	
0x1D	YUV 420 10-bit CSP	L	
0x1E	YUV 422 8-bit	L	
0x1F	YUV 422 10-bit	L	
0x22	RGB565	L	
0x24	RGB888	L	
0x2A	RAW8	L	
0x2B	RAW10	L	
0x2C	RAW12	L	
0x30~0x37	User Defined 8-bit Data	L	

6.3.3.2. DATA INTERLEAVING

The MIPI CSI-2 RX can interleave the data through Virtual Channel ID or Data Type ID. It supports up to 4 virtual channels with one data type or 4 data types when using only one virtual channel. The data of 4 channels will be parsed to different buffer via CSI0 interface. The RX should match the virtual channel id and data type through **MIPI_CSI2_VCDT_RX** register.

6.3.3.3. EMBEDDED DATA

The Embedded Data can be received when **MIPI_CSI2_CFG.EMBD_DAT_EN** is set to 1. At this time, the embedded data is received as payload data and will be parsed to the buffer.

The embedded data should be unpacked using the payload unpacking principle in the same frame.

6.3.3.4. GENERATING INTERRUPT

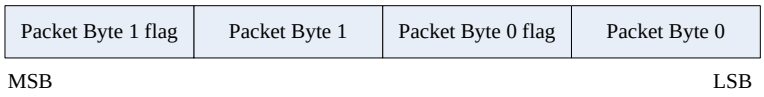
The MIPI CSI-2 RX can generate interrupt pending when a new packet header has been received. This is useful when the Generic Short Packet Data(0x08~0x0F) has been received, for example. Since it can not be treated as payload data, it should trigger an interrupt and the software will read the **Current Packet Header** register to know the Date Type and the word counter field.

6.3.3.5. PACKET GENERATING FORMAT

The packet generated from DRAM is arranged as followed:

Packet byte flag is 0 indicates that the packet byte is the valid content.

Packet byte flag is 1 indicates that the packet byte is the blanking.



6.3.4. MIPI CSI REGISTER LIST

Module Name	Base Address
MIPI_CSI0	0x01CA0000

Register Name	Offset	Register name
MIPI_CSI2_CTL	0x0000	MIPI CSI-2 Control Register
MIPI_CSI2_CFG	0x0004	MIPI CSI-2 Configuration Register
MIPI_CSI2_VCDT_RX	0x0008	MIPI CSI-2 Virtual Channel and Data Type Receive Register
MIPI_CSI2_RX_PKT_NUM	0x000C	MIPI CSI-2 Received Packet Number Register
MIPI_CSI2_VER	0x003C	MIPI CSI-2 Version Register
MIPI_CSI2_CH0_CFG	0x0040	MIPI CSI-2 CH0 Configuration Register
MIPI_CSI2_CH0_INT_EN	0x0050	MIPI CSI-2 CH0 Interrupt Enable Register
MIPI_CSI2_CH0_INT_PD	0x0058	MIPI CSI-2 CH0 Interrupt Pending Register
MIPI_CSI2_CH0_DT_TRM	0x0060	MIPI CSI-2 CH0 Data Type Trigger Masked Register
MIPI_CSI2_CH0_CUR_PH	0x0070	MIPI CSI-2 CH0 Current Packet Header Register
MIPI_CSI2_CH0_ECC	0x0074	MIPI CSI-2 CH0 ECC Register
MIPI_CSI2_CH0_CKS	0x0078	MIPI CSI-2 CH0 Check Sum Register
MIPI_CSI2_CH0_FRAME_NUM	0x007C	MIPI CSI-2 CH0 Frame Number Register
MIPI_CSI2_CH0_LINE_NUM	0x0080	MIPI CSI-2 CH0 Line Number Register
MIPI_CSI2_CH1_CFG	0x0140	MIPI CSI-2 CH1 Configuration Register

MIPI_CSI2_CH1_INT_EN	0x0150	MIPI CSI-2 CH1 Interrupt Enable Register
MIPI_CSI2_CH1_INT_PD	0x0158	MIPI CSI-2 CH1 Interrupt Pending Register
MIPI_CSI2_CH1_DT_TRM	0x0160	MIPI CSI-2 CH1 Data Type Trigger Masked Register
MIPI_CSI2_CH1_CUR_PH	0x0170	MIPI CSI-2 CH1 Current Packet Header Register
MIPI_CSI2_CH1_ECC	0x0174	MIPI CSI-2 CH1 ECC Register
MIPI_CSI2_CH1_CKS	0x0178	MIPI CSI-2 CH1 Check Sum Register
MIPI_CSI2_CH1_FRAME_NUM	0x017C	MIPI CSI-2 CH1 Frame Number Register
MIPI_CSI2_CH1_LINE_NUM	0x0180	MIPI CSI-2 CH1 Line Number Register
MIPI_CSI2_CH2_CFG	0x0240	MIPI CSI-2 CH2 Configuration Register
MIPI_CSI2_CH2_INT_EN	0x0250	MIPI CSI-2 CH2 Interrupt Enable Register
MIPI_CSI2_CH2_INT_PD	0x0258	MIPI CSI-2 CH2 Interrupt Pending Register
MIPI_CSI2_CH2_DT_TRM	0x0260	MIPI CSI-2 CH2 Data Type Trigger Masked Register
MIPI_CSI2_CH2_CUR_PH	0x0270	MIPI CSI-2 CH2 Current Packet Header Register
MIPI_CSI2_CH2_ECC	0x0274	MIPI CSI-2 CH2 ECC Register
MIPI_CSI2_CH2_CKS	0x0278	MIPI CSI-2 CH2 Check Sum Register
MIPI_CSI2_CH2_FRAME_NUM	0x027C	MIPI CSI-2 CH2 Frame Number Register
MIPI_CSI2_CH2_LINE_NUM	0x0280	MIPI CSI-2 CH2 Line Number Register
MIPI_CSI2_CH3_CFG	0x0340	MIPI CSI-2 CH3 Configuration Register
MIPI_CSI2_CH3_INT_EN	0x0350	MIPI CSI-2 CH3 Interrupt Enable Register
MIPI_CSI2_CH3_INT_PD	0x0358	MIPI CSI-2 CH3 Interrupt Pending Register
MIPI_CSI2_CH3_DT_TRM	0x0360	MIPI CSI-2 CH3 Data Type Trigger Masked Register
MIPI_CSI2_CH3_CUR_PH	0x0370	MIPI CSI-2 CH3 Current Packet Header Register
MIPI_CSI2_CH3_ECC	0x0374	MIPI CSI-2 CH3 ECC Register
MIPI_CSI2_CH3_CKS	0x0378	MIPI CSI-2 CH3 Check Sum Register
MIPI_CSI2_CH3_FRAME_NUM	0x037C	MIPI CSI-2 CH3 Frame Number Register
MIPI_CSI2_CH3_LINE_NUM	0x0380	MIPI CSI-2 CH3 Line Number Register

6.3.5. MIPI CSI REGISTER DESCRIPTION

6.3.5.1. MIPI CSI-2 CONTROL REGISTER

Offset: 0x0000			Register Name: MIPI_CSI2_CTL
Bit	**Read/ Write**	**Default/Hex**	**Description**

31	R/W	0x0	**RST** MIPI CSI-2 Reset 0:Reset valid 1:Reset release Software write this bit to “0” to reset the hardware and write “1” to it to work normally.
30	R/W	0x0	**VER_EN** MIPI CSI-2 Version Register Read Enable: 0: Disable 1: Enable
29:2	/	/	/
1	R/W	0x1	**UNPK_EN** Unpacking Payload Enable: 0: Disable unpacking payload 1: Enable unpacking payload P.S. If disabled, the packet number received is depends on the register **MIPI_CSI2_PKT_NUM**
0	R/W	0x0	**EN** MIPI CSI-2 Enable 0:Disable 1:Enable

6.3.5.2. MIPI CSI-2 CONFIGURATION REGISTER

Offset: 0x0004			**Register Name: MIPI_CSI2_CFG**
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0x0	**CH_MODE** Channel Mode Selection 00: 1 Channel (Use Channel 0) 01: 2 Channels (Use Channel 0,1) 10: 3 Channels (Use Channel 0,1,2) 11: 4 Channels (Use Channel 0,1,2,3)
7	R/W	0x0	**PL_BIT_ORD** Payload Bit Order 0:LSB first 1:MSB first
6	R/W	0x0	**PH_BIT_ORD**

			Packet Header Bit Order for ECC 0:LSB first e.g.{WC,DI}={WC[15:8],WC[7:0],DI[7:0]} 1:MSB first e.g.{WC,DI}={WC[8:15],WC[0:7],DI[0:7]}
5:4	R/W	0x0	**PH_BYTE_ORD** Packet Header Byte Order for ECC 00:{WCh,WCl,DI} 01:{DI,WCh,WCl} 10:{WCl,WCh,DI} 11:{DI,WCl,WCh}
3:2	/	/	/
1:0	R/W	0x0	**DL_CFG** Data Lane Configuration 00: 1 Data Lane 01: 2 Data Lanes 10: 3 Data Lanes 11: 4 Data Lanes

6.3.5.3. MIPI CSI-2 VIRTUAL CHANNEL AND DATA TYPE RECEIVE REGISTER

Offset: 0x0008			**Register Name: MIPI_CSI2_VCDT_RX**
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:30	R/W	0x3	**CH3_VC** Virtual Channel Number for Channel 3 VC[0:1]
29:24	R/W	0x1E	**CH3_DT** Data Type ID for Channel 3 DT[5:0]
23:22	R/W	0x2	**CH2_VC** Virtual Channel Number for Channel 2 VC[0:1]
21:16	R/W	0x1E	**CH2_DT** Data Type ID for Channel 2 DT[5:0]
15:14	R/W	0x1	**CH1_VC** Virtual Channel Number for Channel 1 VC[0:1]
13:8	R/W	0x1E	**CH1_DT** Data Type ID for Channel 1

			DT[5:0]
7:6	R/W	0x0	**CH0_VC** Virtual Channel Number for Channel 0 VC[0:1]
5:0	R/W	0x1E	**CH0_DT** Data Type ID for Channel 0 DT[5:0]

6.3.5.4. MIPI CSI-2 RECEIVED PACKET NUMBER

Offset: 0x000C			Register Name: MIPI_CSI2_RX_PKT_NUM
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**PKT_NUM** The packet numbers received when **MIPI_CSI2_CFG.UNPK_EN = 0**

6.3.5.5. MIPI CSI-2 VERSION REGISTER

Offset: 0x003C			Register Name: MIPI_CSI2_VER
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:0	R	/	**VER** Version of hardware circuit. Only can be read when version register read enable is on.

6.3.5.6. MIPI CSI-2 CH0 CONFIGURATION REGISTER

Offset: 0x0040			Register Name: MIPI_CSI2_CH0_CFG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:04	/	/	/
03	R/W	0x0	**SRC_SEL** The video source is progressed or interlaced 0: Progressed 1: Interlaced
02	R/W	0x0	**ITL_SYNC** The synchronization of interlaced 0: Depends on the frame number received 1: Depends on line number received

01	R/W	0x0	**EMBD_DAT_EN** Receiving the embedded data (DT ID = 0x12) 0: Not receiving the embedded data 1: Receiving the embedded data (including unpacking depends on the data type in the same virtual channel, see **MIPI_CSI2_VCDT_RX**)
00	R/W	0x0	**LINE_SYNC** Line synchronization 0: line valid is toggled at the start/end of long data packets 1: line valid is toggled by line synchronization short packets only P.S. If the actual received payload byte number is more than the word counter after ECC, stop receiving at the end of the word counter.

6.3.5.7. MIPI CSI-2 CH0 INTERRUPT ENABLE REGISTER

Offset: 0x0050			Register Name: MIPI_CSI2_CH0_INT_EN
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	**EOT_ERR_INT** EOT error interrupt.
28	R/W	0x0	**CHKSUM_ERR_INT** Checksum error interrupt
27	R/W	0x0	**ECC_WRN_INT** ECC warning interrupt
26	R/W	0x0	**ECC_ERR_INT** ECC error interrupt
25	R/W	0x0	**LINE_SYNC_ERR_INT** Line synchronization error interrupt
24	R/W	0x0	**FRAME_SYNC_ERR_INT** Frame synchronization error interrupt
23:19	/	/	/
18	R/W	0x0	**EMB_DATA_INT** Embedded data interrupt
17	R/W	0x0	**PF_INT** Packet footer interrupt
16	R/W	0x0	**PH_UPDATE_INT** Packet header update interrupt
15:12	/	/	/

11	R/W	0x0	**LINE_START_SYNC_INT** LS synchronization interrupt
10	R/W	0x0	**LINE_END_SYNC_INT** LE synchronization interrupt
9	R/W	0x0	**FRAME_START_SYNC_INT** FS synchronization interrupt
8	R/W	0x0	**FRAME_END_SYNC_INT** FE synchronization interrupt
7:1	/	/	/
0	R/W	0x0	**FIFO_OVER_INT** FIFO overflow interrupt 0: Disable 1: Enable

6.3.5.8. MIPI CSI-2 CH0 INTERRUPT PENDING REGISTER

Offset: 0x0058			Register Name: MIPI_CSI2_CH0_INT_PD
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	**EOT_ERR_PD** EOT error pending bit. Asserted if the RX detect the packet valid end before the word counter is counted to zero. Write “1” to clear.
28	R/W	0x0	**CHKSUM_ERR_PD** Checksum error pending bit. Asserted if the checksum calculated by the Rx does not match that in the packet footer. Write “1” to clear.
27	R/W	0x0	**ECC_WRN_PD** ECC warning pending bit. Asserted if the ECC has detected and corrected a single bit error. Write “1” to clear.
26	R/W	0x0	**ECC_ERR_PD** ECC error pending bit. Asserted when the ECC detects an unrecoverable error. Write “1” to clear.
25	R/W	0x0	**LINE_SYNC_ERR_PD** Line synchronization error pending bit.

			Asserted if a line end short packet is not paired with a line start channel. Write “1” to clear.
24	R/W	0x0	**FRAME_SYNC_ERR_PD** Frame synchronization error pending bit. Asserted if a frame end short packet is not paired with a frame start channel. Write “1” to clear.
23:19	/	/	/
18	R/W	0x0	**EMB_DATA_PD** Embedded data pending bit. Asserted if current line contains embedded data. Write “1” to clear.
17	R/W	0x0	**PF_PD** Packet footer pending bit. Asserted if a packet footer has been detected as paired with **PH_UPDATE_PD**. The **RXD_CKS[15:0]** and **CAL_CKS[15:0]** fields are updated accordingly. Write “1” to clear.
16	R/W	0x0	**PH_UPDATE_PD** Packet header update pending bit. Asserted if any one of the short/long packet header enabled by the **Data Type Trigger Masked** has been detected. The **CUR_VC[1:0]**, **CUR_DT[5:0]** ,**CUR_WC[15:0] , RXD_ECC [7:0] and CAL_ECC[7:0]** fields are updated accordingly. Write “1” to clear.
15:12	/	/	/
11	R/W	0x0	**LINE_START_SYNC_PD** LS synchronization pending bit. Asserted if LS sync has been detected. Write “1” to clear.
10	R/W	0x0	**LINE_END_SYNC_PD** LE synchronization pending bit. Asserted if LE sync has been detected. Write “1” to clear.
9	R/W	0x0	**FRAME_START_SYNC_PD** FS synchronization pending bit. Asserted if FS sync has been detected.

			Write “1” to clear.
8	R/W	0x0	**FRAME_END_SYNC_PD** FE synchronization pending bit. Asserted if FE sync has been detected. Write “1” to clear.
7:1	/	/	/
0	R/W	0x0	**FIFO_OVER_PD** FIFO overflow pending bit. Asserted if FIFO was overflow. Write “1” to clear.

6.3.5.9. MIPI CSI-2 CH0 DATA TYPE TRIGGER MASKED REGISTER

Offset: 0x0060			Register Name: MIPI_CSI2_CH0_DT_TRM
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	**RAW** RAW Long Packet Data Type 0x28 to 0x2F Trigger Masked: 0: Masked 1: Enabled
18	R/W	0x0	**RGB** RGB Long Packet Data Type 0x20 to 0x27 Trigger Masked: 0: Masked 1: Enabled
17	R/W	0x0	**YUV** YUV Long Packet Data Type 0x18 to 0x1F Trigger Masked: 0: Masked 1: Enabled
16	R/W	0x0	**GL** Generic 8bit Long Packet Data Type 0x10 to 0x17 Trigger Masked: 0: Masked 1: Enabled
15	R/W	0x0	**GS7** Generic 8bit Short Packet Data Type 0x0F Trigger Masked: 0: Masked 1: Enabled
14	R/W	0x0	**GS6**

			Generic Short Packet Data Type 0x0E Trigger Masked: 0: Masked 1: Enabled
13	R/W	0x0	**GS5** Generic Short Packet Data Type 0x0D Trigger Masked: 0: Masked 1: Enabled
12	R/W	0x0	**GS4** Generic Short Packet Data Type 0x0C Trigger Masked: 0: Masked 1: Enabled
11	R/W	0x0	**GS3** Generic Short Packet Data Type 0x0B Trigger Masked: 0: Masked 1: Enabled
10	R/W	0x0	**GS2** Generic Short Packet Data Type 0x0A Trigger Masked: 0: Masked 1: Enabled
9	R/W	0x0	**GS1** Generic Short Packet Data Type 0x09 Trigger Masked: 0: Masked 1: Enabled
8	R/W	0x0	**GS0** Generic Short Packet Data Type 0x08 Trigger Masked: 0: Masked 1: Enabled
7:4	/	/	/
3	R/W	0x0	**LE** Data Type 0x03 Trigger Masked: 0: Masked 1: Enabled
2	R/W	0x0	**LS** Data Type 0x02 Trigger Masked: 0: Masked 1: Enabled
1	R/W	0x0	**FE** Data Type 0x01 Trigger Masked:

			0: Masked 1: Enabled
0	R/W	0x0	**FS** Data Type 0x00 Trigger Masked: 0: Masked 1: Enabled

6.3.5.10. MIPI CSI-2 CH0 CURRENT PACKET HEADER REGISTER

Offset: 0x0070			Register Name: MIPI_CSI2_CH0_CUR_PH
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:16	R	0x0	**CUR_WC** Contents of MIPI short packet data field or long packet word count field (after error correction). Update when Packet header update pending comes.
15:8	/	/	/
7:6	R	0x0	**CUR_VC** Virtual Channel number received as part of the short packet/long packet header (after error correction). Update when Packet header update pending comes.
5:0	R	0x0	**CUR_DT** Data type code received as part of the short packet/long packet header (after error correction). Update when Packet header update pending comes.

6.3.5.11. MIPI CSI-2 CH0 ECC REGISTER

Offset: 0x0074			Register Name: MIPI_CSI2_CH0_ECC
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R	0x0	**CAL_ECC** The ECC value calculated by the RX through the received short packet/long packet header. Update when Packet header update pending comes.
15:8	/	/	/
7:0	R	0x0	**RXD_ECC** The ECC value received as part of the short packet/long packet

			header. Update when Packet header update pending comes.

6.3.5.12. MIPI CSI-2 CH0 CHECK SUM REGISTER

Offset: 0x0078			Register Name: MIPI_CSI2_CH0_CKS
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:16	R	0x0	**CAL_CKS** The checksum value calculated by the RX through the received payload data. Update when Packet footer pending comes.
15:0	R	0x0	**RXD_CKS** The checksum value received in a long packet footer. Update when Packet footer pending comes.

6.3.5.13. MIPI CSI-2 CH0 FRAME NUMBER REGISTER

Offset: 0x007C			Register Name: MIPI_CSI2_CH0_FRAME_NUM
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R	0x0	**FRAME_NUM** Update when **FRAME_START_SYNC_PD** and **FRAME_END_SYNC_PD comes**

6.3.5.14. MIPI CSI-2 CH0 LINE NUMBER REGISTER

Offset: 0x0080			Register Name: MIPI_CSI2_CH0_LINE_NUM
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R	0x0	**LINE_NUM** Update when **LINE_START_SYNC_PD** and **LINE_END_SYNC_PD comes**

6.3.5.15. MIPI CSI-2 CH1 CONFIGURATION REGISTER

Offset: 0x0140			Register Name: MIPI_CSI2_CH1_CFG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:04	/	/	/
03	R/W	0x0	**SRC_SEL**

			The video source is progressed or interlaced 0: Progressed 1: Interlaced
02	R/W	0x0	**ITL_SYNC** The synchronization of interlaced 0: Depends on the frame number received 1: Depends on line number received
01	R/W	0x0	**EMBD_DAT_EN** Receiving the embedded data (DT ID = 0x12) 0: Not receiving the embedded data 1: Receiving the embedded data (including unpacking depends on the data type in the same virtual channel, see **MIPI_CSI2_VCDT_RX**)
00	R/W	0x0	**LINE_SYNC** Line synchronization 0: line valid is toggled at the start/end of long data packets 1: line valid is toggled by line synchronization short packets only P.S. If the actual received payload byte number is more than the word counter after ECC, stop receiving at the end of the word counter.

6.3.5.16. MIPI CSI-2 CH1 INTERRUPT ENABLE REGISTER

Offset: 0x0150			**Register Name: MIPI_CSI2_CH1_INT_EN**
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	**EOT_ERR_INT** EOT error interrupt.
28	R/W	0x0	**CHKSUM_ERR_INT** Checksum error interrupt
27	R/W	0x0	**ECC_WRN_INT** ECC warning interrupt
26	R/W	0x0	**ECC_ERR_INT** ECC error interrupt
25	R/W	0x0	**LINE_SYNC_ERR_INT** Line synchronization error interrupt
24	R/W	0x0	**FRAME_SYNC_ERR_INT** Frame synchronization error interrupt
23:19	/	/	/

18	R/W	0x0	**EMB_DATA_INT** Embedded data interrupt
17	R/W	0x0	**PF_INT** Packet footer interrupt
16	R/W	0x0	**PH_UPDATE_INT** Packet header update interrupt
15:12	/	/	/
11	R/W	0x0	**LINE_START_SYNC_INT** LS synchronization interrupt
10	R/W	0x0	**LINE_END_SYNC_INT** LE synchronization interrupt
9	R/W	0x0	**FRAME_START_SYNC_INT** FS synchronization interrupt
8	R/W	0x0	**FRAME_END_SYNC_INT** FE synchronization interrupt
7:1	/	/	/
0	R/W	0x0	**FIFO_OVER_INT** FIFO overflow interrupt 0: Disable 1: Enable

6.3.5.17. MIPI CSI-2 CH1 INTERRUPT PENDING REGISTER

Offset: 0x0158			**Register Name: MIPI_CSI2_CH1_INT_PD**
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	**EOT_ERR_PD** EOT error pending bit. Asserted if the RX detect the packet valid end before the word counter is counted to zero. Write “1” to clear.
28	R/W	0x0	**CHKSUM_ERR_PD** Checksum error pending bit. Asserted if the checksum calculated by the Rx does not match that in the packet footer. Write “1” to clear.
27	R/W	0x0	**ECC_WRN_PD** ECC warning pending bit. Asserted if the ECC has detected and corrected a single bit error.

			Write “1” to clear.
26	R/W	0x0	**ECC_ERR_PD** ECC error pending bit. Asserted when the ECC detects an unrecoverable error. Write “1” to clear.
25	R/W	0x0	**LINE_SYNC_ERR_PD** Line synchronization error pending bit. Asserted if a line end short packet is not paired with a line start channel. Write “1” to clear.
24	R/W	0x0	**FRAME_SYNC_ERR_PD** Frame synchronization error pending bit. Asserted if a frame end short packet is not paired with a frame start channel. Write “1” to clear.
23:19	/	/	/
18	R/W	0x0	**EMB_DATA_PD** Embedded data pending bit. Asserted if current line contains embedded data. Write “1” to clear.
17	R/W	0x0	**PF_PD** Packet footer pending bit. Asserted if a packet footer has been detected as paired with **PH_UPDATE_PD**. The **RXD_CKS[15:0]** and **CAL_CKS[15:0]** fields are updated accordingly. Write “1” to clear.
16	R/W	0x0	**PH_UPDATE_PD** Packet header update pending bit. Asserted if any one of the short/long packet header enabled by the **Data Type Trigger Masked** has been detected. The **CUR_VC[1:0]**, **CUR_DT[5:0]** ,**CUR_WC[15:0] , RXD_ECC [7:0] and CAL_ECC[7:0]** fields are updated accordingly. Write “1” to clear.
15:12	/	/	/
11	R/W	0x0	**LINE_START_SYNC_PD** LS synchronization pending bit. Asserted if LS sync has been detected. Write “1” to clear.

10	R/W	0x0	**LINE_END_SYNC_PD** LE synchronization pending bit. Asserted if LE sync has been detected. Write “1” to clear.
9	R/W	0x0	**FRAME_START_SYNC_PD** FS synchronization pending bit. Asserted if FS sync has been detected. Write “1” to clear.
8	R/W	0x0	**FRAME_END_SYNC_PD** FE synchronization pending bit. Asserted if FE sync has been detected. Write “1” to clear.
7:1	/	/	/
0	R/W	0x0	**FIFO_OVER_PD** FIFO overflow pending bit. Asserted if FIFO was overflow. Write “1” to clear.

6.3.5.18. MIPI CSI-2 CH1 DATA TYPE TRIGGER MASKED REGISTER

Offset: 0x0160			Register Name: MIPI_CSI2_CH1_DT_TRM
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	**RAW** RAW Long Packet Data Type 0x28 to 0x2F Trigger Masked: 0: Masked 1: Enabled
18	R/W	0x0	**RGB** RGB Long Packet Data Type 0x20 to 0x27 Trigger Masked: 0: Masked 1: Enabled
17	R/W	0x0	**YUV** YUV Long Packet Data Type 0x18 to 0x1F Trigger Masked: 0: Masked 1: Enabled
16	R/W	0x0	**GL** Generic 8bit Long Packet Data Type 0x10 to 0x17 Trigger Masked: 0: Masked

			1: Enabled
15	R/W	0x0	**GS7** Generic 8bit Short Packet Data Type 0x0F Trigger Masked: 0: Masked 1: Enabled
14	R/W	0x0	**GS6** Generic Short Packet Data Type 0x0E Trigger Masked: 0: Masked 1: Enabled
13	R/W	0x0	**GS5** Generic Short Packet Data Type 0x0D Trigger Masked: 0: Masked 1: Enabled
12	R/W	0x0	**GS4** Generic Short Packet Data Type 0x0C Trigger Masked: 0: Masked 1: Enabled
11	R/W	0x0	**GS3** Generic Short Packet Data Type 0x0B Trigger Masked: 0: Masked 1: Enabled
10	R/W	0x0	**GS2** Generic Short Packet Data Type 0x0A Trigger Masked: 0: Masked 1: Enabled
9	R/W	0x0	**GS1** Generic Short Packet Data Type 0x09 Trigger Masked: 0: Masked 1: Enabled
8	R/W	0x0	**GS0** Generic Short Packet Data Type 0x08 Trigger Masked: 0: Masked 1: Enabled
7:4	/	/	/
3	R/W	0x0	**LE** Data Type 0x03 Trigger Masked: 0: Masked 1: Enabled

2	R/W	0x0	**LS** Data Type 0x02 Trigger Masked: 0: Masked 1: Enabled
1	R/W	0x0	**FE** Data Type 0x01 Trigger Masked: 0: Masked 1: Enabled
0	R/W	0x0	**FS** Data Type 0x00 Trigger Masked: 0: Masked 1: Enabled

6.3.5.19. MIPI CSI-2 CH1 CURRENT PACKET HEADER REGISTER

Offset: 0x0170			Register Name: MIPI_CSI2_CH1_CUR_PH
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:16	R	0x0	**CUR_WC** Contents of MIPI short packet data field or long packet word count field (after error correction). Update when Packet header update pending comes.
15:8	/	/	/
7:6	R	0x0	**CUR_VC** Virtual Channel number received as part of the short packet/long packet header (after error correction). Update when Packet header update pending comes.
5:0	R	0x0	**CUR_DT** Data type code received as part of the short packet/long packet header (after error correction). Update when Packet header update pending comes.

6.3.5.20. MIPI CSI-2 CH1 ECC REGISTER

Offset: 0x0174			Register Name: MIPI_CSI2_CH1_ECC
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R	0x0	**CAL_ECC**

			The ECC value calculated by the RX through the received short packet/long packet header. Update when Packet header update pending comes.
15:8	/	/	/
7:0	R	0x0	**RXD_ECC** The ECC value received as part of the short packet/long packet header. Update when Packet header update pending comes.

6.3.5.21. MIPI CSI-2 CH1 CHECK SUM REGISTER

Offset: 0x0178			Register Name: MIPI_CSI2_CH1_CKS
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:16	R	0x0	**CAL_CKS** The checksum value calculated by the RX through the received payload data. Update when Packet footer pending comes.
15:0	R	0x0	**RXD_CKS** The checksum value received in a long packet footer. Update when Packet footer pending comes.

6.3.5.22. MIPI CSI-2 CH1 FRAME NUMBER REGISTER

Offset: 0x017C			Register Name: MIPI_CSI2_CH1_FRAME_NUM
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R	0x0	**FRAME_NUM** Update when **FRAME_START_SYNC_PD** and **FRAME_END_SYNC_PD comes**

6.3.5.23. MIPI CSI-2 CH1 LINE NUMBER REGISTER

Offset: 0x0180			Register Name: MIPI_CSI2_CH1_LINE_NUM
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R	0x0	**LINE_NUM** Update when **LINE_START_SYNC_PD** and **LINE_END_SYNC_PD comes**

6.3.5.24. MIPI CSI-2 CH2 CONFIGURATION REGISTER

Offset: 0x0240			Register Name: MIPI_CSI2_CH2_CFG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:04	/	/	/
03	R/W	0x0	**SRC_SEL** The video source is progressed or interlaced 0: Progressed 1: Interlaced
02	R/W	0x0	**ITL_SYNC** The synchronization of interlaced 0: Depends on the frame number received 1: Depends on line number received
01	R/W	0x0	**EMBD_DAT_EN** Receiving the embedded data (DT ID = 0x12) 0: Not receiving the embedded data 1: Receiving the embedded data (including unpacking depends on the data type in the same virtual channel, see **MIPI_CSI2_VCDT_RX**)
00	R/W	0x0	**LINE_SYNC** Line synchronization 0: line valid is toggled at the start/end of long data packets 1: line valid is toggled by line synchronization short packets only P.S. If the actual received payload byte number is more than the word counter after ECC, stop receiving at the end of the word counter.

6.3.5.25. MIPI CSI-2 CH2 INTERRUPT ENABLE REGISTER

Offset: 0x0250			Register Name: MIPI_CSI2_CH2_INT_EN
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	**EOT_ERR_INT** EOT error interrupt.
28	R/W	0x0	**CHKSUM_ERR_INT** Checksum error interrupt
27	R/W	0x0	**ECC_WRN_INT** ECC warning interrupt
26	R/W	0x0	**ECC_ERR_INT**

			ECC error interrupt
25	R/W	0x0	**LINE_SYNC_ERR_INT** Line synchronization error interrupt
24	R/W	0x0	**FRAME_SYNC_ERR_INT** Frame synchronization error interrupt
23:19	/	/	/
18	R/W	0x0	**EMB_DATA_INT** Embedded data interrupt
17	R/W	0x0	**PF_INT** Packet footer interrupt
16	R/W	0x0	**PH_UPDATE_INT** Packet header update interrupt
15:12	/	/	/
11	R/W	0x0	**LINE_START_SYNC_INT** LS synchronization interrupt
10	R/W	0x0	**LINE_END_SYNC_INT** LE synchronization interrupt
9	R/W	0x0	**FRAME_START_SYNC_INT** FS synchronization interrupt
8	R/W	0x0	**FRAME_END_SYNC_INT** FE synchronization interrupt
7:1	/	/	/
0	R/W	0x0	**FIFO_OVER_INT** FIFO overflow interrupt 0: Disable 1: Enable

6.3.5.26. MIPI CSI-2 CH2 INTERRUPT PENDING REGISTER

Offset: 0x0258			**Register Name: MIPI_CSI2_CH2_INT_PD**
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	**EOT_ERR_PD** EOT error pending bit. Asserted if the RX detect the packet valid end before the word counter is counted to zero. Write “1” to clear.
28	R/W	0x0	**CHKSUM_ERR_PD**

			Checksum error pending bit. Asserted if the checksum calculated by the Rx does not match that in the packet footer. Write “1” to clear.
27	R/W	0x0	**ECC_WRN_PD** ECC warning pending bit. Asserted if the ECC has detected and corrected a single bit error. Write “1” to clear.
26	R/W	0x0	**ECC_ERR_PD** ECC error pending bit. Asserted when the ECC detects an unrecoverable error. Write “1” to clear.
25	R/W	0x0	**LINE_SYNC_ERR_PD** Line synchronization error pending bit. Asserted if a line end short packet is not paired with a line start channel. Write “1” to clear.
24	R/W	0x0	**FRAME_SYNC_ERR_PD** Frame synchronization error pending bit. Asserted if a frame end short packet is not paired with a frame start channel. Write “1” to clear.
23:19	/	/	/
18	R/W	0x0	**EMB_DATA_PD** Embedded data pending bit. Asserted if current line contains embedded data. Write “1” to clear.
17	R/W	0x0	**PF_PD** Packet footer pending bit. Asserted if a packet footer has been detected as paired with **PH_UPDATE_PD**. The **RXD_CKS[15:0]** and **CAL_CKS[15:0]** fields are updated accordingly. Write “1” to clear.
16	R/W	0x0	**PH_UPDATE_PD** Packet header update pending bit. Asserted if any one of the short/long packet header enabled by the **Data Type Trigger Masked** has been detected. The **CUR_VC[1:0]**, **CUR_DT[5:0]** ,**CUR_WC[15:0] , RXD_ECC [7:0] and CAL_ECC[7:0]** fields are updated accordingly.

			Write “1” to clear.
15:12	/	/	/
11	R/W	0x0	**LINE_START_SYNC_PD** LS synchronization pending bit. Asserted if LS sync has been detected. Write “1” to clear.
10	R/W	0x0	**LINE_END_SYNC_PD** LE synchronization pending bit. Asserted if LE sync has been detected. Write “1” to clear.
9	R/W	0x0	**FRAME_START_SYNC_PD** FS synchronization pending bit. Asserted if FS sync has been detected. Write “1” to clear.
8	R/W	0x0	**FRAME_END_SYNC_PD** FE synchronization pending bit. Asserted if FE sync has been detected. Write “1” to clear.
7:1	/	/	/
0	R/W	0x0	**FIFO_OVER_PD** FIFO overflow pending bit. Asserted if FIFO was overflow. Write “1” to clear.

6.3.5.27. MIPI CSI-2 CH2 DATA TYPE TRIGGER MASKED REGISTER

Offset: 0x0260			Register Name: MIPI_CSI2_CH2_DT_TRM
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	**RAW** RAW Long Packet Data Type 0x28 to 0x2F Trigger Masked: 0: Masked 1: Enabled
18	R/W	0x0	**RGB** RGB Long Packet Data Type 0x20 to 0x27 Trigger Masked: 0: Masked 1: Enabled

17	R/W	0x0	**YUV** YUV Long Packet Data Type 0x18 to 0x1F Trigger Masked: 0: Masked 1: Enabled
16	R/W	0x0	**GL** Generic 8bit Long Packet Data Type 0x10 to 0x17 Trigger Masked: 0: Masked 1: Enabled
15	R/W	0x0	**GS7** Generic 8bit Short Packet Data Type 0x0F Trigger Masked: 0: Masked 1: Enabled
14	R/W	0x0	**GS6** Generic Short Packet Data Type 0x0E Trigger Masked: 0: Masked 1: Enabled
13	R/W	0x0	**GS5** Generic Short Packet Data Type 0x0D Trigger Masked: 0: Masked 1: Enabled
12	R/W	0x0	**GS4** Generic Short Packet Data Type 0x0C Trigger Masked: 0: Masked 1: Enabled
11	R/W	0x0	**GS3** Generic Short Packet Data Type 0x0B Trigger Masked: 0: Masked 1: Enabled
10	R/W	0x0	**GS2** Generic Short Packet Data Type 0x0A Trigger Masked: 0: Masked 1: Enabled
9	R/W	0x0	**GS1** Generic Short Packet Data Type 0x09 Trigger Masked: 0: Masked 1: Enabled
8	R/W	0x0	**GS0** Generic Short Packet Data Type 0x08 Trigger Masked:

			0: Masked 1: Enabled
7:4	/	/	/
3	R/W	0x0	**LE** Data Type 0x03 Trigger Masked: 0: Masked 1: Enabled
2	R/W	0x0	**LS** Data Type 0x02 Trigger Masked: 0: Masked 1: Enabled
1	R/W	0x0	**FE** Data Type 0x01 Trigger Masked: 0: Masked 1: Enabled
0	R/W	0x0	**FS** Data Type 0x00 Trigger Masked: 0: Masked 1: Enabled

6.3.5.28. MIPI CSI-2 CH2 CURRENT PACKET HEADER REGISTER

Offset: 0x0270			Register Name: MIPI_CSI2_CH2_CUR_PH
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:16	R	0x0	**CUR_WC** Contents of MIPI short packet data field or long packet word count field (after error correction). Update when Packet header update pending comes.
15:8	/	/	/
7:6	R	0x0	**CUR_VC** Virtual Channel number received as part of the short packet/long packet header (after error correction). Update when Packet header update pending comes.
5:0	R	0x0	**CUR_DT** Data type code received as part of the short packet/long packet header (after error correction). Update when Packet header update pending comes.

6.3.5.29. MIPI CSI-2 CH2 ECC REGISTER

Offset: 0x0274			Register Name: MIPI_CSI2_CH2_ECC
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R	0x0	**CAL_ECC** The ECC value calculated by the RX through the received short packet/long packet header. Update when Packet header update pending comes.
15:8	/	/	/
7:0	R	0x0	**RXD_ECC** The ECC value received as part of the short packet/long packet header. Update when Packet header update pending comes.

6.3.5.30. MIPI CSI-2 CH2 CHECK SUM REGISTER

Offset: 0x0278			Register Name: MIPI_CSI2_CH2_CKS
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:16	R	0x0	**CAL_CKS** The checksum value calculated by the RX through the received payload data. Update when Packet footer pending comes.
15:0	R	0x0	**RXD_CKS** The checksum value received in a long packet footer. Update when Packet footer pending comes.

6.3.5.31. MIPI CSI-2 CH2 FRAME NUMBER REGISTER

Offset: 0x027C			Register Name: MIPI_CSI2_CH2_FRAME_NUM
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R	0x0	**FRAME_NUM** Update when **FRAME_START_SYNC_PD** and **FRAME_END_SYNC_PD comes**

6.3.5.32. MIPI CSI-2 CH2 LINE NUMBER REGISTER

Offset: 0x0280			Register Name: MIPI_CSI2_CH2_LINE_NUM
Bit	**Read/**	**Default/Hex**	**Description**

	Write		
31:16	/	/	/
15:0	R	0x0	**LINE_NUM** Update when **LINE_START_SYNC_PD** and **LINE_END_SYNC_PD comes**

6.3.5.33. MIPI CSI-2 CH3 CONFIGURATION REGISTER

Offset: 0x0340			Register Name: MIPI_CSI2_CH3_CFG
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:04	/	/	/
03	R/W	0x0	**SRC_SEL** The video source is progressed or interlaced 0: Progressed 1: Interlaced
02	R/W	0x0	**ITL_SYNC** The synchronization of interlaced 0: Depends on the frame number received 1: Depends on line number received
01	R/W	0x0	**EMBD_DAT_EN** Receiving the embedded data (DT ID = 0x12) 0: Not receiving the embedded data 1: Receiving the embedded data (including unpacking depends on the data type in the same virtual channel, see **MIPI_CSI2_VCDT_RX**)
00	R/W	0x0	**LINE_SYNC** Line synchronization 0: line valid is toggled at the start/end of long data packets 1: line valid is toggled by line synchronization short packets only P.S. If the actual received payload byte number is more than the word counter after ECC, stop receiving at the end of the word counter.

6.3.5.34. MIPI CSI-2 CH3 INTERRUPT ENABLE REGISTER

Offset: 0x0350			Register Name: MIPI_CSI2_CH3_INT_EN
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	**EOT_ERR_INT** EOT error interrupt.

28	R/W	0x0	**CHKSUM_ERR_INT** Checksum error interrupt
27	R/W	0x0	**ECC_WRN_INT** ECC warning interrupt
26	R/W	0x0	**ECC_ERR_INT** ECC error interrupt
25	R/W	0x0	**LINE_SYNC_ERR_INT** Line synchronization error interrupt
24	R/W	0x0	**FRAME_SYNC_ERR_INT** Frame synchronization error interrupt
23:19	/	/	/
18	R/W	0x0	**EMB_DATA_INT** Embedded data interrupt
17	R/W	0x0	**PF_INT** Packet footer interrupt
16	R/W	0x0	**PH_UPDATE_INT** Packet header update interrupt
15:12	/	/	/
11	R/W	0x0	**LINE_START_SYNC_INT** LS synchronization interrupt
10	R/W	0x0	**LINE_END_SYNC_INT** LE synchronization interrupt
9	R/W	0x0	**FRAME_START_SYNC_INT** FS synchronization interrupt
8	R/W	0x0	**FRAME_END_SYNC_INT** FE synchronization interrupt
7:1	/	/	/
0	R/W	0x0	**FIFO_OVER_INT** FIFO overflow interrupt 0: Disable 1: Enable

6.3.5.35. MIPI CSI-2 CH3 INTERRUPT PENDING REGISTER

Offset: 0x0358			Register Name: MIPI_CSI2_CH3_INT_PD
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:30	/	/	/

29	R/W	0x0	**EOT_ERR_PD** EOT error pending bit. Asserted if the RX detect the packet valid end before the word counter is counted to zero. Write “1” to clear.
28	R/W	0x0	**CHKSUM_ERR_PD** Checksum error pending bit. Asserted if the checksum calculated by the Rx does not match that in the packet footer. Write “1” to clear.
27	R/W	0x0	**ECC_WRN_PD** ECC warning pending bit. Asserted if the ECC has detected and corrected a single bit error. Write “1” to clear.
26	R/W	0x0	**ECC_ERR_PD** ECC error pending bit. Asserted when the ECC detects an unrecoverable error. Write “1” to clear.
25	R/W	0x0	**LINE_SYNC_ERR_PD** Line synchronization error pending bit. Asserted if a line end short packet is not paired with a line start channel. Write “1” to clear.
24	R/W	0x0	**FRAME_SYNC_ERR_PD** Frame synchronization error pending bit. Asserted if a frame end short packet is not paired with a frame start channel. Write “1” to clear.
23:19	/	/	/
18	R/W	0x0	**EMB_DATA_PD** Embedded data pending bit. Asserted if current line contains embedded data. Write “1” to clear.
17	R/W	0x0	**PF_PD** Packet footer pending bit. Asserted if a packet footer has been detected as paired with **PH_UPDATE_PD**. The **RXD_CKS[15:0]** and **CAL_CKS[15:0]** fields are updated accordingly. Write “1” to clear.
16	R/W	0x0	**PH_UPDATE_PD**

			Packet header update pending bit. Asserted if any one of the short/long packet header enabled by the **Data Type Trigger Masked** has been detected. The **CUR_VC[1:0]**, **CUR_DT[5:0]** ,**CUR_WC[15:0] , RXD_ECC [7:0] and CAL_ECC[7:0]** fields are updated accordingly. Write “1” to clear.
15:12	/	/	/
11	R/W	0x0	**LINE_START_SYNC_PD** LS synchronization pending bit. Asserted if LS sync has been detected. Write “1” to clear.
10	R/W	0x0	**LINE_END_SYNC_PD** LE synchronization pending bit. Asserted if LE sync has been detected. Write “1” to clear.
9	R/W	0x0	**FRAME_START_SYNC_PD** FS synchronization pending bit. Asserted if FS sync has been detected. Write “1” to clear.
8	R/W	0x0	**FRAME_END_SYNC_PD** FE synchronization pending bit. Asserted if FE sync has been detected. Write “1” to clear.
7:1	/	/	/
0	R/W	0x0	**FIFO_OVER_PD** FIFO overflow pending bit. Asserted if FIFO was overflow. Write “1” to clear.

6.3.5.36. MIPI CSI-2 CH3 DATA TYPE TRIGGER MASKED REGISTER

Offset: 0x0360			**Register Name: MIPI_CSI2_CH3_DT_TRM**
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	**RAW** RAW Long Packet Data Type 0x28 to 0x2F Trigger Masked: 0: Masked 1: Enabled

18	R/W	0x0	**RGB** RGB Long Packet Data Type 0x20 to 0x27 Trigger Masked: 0: Masked 1: Enabled
17	R/W	0x0	**YUV** YUV Long Packet Data Type 0x18 to 0x1F Trigger Masked: 0: Masked 1: Enabled
16	R/W	0x0	**GL** Generic 8bit Long Packet Data Type 0x10 to 0x17 Trigger Masked: 0: Masked 1: Enabled
15	R/W	0x0	**GS7** Generic 8bit Short Packet Data Type 0x0F Trigger Masked: 0: Masked 1: Enabled
14	R/W	0x0	**GS6** Generic Short Packet Data Type 0x0E Trigger Masked: 0: Masked 1: Enabled
13	R/W	0x0	**GS5** Generic Short Packet Data Type 0x0D Trigger Masked: 0: Masked 1: Enabled
12	R/W	0x0	**GS4** Generic Short Packet Data Type 0x0C Trigger Masked: 0: Masked 1: Enabled
11	R/W	0x0	**GS3** Generic Short Packet Data Type 0x0B Trigger Masked: 0: Masked 1: Enabled
10	R/W	0x0	**GS2** Generic Short Packet Data Type 0x0A Trigger Masked: 0: Masked 1: Enabled
9	R/W	0x0	**GS1** Generic Short Packet Data Type 0x09 Trigger Masked:

			0: Masked 1: Enabled
8	R/W	0x0	**GS0** Generic Short Packet Data Type 0x08 Trigger Masked: 0: Masked 1: Enabled
7:4	/	/	/
3	R/W	0x0	**LE** Data Type 0x03 Trigger Masked: 0: Masked 1: Enabled
2	R/W	0x0	**LS** Data Type 0x02 Trigger Masked: 0: Masked 1: Enabled
1	R/W	0x0	**FE** Data Type 0x01 Trigger Masked: 0: Masked 1: Enabled
0	R/W	0x0	**FS** Data Type 0x00 Trigger Masked: 0: Masked 1: Enabled

6.3.5.37. MIPI CSI-2 CH3 CURRENT PACKET HEADER REGISTER

Offset: 0x0370			**Register Name: MIPI_CSI2_CH3_CUR_PH**
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:16	R	0x0	**CUR_WC** Contents of MIPI short packet data field or long packet word count field (after error correction). Update when Packet header update pending comes.
15:8	/	/	/
7:6	R	0x0	**CUR_VC** Virtual Channel number received as part of the short packet/long packet header (after error correction). Update when Packet header update pending comes.

5:0	R	0x0	**CUR_DT** Data type code received as part of the short packet/long packet header (after error correction). Update when Packet header update pending comes.

6.3.5.38. MIPI CSI-2 CH3 ECC REGISTER

Offset: 0x0374			Register Name: MIPI_CSI2_CH3_ECC
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R	0x0	**CAL_ECC** The ECC value calculated by the RX through the received short packet/long packet header. Update when Packet header update pending comes.
15:8	/	/	/
7:0	R	0x0	**RXD_ECC** The ECC value received as part of the short packet/long packet header. Update when Packet header update pending comes.

6.3.5.39. MIPI CSI-2 CH3 CHECK SUM REGISTER

Offset: 0x0378			Register Name: MIPI_CSI2_CH3_CKS
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:16	R	0x0	**CAL_CKS** The checksum value calculated by the RX through the received payload data. Update when Packet footer pending comes.
15:0	R	0x0	**RXD_CKS** The checksum value received in a long packet footer. Update when Packet footer pending comes.

6.3.5.40. MIPI CSI-2 CH3 FRAME NUMBER REGISTER

Offset: 0x037C			Register Name: MIPI_CSI2_CH3_FRAME_NUM
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R	0x0	**FRAME_NUM** Update when **FRAME_START_SYNC_PD** and

			FRAME_END_SYNC_PD comes

6.3.5.41. MIPI CSI-2 CH3 LINE NUMBER REGISTER

Offset: 0x0380			**Register Name: MIPI_CSI2_CH3_LINE_NUM**
Bit	**Read/ Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R	0x0	**LINE_NUM** Update when **LINE_START_SYNC_PD** and **LINE_END_SYNC_PD comes**

7 DISPLAY

This chapter introduces A31 display capability from six perspectives:

- TCON
- DEFE
- DEBE
- HDMI
- MIPI DSI
- IEP

7.1. TCON

7.1.1. OVERVIEW

The LCD/TV timing controller features:

- Support dual LCD output
- Support LVDS interface with single/dual link, up to 1920x1080@60fps
- Support RGB interface with DE/SYNC mode, up to 2048x1536@60fps
- Support serial RGB/dummy RGB/CCIR656 interface, up to 1280x720@60fps
- Support i80 interface with 18/16/9/8 bit, support TE, up to 1280x720@60fps
- Support pixel format: RGB888, RGB666 and RGB565
- Dither function for RGB666/RGB565/RGB888
- Gamma correction with R/G/B channel independence

7.1.2. TCON BLOCK DIAGRAM

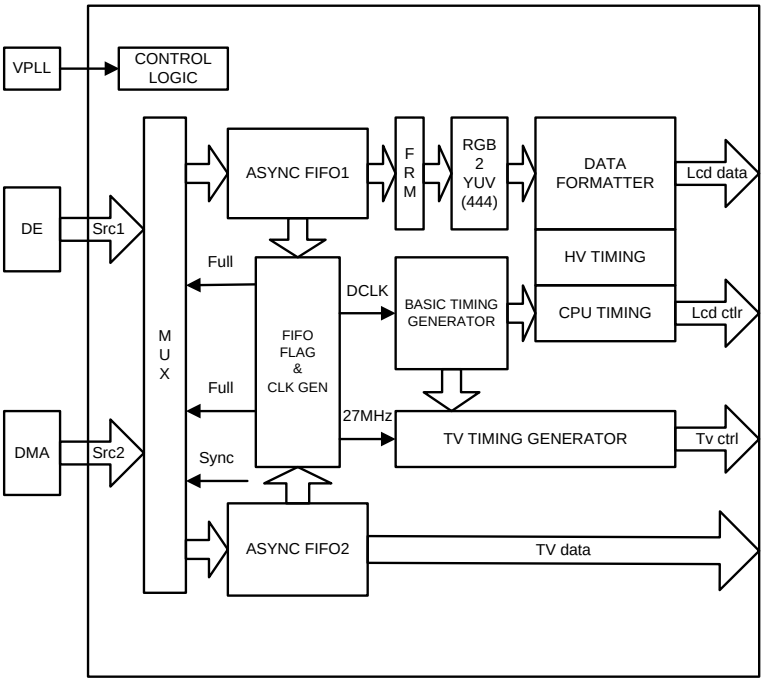


Figure 7-1 TCON Block Diagram

7.1.3. TCON DESCRIPTION

HV_I/F(Sync+DE Mode)

HV I/F is also known as Sync + DE mode, which is widely used in TFT LCD module for PMP/MP4 applications.

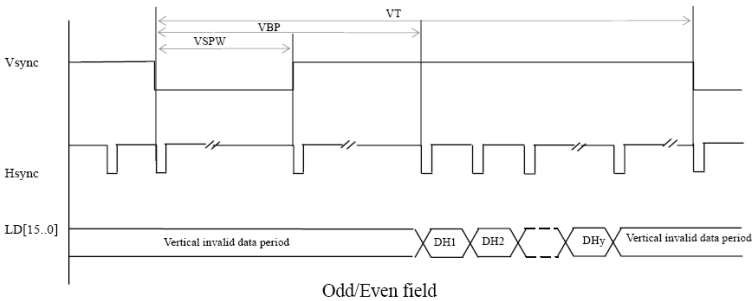
Its signals are defined as below:

Main Signal	I/O type	Description
Vsync	O	Vertical sync, indicates one new frame
Hsync	O	Horizontal sync, indicate one new scan line
DCLK	O	Dot clock, pixel data are sync by this clock
LDE	O	LCD data enable
LD[23..0]	O	24Bit RGB/YUV output from input FIFO for panel

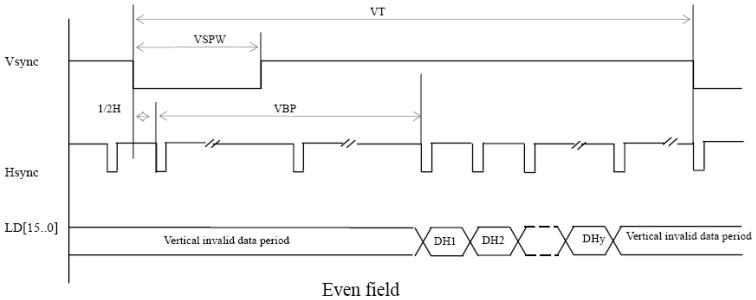
HV control signals are active low.

Panel interface timing

Verital Timing:

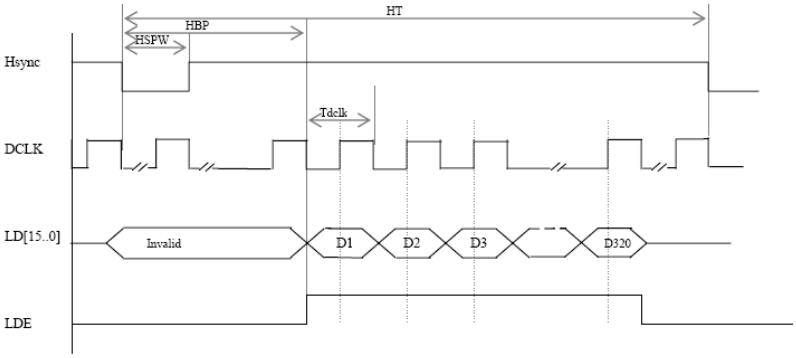


Odd/Even field

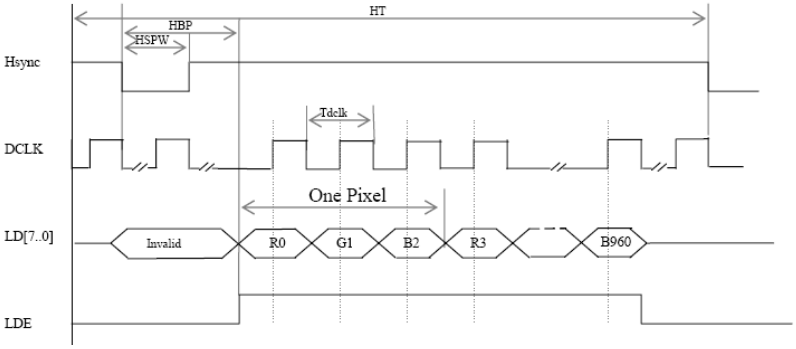


Even field

Parallel Mode Horizontal Timing:



Serial Mode Horizontal Timing:



CCIR output SAV/EAV sync signal

When in HV serial YUV output mode, it's timing is CCIR656/601 compatible. SAV add right before active area every line; EAV add right after active area every line.

The logic is:

F = "0" for Field 1 F = "1" for Field 2

V = "1" during vertical blanking

H = "0" at SAV H = "1" at EAV

P3–P0 = protection bits

P3 = V ⊕ H

P2 = F ⊕ H

P1 = F ⊕ V

P0 = F ⊕ V ⊕ H

(⊕ represents the exclusive-OR function)

The 4 byte SAV/EAV sequences are:

	8-bit Data								10-bit Data	
	D9 (MSB)	D8	D7	D6	D5	D4	D3	D2	D1	D0
preamble	1	1	1	1	1	1	1	1	1	1
	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0
status word	1	F	V	H	P3	P2	P1	P0	0	0

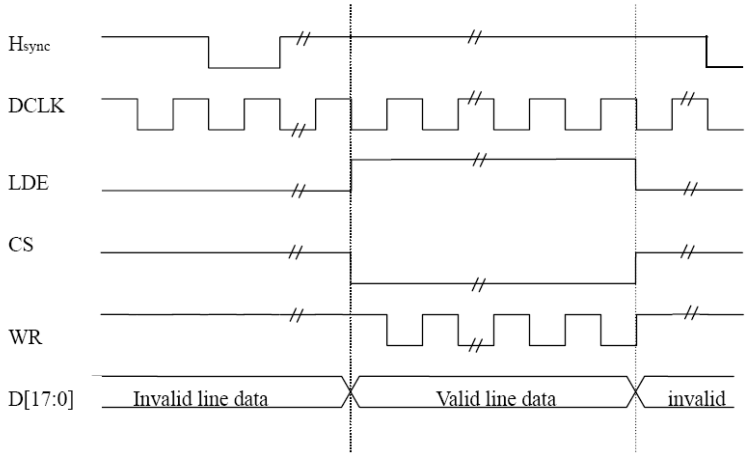
CPU_I/F

CPU I/F LCD panel is the most common interface used for small size, low resolution LCD panels.

Main Signal	I/O type	Description
CS	O	Chip select, active low
WR	O	Write strobe, active low
RD	O	Read strobe, active low
A1	O	Address bit, controlled by "**LCD_CPUI/F**" BIT21
D[17..0]	I/O	Digital RGB output signal

CPU control signals are active low.

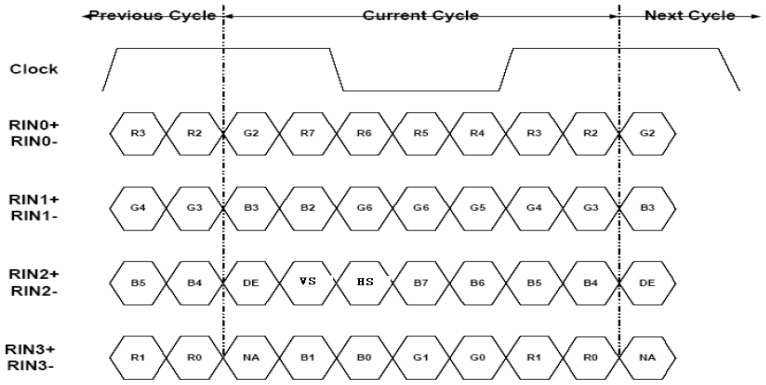
Following figure illustrates the relationship between basic timing and CPU timing. WR is 180 degree delay of DCLK; CS is active when pixel data is valid; RD is always set to 1; A1 are set by **Lcd_CPUI/F**.



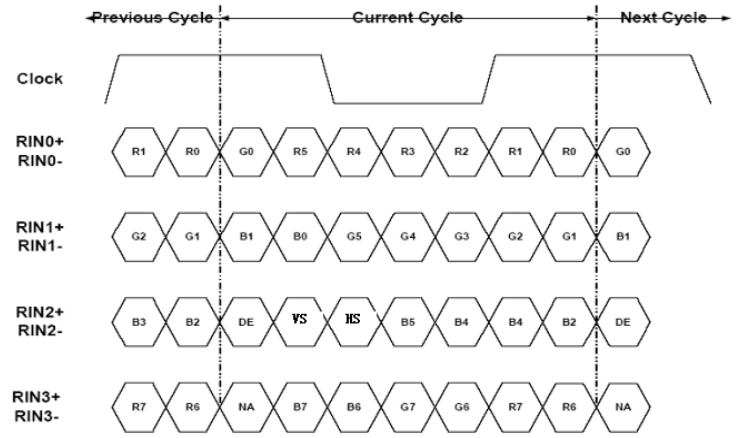
When CPU I/F is in IDLE state, it can generate WR/RD timing by setting **Lcd_CPUI/F**. CS strobe is one DCLK width, and WR/RD strobe is half DCLK width.

LVDS_IF

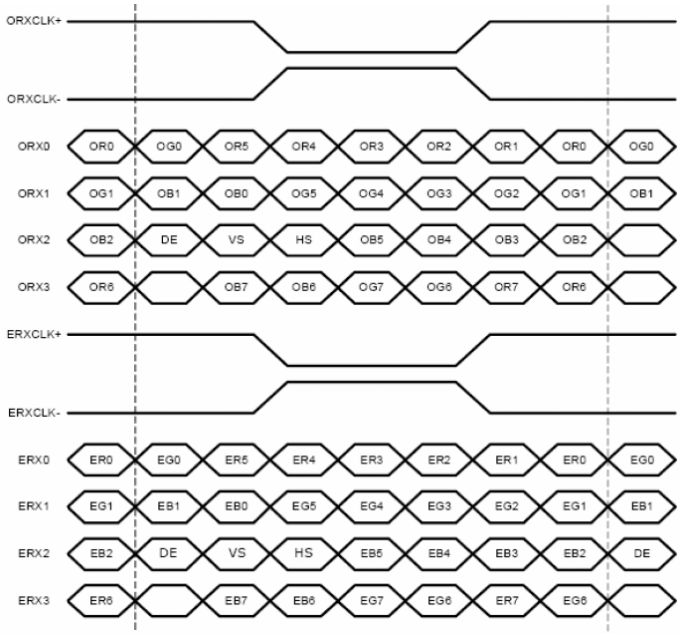
Single channel: JEDIA mode



Single channel: NS mode



Dual channel: NS mode



Notes: odd data is the first data.

PIN assignment:

SINGLE		DUAL	
LCDC0	GND	LCDC0/ LCDC1	GND
	RIN0-		ORX0-
	RIN0+		ORX0+
	RIN1-		ORX1-
	RIN1+		ORX1+
	VCC		VCC
	GND		GND
	RIN2-		ORX2-
	RIN2+		ORX2+
	RINCLK-		ORXCLK-
	RINCLK+		ORXCLK+
	RIN3-		ORX3-
	RIN3+		ORX3+
LCDC1	GND		GND
	RIN0-		ERX0-
	RIN0+		ERX0+
	RIN1-		ERX1-
	RIN1+		ERX1+
	VCC		VCC
	GND		GND
	RIN2-		ERX2-
	RIN2+		ERX2+
	RINC-		ERXCLK-
	RINC+		ERXCLK+
	RIN3-		ERX3-
	RIN3+		ERX3+
	GND		GND

7.1.4. TCON REGISTER LIST

Module Name	Base Address
TCON	0x01C0C000

Register Name	Offset	Description

TCON_GCTL_REG	0x0000	TCON Global Control Register
TCON_GINT0_REG	0x0004	TCON Global Interrupt Register0
TCON_GINT1_REG	0x0008	TCON Global Interrupt Register1
TCON0_FRM_CTL_REG	0x0010	TCON FRM Control Register
TCON0_CTL_REG	0x0040	TCON0 Control Register
TCON0_DCLK_REG	0x0044	TCON0 Data Clock Register
TCON0_BASIC0_REG	0x0048	TCON0 Basic Timing Register0
TCON0_BASIC1_REG	0x004C	TCON0 Basic Timing Register1
TCON0_BASIC2_REG	0x0050	TCON0 Basic Timing Register2
TCON0_BASIC3_REG	0x0054	TCON0 Basic Timing Register3
TCON0_HV_IF_REG	0x0058	TCON0 Hv Panel Interface Register
TCON0_CPU_IF_REG	0x0060	TCON0 CPU Panel Interface Register
TCON0_CPU_WR_REG	0x0064	TCON0 CPU Panel Write Data Register
TCON0_CPU_RD0_REG	0x0068	TCON0 CPU Panel Read Data Register0
TCON0_CPU_RD1_REG	0x006C	TCON0 CPU Panel Read Data Register1
TCON0_LVDS_IF_REG	0x0084	TCON0 LVDS Panel Interface Register
TCON0_IO_POL_REG	0x0088	TCON0 IO Polarity Register
TCON0_IO_TRI_REG	0x008C	TCON0 IO Control Register
TCON1_CTL_REG	0x0090	TCON1 Control Register
TCON1_BASIC0_REG	0x0094	TCON1 Basic Timing Register0
TCON1_BASIC1_REG	0x0098	TCON1 Basic Timing Register1
TCON1_BASIC2_REG	0x009C	TCON1 Basic Timing Register2
TCON1_BASIC3_REG	0x00A0	TCON1 Basic Timing Register3
TCON1_BASIC4_REG	0x00A4	TCON1 Basic Timing Register4
TCON1_BASIC5_REG	0x00A8	TCON1 Basic Timing Register5
TCON1_IO_POL_REG	0x00F0	TCON1 IO Polarity Register
TCON1_IO_TRI_REG	0x00F4	TCON1 IO Control Register
TCON_CEU_CTL_REG	0x0100	TCON CEU Control Register
TCON0_CPU_TRI0_REG	0x0160	TCON0 CPU Panel Trigger Register0
TCON0_CPU_TRI1_REG	0x0164	TCON0 CPU Panel Trigger Register1
TCON0_CPU_TRI2_REG	0x0168	TCON0 CPU Panel Trigger Register2
TCON0_CPU_TRI3_REG	0x016C	TCON0 CPU Panel Trigger Register3
TCON_CMAP_CTL_REG	0x0180	TCON Color Map Control Register
TCON_CMAP_ODD0_REG	0x0190	TCON Color Map Odd Line Register0
TCON_CMAP_ODD1_REG	0x0194	TCON Color Map Odd Line Register1
TCON_CMAP_EVEN0_REG	0x0198	TCON Color Map Even Line Register0
TCON_CMAP_EVEN1_REG	0x019C	TCON Color Map Even Line Register1

TCON_MUX_CTL_REG	0x0200	TCON MUX Control Register

7.1.5. TCON REGISTER DESCRIPTION

7.1.5.1. TCON_GCTL_REG

Offset: 0x000			Register Name: TCON global control register
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0	**TCON_En** 0: disable 1: enable When it's disabled, the module will be reset to idle state.
30	R/W	0	**TCON_Gamma_En** 0: disable 1: enable
29:0	/	/	**/**

7.1.5.2. TCON_GINT0_REG

Offset: 0x004			Register Name: TCON global interrupt register0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0	**TCON0_Vb_Int_En** 0: disable 1: enable
30	R/W	0	**TCON1_Vb_Int_En** 0: disable 1: enable
29	R/W	0	**TCON0_Line_Int_En** 0: disable 1: enable
28	R/W	0	**TCON1_Line_Int_En** 0: disable 1: enable
27	R/W	0	**TCON0_Tri_Finish_Int_En** 0: disable 1: enable
26:	R/W	0	**TCON0_Tri_Counter_Int_En** 0: disable

			1: enable
25:16	/	/	/
15	R/W	0	**TCON0_Vb_Int_Flag** Asserted during vertical no-display period every frame. Write 0 to clear it.
14	R/W	0	**TCON1_Vb_Int_Flag** Asserted during vertical no-display period every frame. Write 0 to clear it.
13	R/W	0	**TCON0_Line_Int_Flag** trigger when SY0 match the current TCON0 scan line Write 0 to clear it.
12	R/W	0	**TCON1_Line_Int_Flag** trigger when SY1 match the current TCON1 scan line Write 0 to clear it.
11	R/W	0	**TCON0_Tri_Finish_Int_Flag** trigger when cpu trigger mode finish Write 0 to clear it.
10	R/W	0	**TCON0_Tri_Counter_Int_Flag** trigger when tri counter reache this value Write 0 to clear it.
9:0	/	/	/

7.1.5.3. TCON_GINT1_REG

Offset: 0x008			**Register Name: TCON global interrupt register1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0	**TCON0_Line_Int_Num** scan line for TCON0 line trigger(including inactive lines) Setting it for the specified line for trigger0. Note: SY0 is writable only when LINE_TRG0 disable.
15:12	/	/	/
11:0	R/W	0	**TCON1_Line_Int_Num** scan line for TCON1 line trigger(including inactive lines) Setting it for the specified line for trigger 1. Note: SY1 is writable only when LINE_TRG1 disable.

7.1.5.4. TCON0_FRM_CTL_REG

Offset: 0x010			Register Name: TCON FRM control register
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0	**TCON0_Frm_En** 0:disable 1:enable
30:12	/	/	**/**
6	R/W	0	**TCON0_Frm_Mode_R** 0: 6bit frm output 1: 5bit frm output
5	R/W	0	**TCON0_Frm_Mode_G** 0: 6bit frm output 1: 5bit frm output
4	R/W	0	**TCON0_Frm_Mode_B** 0: 6bit frm output 1: 5bit frm output
1:0	R/W	0	**TCON0_Frm_Test** 00: FRM 01: half 5/6bit, half FRM 10: half 8bit, half FRM 11: half 8bit, half 5/6bit

7.1.5.5. TCON0_CTL_REG

Offset: 0x040			Register Name: TCON0 control register
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0	**TCON0_En** 0: disable 1: enable Note: It executes at the beginning of the first blank line of TCON0 timing.
30:29	/	/	**/**
28	R/W	0	**TCON0_Work_Mode** 0: normal 1: dynamic freq
27:26	/	/	**/**
25:24	R/W	0	**TCON0_IF** 00: HV(Sync+DE)

			01: 8080 I/F 10: / 11: reserved
23	R/W	0	**TCON0_RB_Swap** 0: default 1: swap RED and BLUE data at FIFO1
22	/	/	**/**
21	R/W	0	**TCON0_FIFO1_Rst** Write 1 and then 0 at this bit will reset FIFO 1 Note: 1 holding time must more than 1 DCLK
20	/	/	**/**
19:9	/	/	**/**
8:4	R/W	0	**TCON0_Start_Delay** STA delay NOTE: valid only when **TCON0_EN == 1**
3	/	/	**/**
2:0	R/W	0	**TCON0_SRC_SEL:** 000: DE0 001: DE1 010: DMA RGBA888 input(FIFO1 enable) 011: DMA RGB565 input(FIFO1 enable) 100: Test Data all 0 101: Test Data all 1 11x: reservd when set as DMA RGBA888 input DMA Des Bus Width should config as “32bit” when set as DMA RGB565 input DMA Des Bus Width should config as “16bit”

7.1.5.6. TCON0_DCLK REG

Offset: 0x044			Register Name: TCON0 data clock register
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7			
6:0	R/W	0	**TCON0_Dclk_Div** Tdclk = Tsclk * DCLKDIV Note: 1.if dclk1&dclk2 used，DCLKDIV >=6

			2.if dclk only，DCLKDIV >=1

7.1.5.7. TCON0_BASIC0_REG

Offset: 0x048			Register Name: TCON0 basic timing register0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	**/**
27:16	R/W	0	**TCON0_X** Panel width is X+1
15:12	/	/	**/**
11:0	R/W	0	**TCON0_Y** Panel height is Y+1

7.1.5.8. TCON0_BASIC1_REG

Offset: 0x04C			Register Name: TCON0 basic timing register1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	**/**
30:29	/	/	**/**
28:16	R/W	0	**HT** Thcycle = (HT+1) * Tdclk Computation 1) parallel:HT = X + BLANK Limitation: 1) parallel :HT >= (HBP +1) + (X+1) +2 2) serial 1: HT >= (HBP +1) + (X+1) *3+2 3) serial 2: HT >= (HBP +1) + (X+1) *3/2+2
15:12	/	/	**/**
11:0	R/W	0	**HBP** horizontal back porch (in dclk) Thbp = (HBP +1) * Tdclk

7.1.5.9. TCON0_BASIC2_REG

Offset: 0x050			Register Name: TCON0 basic timing register2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	**/**
28:16	R/W	0	**VT** TVT = (VT)/2 * Thsync Note: VT/2 >= (VBP+1) + (Y+1) +2

15:12	/	/	**/**
11:0	R/W	0	**VBP** Tvbp = (VBP +1) * Thsync

7.1.5.10. TCON0_BASIC3_REG

Offset: 0x054			Register Name: TCON0 basic timing register3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	**/**
25:16	R/W	0	**HSPW** Thspw = (HSPW+1) * Tdclk Note: HT> (HSPW+1)
15:10	/	/	**/**
9:0	R/W	0	**VSPW** Tvspw = (VSPW+1) * Thsync Note: VT/2 > (VSPW+1)

7.1.5.11. TCON0_HV_IF_REG

Offset: 0x058			Register Name: TCON0 hv panel interface register
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0	**HV_Mode** 0000: 24bit/1cycle parallel mode 1000: 8bit/3cycle RGB serial mode(RGB888) 1010: 8bit/4cycle Dummy RGB(DRGB) 1011: 8bit/4cycle RGB Dummy(RGBD) 1100: 8bit/2cycle YUV serial mode(CCIR656)
27:26	R/W	0	**RGB888_SM0** serial RGB888 mode Output sequence at odd lines of the panel (line 1, 3, 5, 7…) 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B
25:24	R/W	0	**RGB888_SM1** serial RGB888 mode Output sequence at even lines of the panel (line 2, 4, 6, 8…) 00: R→G→B 01: B→R→G

			10: G→B→R 11: R→G→B
23:22	R/W	0	**YUV_SM** serial YUV mode Output sequence 2-pixel-pair of every scan line 00: YUYV 01: YVYU 10: UYVY 11: VYUY
21:20	R/W	0	**YUV EAV/SAV F line delay** 0:F toggle right after active video line 1:delay 2 line(CCIR NTSC) 2:delay 3 line(CCIR PAL) 3:reserved
19：0	/	/	**/**

7.1.5.12. TCON0_CPU_IF_REG

Offset: 0x060			Register Name: TCON0 cpu panel interface register
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0	**CPU_MOD** 0000: 18bit/256K mode 0010: 16bit mode0 0100: 16bit mode1 0110: 16bit mode2 1000: 16bit mode3 1010: 9bit mode 1100: 8bit 256K mode 1110: 8bit 65K mode xxx1: 24bit for DSI
27	/	/	**/**
26	R/W	0	**DA** pin A1 value in 8080 mode auto/flash states
25	R/W	0	**CA** pin A1 value in 8080 mode WR/RD execute
24	/	/	**/**
23	R	0	**Wr_Flag** 0:write operation is finishing

			1:write operation is pending
22	R	0	**Rd_Flag** 0:read operation is finishing 1:read operation is pending
21:18	/	/	**/**
17	R/W	0	**AUTO** auto Transfer Mode: If it's 1, all the valid data during this frame are write to panel. Note: This bit is sampled by Vsync
16	R/W	0	**FLUSH** direct transfer mode: If it's enabled, FIFO1 is regardless of the HV timing, pixels data keep being transferred unless the input FIFO was empty. Data output rate control by DCLK.
15:6	/	/	**/**
5:4	R/W	0	**Trigger_Sync_Mode** 0: start frame flush immediately by bit1. 1: start frame flush sync to TE PIN. rising by bit1. 2. start frame flush sync to TE PIN. falling by bit1. when set as 1 or 2, io0 is map as TE input.
3	R/W	0	**Trigger_FIFO_Bist_En** 0: disable 1: enable Entry addr is 0xFF8
2	R/W	0	**Trigger_FIFO_En** 0:enable 1:disable
1	R/W	0	**Trigger_Start** write '1' to start a frame flush, write'0' has no effect. this flag indicated frame flush is running sofeware must make sure write '1' only when this flag is '0'.
0	R/W	0	**Trigger_En** 0: trigger mode disable 1: trigger mode enable

7.1.5.13. TCON0_CPU_WR_REG

Offset: 0x064	Register Name: TCON0 cpu panel write data register

Bit	Read/Write	Default/Hex	Description
31:0	/	/	/
23:0	W	0	**Data_Wr** data write on 8080 bus, launch a write operation on 8080 bus

7.1.5.14. TCON0_CPU_RD0_REG

Offset: 0x068			Register Name: TCON0 cpu panel read data register0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	**/**
23:0	R	/	**Data_Rd0** data read on 8080 bus, launch a new read operation on 8080 bus

7.1.5.15. TCON0_CPU_RD1_REG

Offset: 0x06C			Register Name: TCON0 cpu panel read data register1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	**/**
23:0	R	/	**Data_Rd1** data read on 8080 bus, without a new read operation on 8080 bus

7.1.5.16. TCON0_LVDS_IF_REG

Offset: 0x084			Register Name: TCON0 lvds panel interface register
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0	**TCON0_LVDS_En** 0: disable 1: enable
30	R/W	0	**TCON0_LVDS_Link_Sel** 0: single link 1: dual link
29	R/W	0	**TCON0_LVDS_Even_Odd_Dir** 0: normal 1: reverse
28	R/W	0	**TCON0_LVDS_Dir** 1: normal 2: reverse NOTE: LVDS direction

27	R/W	0	**TCON0_LVDS_Mode** 0: NS mode 1: JEIDA mode
26	R/W	0	**TCON0_LVDS_BitWidth** 0: 24bit 1: 18bit
25	R/W	0	**TCON0_LVDS_DeBug_En** 0: disable 1: enable
24	R/W	0	**TCON0_LVDS_DeBug_Mode** 0: mode0 1: mode1
23	R/W	0	**TCON0_LVDS_Correct_Mode** 0: mode0 1: mode1
22:21	/	/	/
20	R/W	0	**TCON0_LVDS_Clk_Sel** 0: MIPI PLL 1: TCON0 CLK
19:0	/	/	/

7.1.5.17. TCON0_IO_POL_REG

Offset: 0x088			Register Name: TCON0 IO polarity register
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0	**IO_Output_Sel** 0: normal output 1: register output when set as '1', d[23:0], io0, io1,io3 sync to dclk
30:28	R/W	0	**DCLK_Sel** 000: used DCLK0(normal phase offset) 001: used DCLK1(1/3 phase offset) 010: used DCLK2(2/3 phase offset) 101: DCLK0/2 phase 0 100: DCLK0/2 phase 90 reserved
27	R/W	0	**IO3_Inv** 0: not invert

			1: invert
26	R/W	0	**IO2_ Inv** 0: not invert 1: invert
25	R/W	0	**IO1_Inv** 0: not invert 1: invert
24	R/W	0	**IO0_Inv** 0: not invert 1: invert
23:0	R/W	0	**Data_Inv** TCON0 output port D[23:0] polarity control, with independent bit control: 0s: normal polarity 1s: invert the specify output

7.1.5.18. TCON0_IO_TRI_REG

Offset: 0x08C			Register Name: TCON0 IO control register
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	**/**
28	/	/	**RGB_Endian** 0: normal 1: bits_invert
27	R/W	1	**IO3_Output_Tri_En** 1: disable 0: enable
26	R/W	1	**IO2_Output_Tri_En** 1: disable 0: enable
25	R/W	1	**IO1_Output_Tri_En** 1: disable 0: enable
24	R/W	1	**IO0_Output_Tri_En** 1: disable 0: enable
23:0	R/W	0xFFFFFF	**Data_Output_Tri_En** TCON0 output port D[23:0] output enable, with independent bit

			control: 1s: disable 0s: enable

7.1.5.19. TCON1_CTL_REG

Offset: 0x090			Register Name: TCON1 control register
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0	**TCON1_En** 0: disable 1: enable
30:9	/	/	**/**
8:4	R/W	0	**Start_Delay** This is for DE1 and DE2
3:2	/	/	/
1:0	R/W	0	**TCON1_Src_Sel** 00: DE 0 01: DE 1 1x: BLUE data(FIFO2 disable, RGB=0000FF)

7.1.5.20. TCON1_BASIC0_REG

Offset: 0x094			Register Name: TCON1 basic timing register0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	**/**
27:16	R/W	0	**TCON1_XI** source width is X+1
15:12	/	/	/
11:0	R/W	0	**TCON1_YI** source height is Y+1

7.1.5.21. TCON1_BASIC1_REG

Offset: 0x098			Register Name: TCON1 basic timing register1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	**/**
27:16	R/W	0	**LS_XO** width is LS_XO+1
15:12	/	/	**/**
11:0	R/W	0	**LS_YO**

			width is LS_YO+1 NOTE: this version **LS_YO = TCON1_YI**

7.1.5.22. TCON1_BASIC2_REG

Offset: 0x09C			Register Name: TCON1 basic timing register2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	**/**
27:16	R/W	0	**TCON1_XO** width is TCON1_XO+1
15:12	/	/	**/**
11:0	R/W	0	**TCON1_YO** height is TCON1_YO+1

7.1.5.23. TCON1_BASIC3_REG

Offset: 0x0A0			Register Name: TCON1 basic timing register3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	**/**
28:16	R/W	0	**HT** horizontal total time Thcycle = (HT+1) * Thdclk
15:12	/	/	**/**
11:0	R/W	0	**HBP** horizontal back porch Thbp = (HBP +1) * Thdclk

7.1.5.24. TCON1_BASIC4_REG

Offset: 0x0A4			Register Name: TCON1 basic timing register4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	**/**
28:16	R/W	0	**VT** horizontal total time (in HD line) Tvt = VT/2 * Th
15:12	/	/	**/**
11:0	R/W	0	**VBP** horizontal back porch (in HD line) Tvbp = (VBP +1) * Th

7.1.5.25. TCON1_BASIC5_REG

Offset: 0x0A8			Register Name: TCON1 basic timing register5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	**/**
25:16	R/W	0	**HSPW** horizontal Sync Pulse Width (in dclk) Thspw = (HSPW+1) * Tdclk Note: HT> (HSPW+1)
15:10	/	/	**/**
9:0	R/W	0	**VSPW** vertical Sync Pulse Width (in lines) Tvspw = (VSPW+1) * Th Note: VT/2 > (VSPW+1)

7.1.5.26. TCON1_IO_POL_REG

Offset: 0x0F0			Register Name: TCON1 IO polarity register
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	**7.1.5.27. /**
27	R/W	0	**IO3_Inv** 0: not invert 1: invert
26	R/W	0	**IO2 Inv** 0: not invert 1: invert
25	R/W	0	**IO1_Inv** 0: not invert 1: invert
24	R/W	0	**IO0_Inv** 0: not invert 1: invert
23:0	R/W	0	**Data_Inv** TCON1 output port D[23:0] polarity control, with independent bit control: 0s: normal polarity 1s: invert the specify output

7.1.5.28. TCON1_IO_TRI_REG

Offset: 0x0F4			Register Name: TCON1 IO control register
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	**/**
27	R/W	1	**IO3_Output_Tri_En** 1: disable 0: enable
26	R/W	1	**IO2_Output_Tri_En** 1: disable 0: enable
25	R/W	1	**IO1_Output_Tri_En** 1: disable 0: enable
24	R/W	1	**IO0_Output_Tri_En** 1: disable 0: enable
27:0	R/W	0xFFFFFF	**Data_Output_Tri_En** TCON1 output port D[23:0] output enable, with independent bit control: 1s: disable 0s: enable

7.1.5.29. TCON_ECC_FIFO_REG

Offset: 0x0F8			Register Name: TCON ECC FIFO register
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	/	**ECC_FIFO_BIST_EN** 0: disable 1: enable
30	R/W	/	**ECC_FIFO_ERR_FLAG**
29:24	/	/	**/**
23:16	R/W	/	**ECC_FIFO_ERR_BITS**
15:9	/	/	**/**
8	R/W	/	**ECC_FIFO_BLANK_EN** 0: disable ecc function in blanking 1: enable ecc function in blanking ECC function is tent to trigged in blanking area at hv mode, set ‘1’ when in hv mode

7:0	R/W	/	**ECC_FIFO_SETTING** Note：bit3 0 enable，1 disable

7.1.5.30. TCON_CEU_CTL_REG

Offset: 0x100			Register Name: TCON CEU control register
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0	**CEU_en** 0: bypass 1: enable
30:0	/	/	**/**

7.1.5.31. TCON0_CPU_TRI0_REG

Offset: 0x160			Register Name: TCON0 cpu panel trigger register0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	**/**
27:16	R/W	0	**Block_Space** should be set >20*pixel_cycle
15:12	/	/	**/**
11:0	R/W	0	**Block_Size**

7.1.5.32. TCON0_CPU_TRI1_REG

Offset: 0x164			Register Name: TCON0 cpu panel trigger register1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R	0	**Block_Current_Num**
15:0	R/W	0	**Block_Num**

7.1.5.33. TCON0_CPU_TRI2_REG

Offset: 0x168			Register Name: TCON0 cpu panel trigger register2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x20	**Start_Delay** Tdly = (Start_Delay +1) * be_clk*8
15	R/W	0	**Trans_Start_Mode** 0: ecc_fifo+tri_fifo 1: tri_fifo
14:13	R/W	0	**Sync_Mode** 0x: auto

			10: 0 11: 1
12:0	R/W	0	**Trans_Start_Set**

7.1.5.34. TCON0_CPU_TRI3_REG

Offset: 0x16C			Register Name: TCON0 cpu panel trigger register3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R/W	0	**Tri_Int_Mode** 00: disable 01: counter mode 10: te rising mode 11: te falling mode when set as 01, Tri_Counter_Int occur in cycle of (Count_N+1)×(Count_M+1)×4 dclk. when set as 10 or 11, io0 is map as TE input.
27:24	/	/	/
23:8	R/W	0	**Counter_N**
7:0	R/W	0	**Counter_M**

7.1.5.35. TCON_CMAP_CTL_REG

Offset: 0x180			Register Name: TCON color map control register
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0	**Color_Map_En** 0: bypass 1: enable This module only work when X is divided by 4
30:1	/	/	**/**
0	R/W	0	**Out_Format** 0: 4 pixel output mode: Out0 -> Out1 -> Out2 -> Out3 1: 2 pixel output mode: Out0 -> Out1

7.1.5.36. TCON_CMAP_ODD0_REG

Offset: 0x190			Register Name: TCON color map odd register0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0	**Out_Odd1**
15:0	R/W	0	**Out_Odd0**

			bit15-12: Reservd bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0x0: in_b0 0x1: in_g0 0x2: in_r0 0x3: reservd 0x4: in_b1 0x5: in_g1 0x6: in_r1 0x7: reservd 0x8: in_b2 0x9: in_g2 0xa: in_r2 0xb: reservd 0xc: in_b3 0xd: in_g3 0xe: in_r3 0xf: reservd

7.1.5.37. TCON_CMAP_ODD1_REG

Offset: 0x194			Register Name: TCON color map odd register1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0	Out_Odd3
15:0	R/W	0	Out_Odd2

7.1.5.38. TCON_CMAP_EVEN0_REG

Offset: 0x198			Register Name: TCON color map even register0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0	Out_Even1
15:0	R/W	0	Out_Even0

7.1.5.39. TCON_CMAP_ EVEN1_REG

Offset: 0x19C			Register Name: TCON color map even register1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0	Out_Even3

15:0	R/W	0	Out_Even2

7.1.5.40. TCON_MUX_CTL_REG

Offset: 0x200			Register Name: TCON mux control register
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	**/**
9:8	R/W	0	**HDMI_OUTPUT_SRC** 0: LCDC0 TCON1 1: LCDC1 TCON1 1x: close(clock gate)
7:2	/	/	**/**
1:0	R/W	0	**MIPI_DSI_OUTPUT_SRC** 00: LCDC0 TCON0 01: LCDC1 TCON0 1x: close(clock gate)

7.1.6. CONTROL SIGNAL AND DATA PORT MAPPING

LCD IO PORT

I/F	Sync RGB Interface					CPU/I80						LVDS	
	Para RGB	Serial RGB			CCIR 656	Para RGB 666	Para RGB 565	Serial RGB 666		Serial RGB 565		Sing Link	Dual Link
Cycle		1st	2nd	3rd				1st	2nd	1st	2nd		
IO0	VSYNC					CS							
IO1	HSYNC					RD							
IO2	DCLK					WR							
IO3	DE					RS							
D23	B7					R5	R4						
D22	B6					R4	R3						
D21	B5					R3	R2						
D20	B4					R2	R1						
D19	B3					R1	R0					1-VN3	E-VN3
D18	B2					R0	G5					1-VP3	E-VP3

D17	B1											1-VNC	E-VNC
D16	B0											1-VPC	E-VPC
D15	G7					G5	G4					1-VN2	E-VN2
D14	G6					G4	G3					1-VP2	E-VP2
D13	G5					G3						1-VN1	E-VN1
D12	G4	D17	D27	D37	D7	G2	G2	R5	G2	R4	G2	1-VP1	E-VP1
D11	G3	D16	D26	D36	D6	G1	G1	R4	G1	R3	G1	1-VN0	E-VN0
D10	G2	D15	D25	D35	D5	G0	G0	R3	G0	R2	G0	1-VP0	E-VP0
D9	G1											0-VN3	O-VN3
D8	G0											0-VP3	O-VP3
D7	B7	D14	D24	D34	D4	B5	B4	R2	B5	R1	B4	0-VNC	O-VNC
D6	B6	D13	D23	D33	D3	B4	B3	R1	B4	R0	B3	0-VPC	O-VPC
D5	B5	D12	D22	D32	D2	B3	B2	R0	B3	G5	B2	0-VN2	O-VN2
D4	B4	D11	D21	D31	D1	B2	B1	G5	B2	G4	B1	0-VP2	O-VP2
D3	B3	D10	D20	D30	D0	B1	B0	G4	B1	G3	B0	0-VN1	O-VN1
D2	B2					B0		G3	B0			0-VP1	O-VP1
D1	B1											0-VN0	O-VN0
D0	B0											0-VP0	O-VP0

7.2. DEFE

7.2.1. OVERVIEW

The Display Engine FrontEnd (DEFE) performs image capture/driver, video/graphic scale, format conversion and color space conversion. It is composed of DMA controller, input controller, deinterlacing, scaler, color space conversion, post processing and output controller.

The DEFE features:

- Output scan type: interlace/progressive
- Input format: YUV444/YUV422/YUV420/YUV411/ARGB888/ARGB4444/RGB565 and ARGB1555
- Direct display output format: ARGB
- Write back output format: RGB/YUV444/YUV420/YUV422/YUV411
- 4 channel scaling pipelines for scaling up/down
- Programmable source image size from 8x4 to 8192x8192 resolution
- Programmable destination image size from 8x4 to 8192x8192 resolution
- 8 tap scale filter in horizontal and 4 tap in vertical direction
- 32 Programmable coefficients for each tap
- Color space conversion between YUV and RGB
- Output support directly display and write back to memory
- Input support from dram, DEBE and interface of lcd with DEBE
- De-interlace method: weave/bob/pixel-motion-adaptive/pixel-motion-adaptive bob
- Support full 1080P 3D format content input/output format convert/display(including HDMI)
- Support 2160P video display(input and output support 4096x2160 at the same time)

7.2.2. DEFE BLOCK DIAGRAM

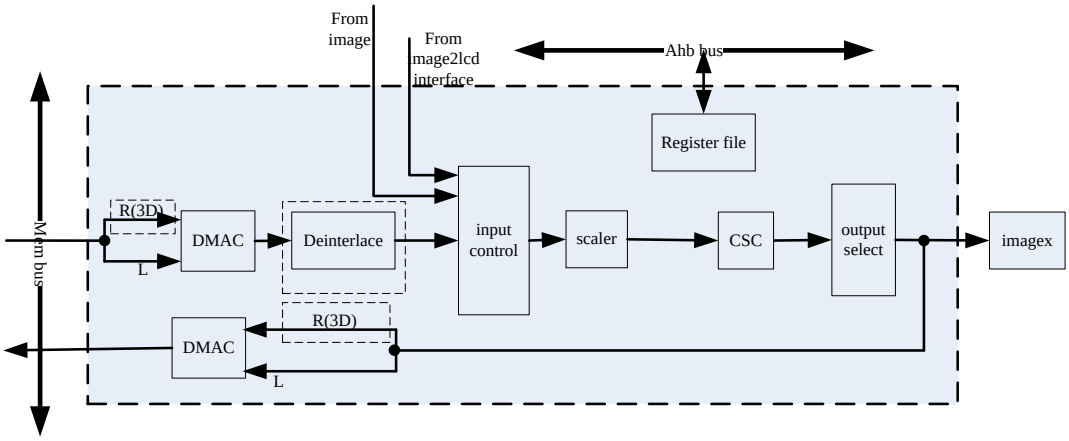


Figure 7-2 DEFE Block Diagram

7.2.3. DEFE DESCRIPTION

DEFE supports scaling or resizing of planar or interleaved video component data. Resizing, or scaling, the image means generating a new image that is larger or smaller than the original. The new image will have a larger or smaller number of pixels in the horizontal and/or vertical directions than the original image. And filtering provides image enhancement, scaler provides high quality, 8-tap filtering in horizontal and 4-tap in vertical, of YUV or RGB data.

7.2.3.1. RE-SAMPLING

Up-sampling is the process of inserting new data samples between original data samples to increase the sampling rate.

Down-sampling is the process of reducing the sampling rate by removing or throwing away original data samples.

In order to generate the output pixels, first need relate the output grid to the input grid. Scaling is a pixel transformation in which an array of output pixels is generated from an array of input pixels. The value of each pixel on the output pixel grid is calculated from the values of its adjacent pixels on the input grid. To find these adjacent pixels, need overlay the output grid on the input grid and align the starting pixels, X0Y0, of the two grids. To identify the adjacent input pixels for a given output pixel, you divide the output pixel X (pixel number along the output line) and Y (pixel line number within window) by their corresponding scaling factors:

Xout = Xin / (horizontal scaling factor)

where: horizontal scaling factor = input length / output length

Yout = Yin / (vertical scaling factor)

where: vertical scaling factor = input height / output height

Note that the resulting Xin and Yin values will be real numbers because the output pixels will usually fall

between the input pixels. The fractional portion indicates the fractional distance to the next pixel. To calculate the output pixel value, you use the value for the nearest pixel to the left and above and combine it with the value of the other adjacent pixel(s). For example, horizontal interpolation uses the starting pixel to the left interpolated with the next pixel to the right, with the fractional value used to determine the weighting for the interpolation.

7.2.3.2. INPUT DATA CHANNEL

DEFE supports planar or interleaved video component data inputting, there are 3 input channels in DEFE: channel0, channel1, channel2. In planar mode, if the U, V data are not combined, the channe0, 1, 2 refer to the Y, U, V data channel respectively, if the U, V data are combined, the channel0 refer to the Y channel, and the channel 1 refer to the U, V combined channel, and the channel2 will be inactive. In interleaved mode, the channel0 refer to UYVY (or VYUY, YUYV, or YVYU depending on the configuration), and the channel1 and channel2 will be inactive.

Notes: Interleaved YUV data, only YUV422 and YUV444 format is valid.

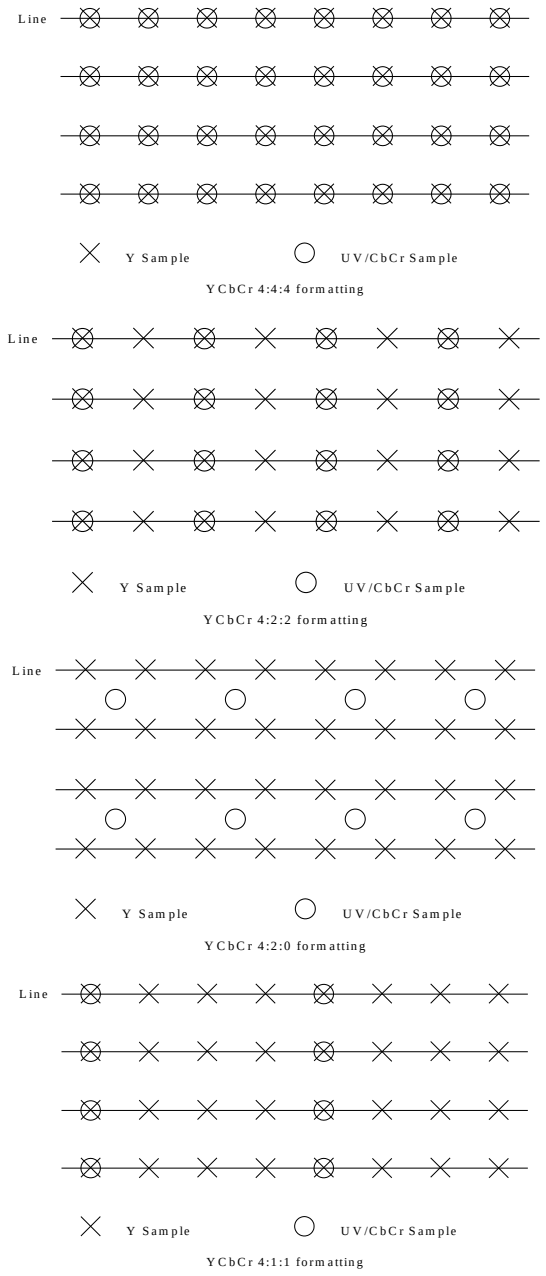
7.2.3.3. CSC (COLOR SPACE CONVERSION) DESCRIPTION

YUV / RGB conversion is used to generate an RGB version data of the image for display or RGB / YUV version data for write back to memory.

Conversion algorithm formula:

R = (R Y component coefficient * Y) + (R U component coefficient * U) + (R V component coefficient * V) + R constant	Y = (Y R component coefficient * R) + (Y G component coefficient * G) + (Y B component coefficient * B) + Y constant
G = (G Y component coefficient * Y) + (G U component coefficient * U) + (G V component coefficient * V) + G constant	U = (U R component coefficient * R) + (U G component coefficient * G) + (U B component coefficient * B) + U constant
B = (B Y component coefficient * Y) + (B U component coefficient * U) + (B V component coefficient * V) + B constant	V = (V R component coefficient * R) + (V G component coefficient * G) + (V B component coefficient * B) + V constant

7.2.3.4. DEFE SOURCE INPUT FORMATS



7.2.3.5. IMAGE DATA MEMORY MAPPING

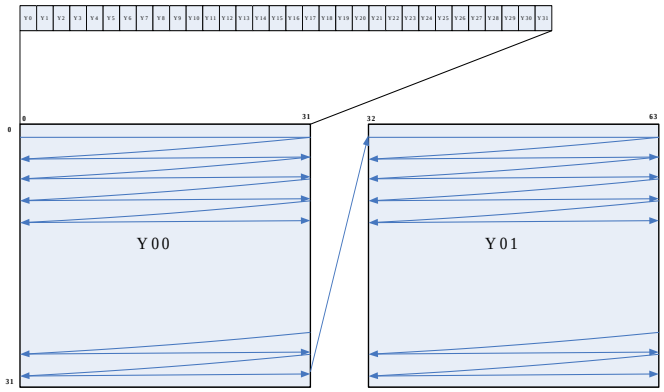
As for the DEFE, except the sequence non tile-based format input data is supported, the tile-based format input data is supported as well. The tile-based format data is valid for YUV422, YUV420 and YUV411 when input data mode is planar or UV combined mode.

Here is reference for the tile-based format memory mapping in different conditions.

TILE-BASED UV COMBINED MODE

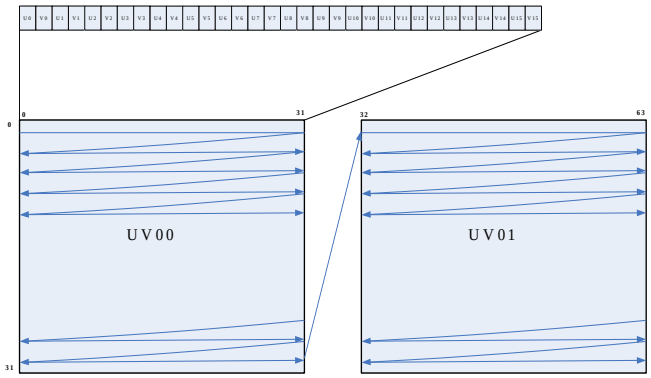
Y component mapping:

The mapping of Y component is the same in YUV422, YUV420 and YUV411.

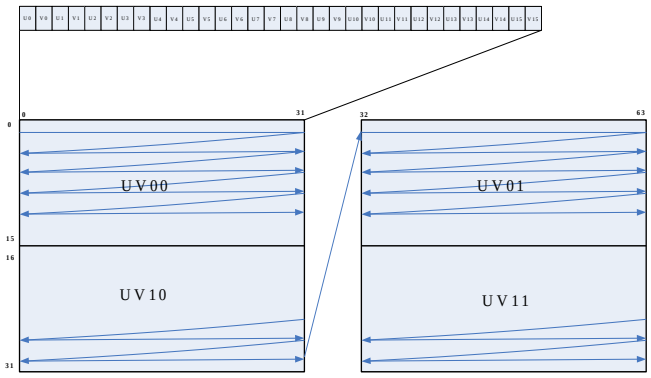


UV component mapping:

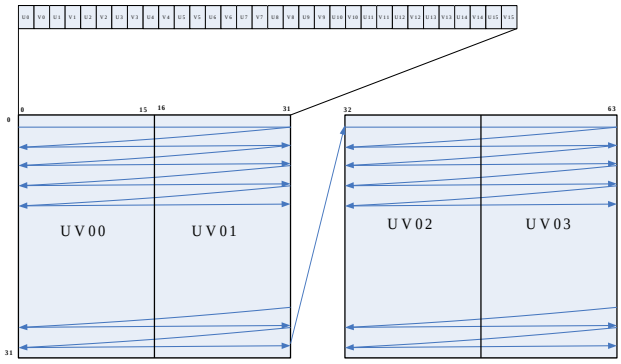
YUV422:



YUV420:



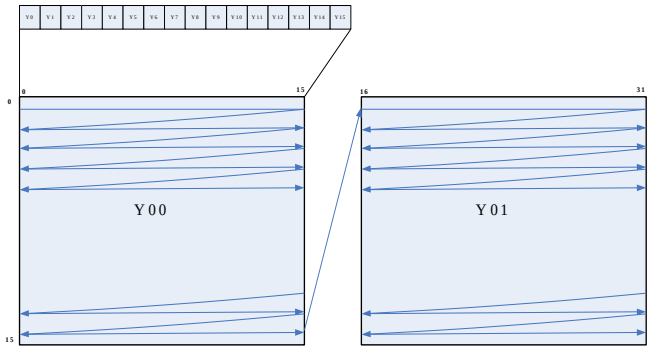
YUV411:



TILE-BASED PLANAR MODE:

Y component:

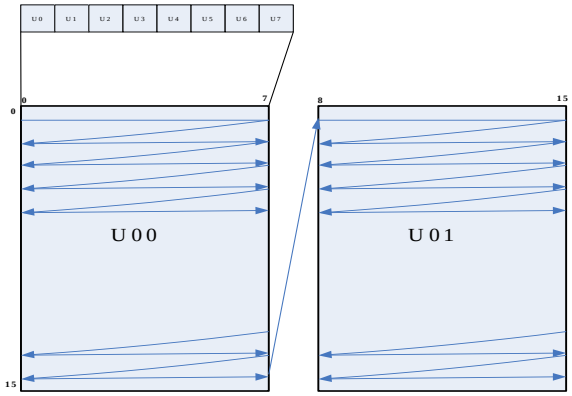
The mapping of Y component is the same in YUV422, YUV420 and YUV411.



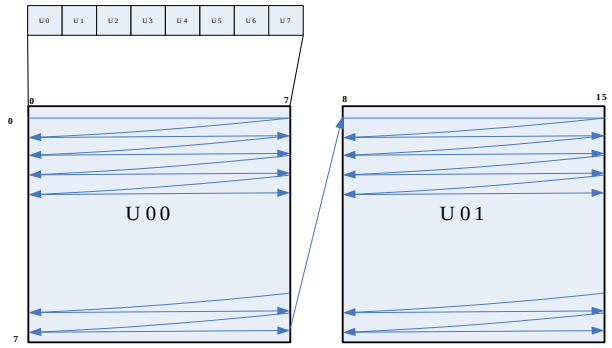
U or V component:

The mapping of V component is the same with U component.

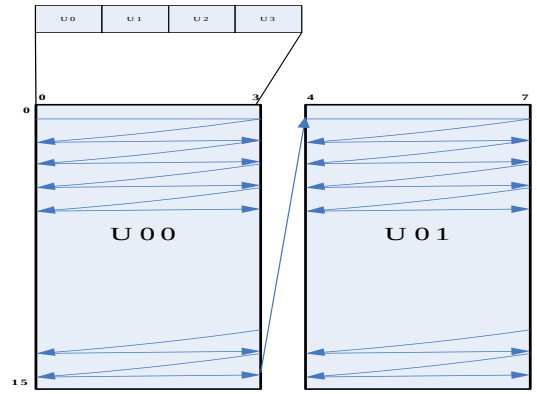
YUV422:



YUV420:

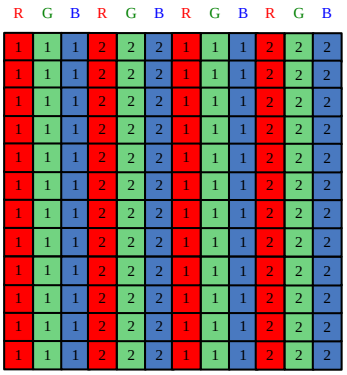


YUV411:

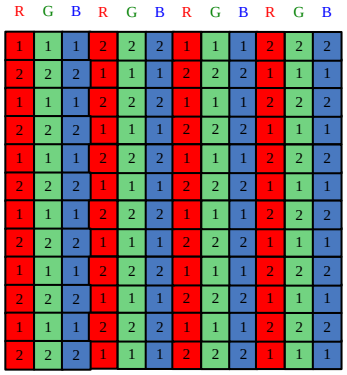


3D OUTPUT MODE

CI_1

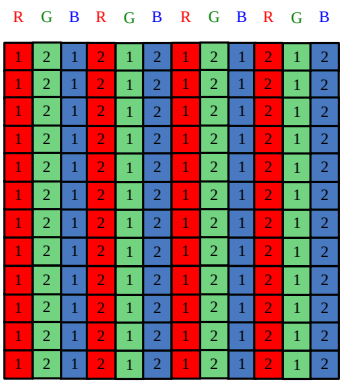


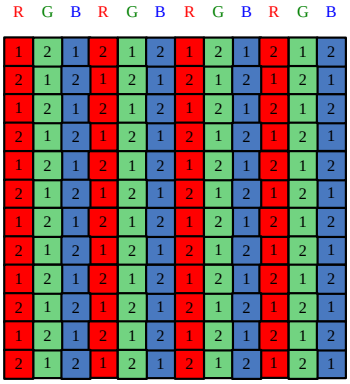
CI_2



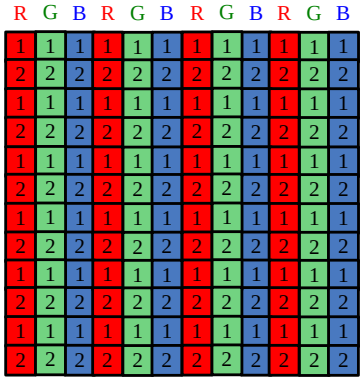
CI_3

CI_4





LIRGB



7.2.4. DEFE REGISTER LIST

Module Name	Base Address
DEFE0	0x01E00000
DEFE1	0x01E20000

Register Name	Offset	Description
DEFE_EN_REG	0x0000	DEFE Module Enable Register
DEFE_FRM_CTRL_REG	0x0004	DEFE Frame Process Control Register
DEFE_BYPASS_REG	0x0008	DEFE CSC By-Pass Register
DEFE_AGTH_SEL_REG	0x000C	DEFE Algorithm Selection Register
DEFE_LINT_CTRL_REG	0x0010	DEFE Line Interrupt Control Register
DEFE_3D_PRELUMA_REG	0x001C	DEFE 3D Pre-Luma Buffer Address Register
DEFE_BUF_ADDR0_REG	0x0020	DEFE Input Channel 0 Buffer Address Register
DEFE_BUF_ADDR1_REG	0x0024	DEFE Input Channel 1 Buffer Address Register
DEFE_BUF_ADDR1_REG	0x0028	DEFE Input Channel 2 Buffer Address Register

DEFE_FIELD_CTRL_REG	0x002C	DEFE Field Sequence Register
DEFE_TB_OFF0_REG	0x0030	DEFE Channel 0 Tile-Based Offset Register
DEFE_TB_OFF1_REG	0x0034	DEFE Channel 1 Tile-Based Offset Register
DEFE_TB_OFF2_REG	0x0038	DEFE Channel 2 Tile-Based Offset Register
DEFE_3D_PRECHROMA_REG	0x001C	DEFE 3D Pre-Chroma Buffer Address Register
DEFE_LINESTRD0_REG	0x0040	DEFE Channel 0 Line Stride Register
DEFE_LINESTRD1_REG	0x0044	DEFE Channel 1 Line Stride Register
DEFE_LINESTRD2_REG	0x0048	DEFE Channel 2 Line Stride Register
DEFE_INPUT_FMT_REG	0x004C	DEFE Input Format Register
DEFE_WB_ADDR0_REG	0x0050	DEFE Write Back Address0 Register
DEFE_WB_ADDR1_REG	0x0054	DEFE Write Back Address1 Register
DEFE_WB_ADDR2_REG	0x0058	DEFE Write Back Address2 Register
DEFE_OUTPUT_FMT_REG	0x005C	DEFE Output Format Register
DEFE_INT_EN_REG	0x0060	DEFE Interrupt Enable Register
DEFE_INT_STATUS_REG	0x0064	DEFE Interrupt Status Register
DEFE_STATUS_REG	0x0068	DEFE Status Register
DEFE_CSC_COEF00_REG	0x0070	DEFE CSC Coefficent 00 Register
DEFE_CSC_COEF01_REG	0x0074	DEFE CSC Coefficent 01 Register
DEFE_CSC_COEF02_REG	0x0078	DEFE CSC Coefficent 02 Register
DEFE_CSC_COEF03_REG	0x007C	DEFE CSC Coefficent 03 Register
DEFE_CSC_COEF10_REG	0x0080	DEFE CSC Coefficent 10 Register
DEFE_CSC_COEF11_REG	0x0084	DEFE CSC Coefficent 11 Register
DEFE_CSC_COEF12_REG	0x0088	DEFE CSC Coefficent 12 Register
DEFE_CSC_COEF13_REG	0x008C	DEFE CSC Coefficent 13 Register
DEFE_CSC_COEF20_REG	0x0090	DEFE CSC Coefficent 20 Register
DEFE_CSC_COEF21_REG	0x0094	DEFE CSC Coefficent 21 Register
DEFE_CSC_COEF22_REG	0x0098	DEFE CSC Coefficent 22 Register
DEFE_CSC_COEF23_REG	0x009C	DEFE CSC Coefficent 23 Register
DEFE_DI_CTRL_REG	0x00A0	DEFE De-interlacing Control Register
DEFE_DI_DIAGINTP_REG	0x00A4	DEFE De-interlacing Diag-Interpolate Register
DEFE_DI_TEMPDIFF_REG	0x00A8	DEFE De-interlacing Temp-Difference Register
DEFE_DI_LUMA_TH_REG	0x00AC	DEFE De-interlaing Luma Motion Threshold Register
DEFE_DI_SPATCOMP_REG	0x00B0	DEFE De-interlacing Spatial Compare Register
DEFE_DI_CHROMADIFF_REG	0x00B4	DEFE De-interlacing Chroma Diff Register
DEFE_DI_PRELUMA_REG	0x00B8	DEFE De-interlacing Pre-Frame Luma Address Register

DEFE_DI_ PRECHROMA _REG	0x00BC	DEFE De-interlacing Pre-Frame Chroma Address Register
DEFE_DI_TILEFLAG0_REG	0x00C0	DEFE De-interlacing Tile Flag0 Address Register
DEFE_DI_TILEFLAG1_REG	0x00C4	DEFE De-interlacing Tile Flag1 Address Register
DEFE_DI_FLAGLINESTRD_REG	0x00C8	DEFE De-interlacing Tile Flag LineStride Register
DEFE_DI_FLAG_SEQ_REG	0x00CC	DEFE De-interlacing Flag Sequence Register
DEFE_WB_LINESTRD_EN_REG	0x00D0	DEFE Write Back Line Stride Enable Register
DEFE_WB_LINESTRD0_REG	0x00D4	DEFE Write Back Channel 3 Line Stride Register
DEFE_WB_LINESTRD1_REG	0x00D8	DEFE Write Back Channel 4 Line Stride Register
DEFE_WB_LINESTRD2_REG	0x00DC	DEFE Write Back Channel 5 Line Stride Register
DEFE_3D_CTRL_REG	0x00E0	DEFE 3D Mode Control Register
DEFE_3D_BUF_ADDR0_REG	0x00E4	DEFE 3D Channel 0 Buffer Address Register
DEFE_3D_BUF_ADDR1_REG	0x00E8	DEFE 3D Channel 1 Buffer Address Register
DEFE_3D_BUF_ADDR2_REG	0x00EC	DEFE 3D Channel 2 Buffer Address Register
DEFE_3D_TB_OFF0_REG	0x00F0	DEFE 3D Channel 0 Tile-Based Offset Register
DEFE_3D_TB_OFF1_REG	0x00F4	DEFE 3D Channel 1 Tile-Based Offset Register
DEFE_3D_TB_OFF2_REG	0x00F8	DEFE 3D Channel 2 Tile-Based Offset Register
DEFE_3D_WB_LINESTRD_REG	0x00FC	DEFE 3D Write Back Line-Stride Register
DEFE_CH0_INSIZE_REG	0x0100	DEFE Channel 0 Input Size Register
DEFE_CH0_OUTSIZE_REG	0x0104	DEFE Channel 0 Output Size Register
DEFE_CH0_HORZFACT_REG	0x0108	DEFE Channel 0 Horizontal Factor Register
DEFE_CH0_VERTFACT_REG	0x010C	DEFE Channel 0 Vertical factor Register
DEFE_CH0_HORZPHASE_REG	0x0110	DEFE Channel 0 Horizontal Initial Phase Register
DEFE_CH0_VERTPHASE0_REG	0x0114	DEFE Channel 0 Vertical Initial Phase 0 Register
DEFE_CH0_VERTPHASE1_REG	0x0118	DEFE Channel 0 Vertical Initial Phase 1 Register
DEFE_CH0_HORZTAP0_REG	0x0120	DEFE Channel 0 Horizontal Tap Offset 0 Register
DEFE_CH0_HORZTAP1_REG	0x0124	DEFE Channel 0 Horizontal Tap Offset 1 Register
DEFE_CH0_VERTTAP_REG	0x0128	DEFE Channel 0 Vertical Tap Offset Register
DEFE_CH1_INSIZE_REG	0x0200	DEFE Channel 1 Input Size Register
DEFE_CH1_OUTSIZE_REG	0x0204	DEFE Channel 1 Output Size Register
DEFE_CH1_HORZFACT_REG	0x0208	DEFE Channel 1 Horizontal Factor Register
DEFE_CH1_VERTFACT_REG	0x020C	DEFE Channel 1 Vertical factor Register
DEFE_CH1_HORZPHASE_REG	0x0210	DEFE Channel 1 Horizontal Initial Phase Register
DEFE_CH1_VERTPHASE0_REG	0x0214	DEFE Channel 1 Vertical Initial Phase 0 Register
DEFE_CH1_VERTPHASE1_REG	0x0218	DEFE Channel 1 Vertical Initial Phase 1 Register
DEFE_CH1_HORZTAP0_REG	0x0220	DEFE Channel 1 Horizontal Tap Offset 0 Register
DEFE_CH1_HORZTAP1_REG	0x0224	DEFE Channel 1 Horizontal Tap Offset 1 Register

DEFE_CH1_VERTTAP_REG	0x0228	DEFE Channel 1 Vertical Tap Offset Register
DEFE_CH0_HORZCOEF0_REGN	0x0400+N*4	DEFE Channel 0 Horizontal Filter Coefficient Register (N=0:31)
DEFE_CH0_HORZCOEF1_REGN	0x0480+N*4	DEFE Channel 0 Horizontal Filter Coefficient Register (N=0:31)
DEFE_CH0_VERTCOEF_REGN	0x0500+N*4	DEFE Channel 0 Vertical Filter Coeffient Register (N=0:31)
DEFE_CH1_HORZCOEF0_REGN	0x0600+N*4	DEFE Channel 1 Horizontal Filter Coeffient Register(N=0:31)
DEFE_CH1_HORZCOEF1_REGN	0x0680+N*4	DEFE Channel 1 Horizontal Filter Coeffient Register (N=0:31)
DEFE_CH1_VERTCOEF_REGN	0x0700+N*4	DEFE Channel 1 Vertical Filter Coeffient Register (N=0:31)
DEFE_CH3_HORZCOEF0_REGN	0x0800+N*4	DEFE Channel 3 Horizontal Filter Coefficient Register (N=0:31)
DEFE_CH3_HORZCOEF1_REGN	0x0880+N*4	DEFE Channel 3 Horizontal Filter Coefficient Register (N=0:31)
DEFE_CH3_VERTCOEF_REGN	0x0900+N*4	DEFE Channel 3 Vertical Filter Coeffient Register (N=0:31)

7.2.5. DEFE REGISTER DESCRIPTION

7.2.5.1. DEFE_EN_REG

Offset: 0x0			Register Name: DEFE_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	EN DEFE enable 0: Disable 1: Enable When DEFE enable bit is disabled, the clock of DEFE module will be disabled If this bit transitions from 0 to 1, the frame process control register and the interrupt enable register will be initialed to default value, and the state machine of the module is reset

7.2.5.2. DEFE_FRM_CTRL_REG

Offset: 0x4			Register Name: DEFE_FRM_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	FRM_START Frame start & reset control 0: reset 1: start If the bit is written to zero, the whole state machine and data paths of DEFE module will be reset. When the bit is written to 1, DEFE will start a new frame process.
15	/	/	/
14:12	R/W	0x0	IN_CTRL DEFE input source control 000: from dram 100: from DEBE0 interface of DEBE2lcd (don't influence the interface timing of DEBE) 101: from DEBE1 interface of DEBE2lcd(don't influence the interface timing of DEBE) 110: from DEBE0(influence the interface timing of DEBE) 111: from DEBE1(influence the interface timing of DEBE) Other: reserved
11	R/W	0x0	OUT_CTRL DEFE output control 0: enable DEFE output to DEBE 1: disable DEFE output to DEBE If DEFE write back function is enabled, DEFE output to DEBE isn't recommended.
10	/	/	/
9:8	R/W	0x0	OUT_PORT_SEL DEFE output port select 00: DEBE0 01: DEBE1 other: reserved
7:3	/	/	/
2	R/W	0x0	WB_EN

			Write back enable 0: Disable 1: Enable If output to DEBE is enabled, the writing back process will start when write back enable bit is set and a new frame processing begins. The bit will be self-cleared when writing-back frame process starts.
1	R/W	0x0	COEF_RDY_EN Filter coefficients ready enable 0: not ready 1: filter coefficients configuration ready In order to avoid the noise, you have to ensure the same set filter coefficients are used in one frame, so the filter coefficients are buffered, the programmer can change the coefficients in any time. When the filter coefficients setting is finished, the programmer should set the bit if the programmer need the new coefficients in next scaling frame. When the new frame start, the bit will be self-cleared.
0	R/W	0x0	REG_RDY_EN Register ready enable 0: not ready 1: registers configuration ready As same as filter coefficients configuration, in order to ensure the display be correct, the correlative display configuration registers are buffered too, the programmer also can change the value of correlative registers in any time. When the registers setting is finished, the programmer should set the bit if the programmer need the new configuration in next scaling frame. When the new frame start, the bit will also be self-cleared.

7.2.5.3. DEFE_BYPASS_REG

Offset: 0x8			Register Name: DEFE_BYPASS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x0	SRAM_MAP_SEL Internal sram mapping select

			0: normal mode, in/out maximum width 1920 for all input formats 1: in/out maximum width 4096 only for input yuv420 2: in/out maximum width 2560 for all input format 3: reserved These bits are valid only when deinterlaceing function closed, and source comes from dram. 3D column mode is valid only in normal mode.
29:2	/	/	/
1	R/W	0x0	CSC_BYPASS_EN CSC by-pass enable 0: CSC enable 1: CSC will be by-passed Actually, in order to ensure the module working be correct, this bit only can be set when input data format is the same as output data format (both YUV or both RGB)
0	/	/	/

7.2.5.4. DEFE_AGTH_SEL_REG

Offset: 0xC			Register Name: DEFE_AGTH_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	LINEBUF_AGTH DEFE line buffer algorithm select 0: horizontal filtered result 1: original data
7:0	/	/	/

7.2.5.5. DEFE_LINT_CTRL_REG

Offset: 0x10			Register Name: DEFE_LINT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R	0x0	CURRENT_LINE
15	R/W	0x0	FIELD_SEL Field select 0: each field 1: end field(field counter in reg0x2c)

14:13	/	/	/
12:0	R/W	0x0	TRIG_LINE Trigger line number of line interrupt

7.2.5.6. DEFE_3D_PRELUMA_REG

Offset: 0x1C			Register Name: DEFE_3D_PRELUMA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	PREFRM_ADDR Pre-frame buffer address of luma for 3D right image.

7.2.5.7. DEFE_BUF_ADDR0_REG

Offset: 0x20			Register Name: DEFE_BUF_ADDR0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	BUF_ADDR DEFE frame buffer address In tile-based type: The address is the start address of the line in the first tile used to generating output frame. In non-tile-based type: The address is the start address of the first line.

7.2.5.8. DEFE_BUF_ADDR1_REG

Offset: 0x24			Register Name: DEFE_BUF_ADDR1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	BUF_ADDR DEFE frame buffer address In tile-based type: The address is the start address of the line in the first tile used to generating output frame. In non-tile-based type: The address is the start address of the first line.

7.2.5.9. DEFE_BUF_ADDR2_REG

Offset: 0x28	Register Name: DEFE_BUF_ADDR2_REG

Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	BUF_ADDR DEFE frame buffer address In tile-based type: The address is the start address of the line in the first tile used to generating output frame. In non-tile-based type: The address is the start address of the first line.

7.2.5.10. DEFE_FIELD_CTRL_REG

Offset: 0x2C			Register Name: DEFE_FIELD_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:24	R/W	0x20	FIR_OFFSET FIR compute initial value
23:13	/	/	/
12	R/W	0x0	FIELD_LOOP_MOD Field loop mode 0：the last field； 1：the full frame
11	/	/	/
10:8	R/W	0x0	VALID_FIELD_CNT Valid field counter bit the valid value = this value + 1；
7:0	R/W	0x0	FIELD_CNT Field counter each bit specify a field to display，0：top field，1：bottom field

7.2.5.11. DEFE_TB_OFF0_REG

Offset: 0x30			Register Name: DEFE_TB_OFF0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x0	X_OFFSET1 The x offset of the bottom-right point in the end tile
15:13	/	/	/
12:8	R/W	0x0	Y_OFFSET0

			The y offset of the top-left point in the first tile
7:5	/	/	/
4:0	R/W	0x0	X_OFFSET0 The x offset of the top-left point in the first tile

7.2.5.12. DEFE_TB_OFF1_REG

Offset: 0x34			Register Name: DEFE_TB_OFF1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x0	X_OFFSET1 The x offset of the bottom-right point in the end tile
15:13	/	/	/
12:8	R/W	0x0	Y_OFFSET0 The y offset of the top-left point in the first tile
7:5	/	/	/
4:0	R/W	0x0	X_OFFSET0 The x offset of the top-left point in the first tile

7.2.5.13. DEFE_TB_OFF2_REG

Offset: 0x38			Register Name: DEFE_TB_OFF2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x0	X_OFFSET1 The x offset of the bottom-right point in the end tile
15:13	/	/	/
12:8	R/W	0x0	Y_OFFSET0 The y offset of the top-left point in the first tile
7:5	/	/	/
4:0	R/W	0x0	X_OFFSET0 The x offset of the top-left point in the first tile

7.2.5.14. DEFE_3D_PRECHROMA_REG

Offset: 0x3C			Register Name: DEFE_3D_PRECHROMA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	PREFRM_ADDR Pre-frame buffer address of chroma for 3D right image.

7.2.5.15. DEFE_LINESTRD0_REG

Offset: 0x40			Register Name: DEFE_LINESTRD0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LINE_STRIDE **In tile-based type** The stride length is the distance from the start of the end line in one tile to the start of the first line in next tile(here next tile is in vertical direction) **In non-tile-based type** The stride length is the distance from the start of one line to the start of the next line.

7.2.5.16. DEFE_LINESTRD1_REG

Offset: 0x44			Register Name: DEFE_LINESTRD1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LINE_STRIDE **In tile-based type** The stride length is the distance from the start of the end line in one tile to the start of the first line in next tile(here next tile is in vertical direction) **In non-tile-based type** The stride length is the distance from the start of one line to the start of the next line.

7.2.5.17. DEFE_LINESTRD2_REG

Offset: 0x48			Register Name: DEFE_LINESTRD2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LINE_STRIDE **In tile-based type** The stride length is the distance from the start of the end line in one tile to the start of the first line in next tile(here next tile is in vertical direction) **In non-tile-based type** The stride length is the distance from the start of one line to the

			start of the next line.

7.2.5.18. DEFE_INPUT_FMT_REG

Offset: 0x4C			Register Name: DEFE_INPUT_FMT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	BYTE_SEQ Input data byte sequence selection 0: P3P2P1P0(word) 1: P0P1P2P3(word)
15	/	/	/
14	R/W	0x0	A_COEF_SEL Alpha fir coefficient select 0: the same with channel 0(G or Y) 1: the individe coeficients
13	/	/	/
12	R/W	0x0	SCAN_MOD Scanning Mode selection 0: non-interlace 1: interlace
11	/	/	/
10:8	R/W	0x0	DATA_MOD Input data mode selection 000: non-tile-based planar data 001: interleaved data 010: non-tile-based UV combined data 100: tile-based planar data 110: tile-based UV combined data other: reserved
7	/	/	/
6:4	R/W	0x0	DATA_FMT Input component data format **In non-tile-based planar data mode:** 000: YUV 4:4:4 001: YUV 4:2:2 010: YUV 4:2:0 011: YUV 4:1:1

			101: RGB888 Other: Reserved **In interleaved data mode:** 000: YUV 4:4:4 001: YUV 4:2:2 100: RGB565 101: ARGB8888 110: ARGB4444 111: ARGB1555 Other: reserved **In non-tile-based UV combined data mode:** 001: YUV 4:2:2 010: YUV 4:2:0 011: YUV 4:1:1 Other: reserved **In tile-based planar data mode:** 001: YUV 4:2:2 010: YUV 4:2:0 011: YUV 4:1:1 Other: Reserved **In tile-based UV combined data mode:** 001: YUV 4:2:2 010: YUV 4:2:0 011: YUV 4:1:1 Other: reserved
3:2	/	/	/
1:0	R/W	0x0	DATA_PS Pixel sequence **In interleaved YUV422 data mode:** 00: Y1V0Y0U0 01: V0Y1U0Y0 10: Y1U0Y0V0 11: U0Y1V0Y0

			In interleaved YUV444 data mode: 00: VUYA 01: AYUV Other: reserved **In UV combined data mode: (UV component)** 00: V1U1V0U0 01: U1V1U0V0 Other: reserved **In interleaved ARGB8888 data mode:** 00: BGRA 01: ARGB Other: reserved **In interleaved RGB565 data mode:** 00:RGB565 01:BGR565 Other: reserved **In interleaved ARGB4444 data mode:** 00: ARGB4444 01: BGRA4444 Other: reserved **In interleaved ARGB1555 data mode:** 00: ARGB1555 01: BGRA5551 Other: reserved

7.2.5.19. DEFE_WB_ADDR0_REG

Offset: 0x50			**Register Name: DEFE_WB_ADDR0_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	WB_ADDR Write-back address setting for output data.

7.2.5.20. DEFE_WB_ADDR1_REG

Offset: 0x54	**Register Name: DEFE_WB_ADDR1_REG**

Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	WB_ADDR Write-back address setting for output data.

7.2.5.21. DEFE_WB_ADDR2_REG

Offset: 0x58			Register Name: DEFE_WB_ADDR2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	WB_ADDR Write-back address setting for output data.

7.2.5.22. DEFE_OUTPUT_FMT_REG

Offset: 0x5C			Register Name: DEFE_OUTPUT_FMT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	BYTE_SEQ Output data byte sequence selection 0: P3P2P1P0(word) 1: P0P1P2P3(word) For ARGB, when this bit is 0, the byte sequence is BGRA, and when this bit is 1, the byte sequence is ARGB;
7	R/W	0x0	ALPHA_EN Output alpha enable 0: disable, output alpha value = 0xff 1: enable
6:5	/	/	/
4	R/W	0x0	SCAN_MOD Output interlace enable 0: disable 1: enable When output interlace enable, scaler selects YUV initial phase according to LCD field signal
3	/	/	/
2:0	R/W	0x0	DATA_FMT Data format 000: planar RGB888 conversion data format 001: interleaved BGRA8888 conversion data format 010: interleaved ARGB8888 conversion data format

			100: planar YUV 444 101: planar YUV 420(only support YUV input and not interleaved mode) 110: planar YUV 422(only support YUV input) 111: planar YUV 411(only support YUV input) Other: reserved

7.2.5.23. DEFE_INT_EN_REG

Offset: 0x60			Register Name: DEFE_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10	R/W	0x0	REG_LOAD_EN Register ready load interrupt enable
9	R/W	0x0	LINE_EN Line interrupt enable
8	/	/	/
7	R/W	0x0	WB_EN Write-back end interrupt enable 0: Disable 1: Enable
6:0	/	/	/

7.2.5.24. DEFE_INT_STATUS_REG

Offset: 0x64			Register Name: DEFE_INT_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10	R/W	0x0	REG_LOAD_STATUS Register ready load interrupt status
9	R/W	0x0	LINE_STATUS Line interrupt status
8	/	/	/
7	R/W	0x0	WB_STATUS Write-back end interrupt status
6:0	/	/	/

7.2.5.25. DEFE_STATUS_REG

Offset: 0x68	Register Name: DEFE_STATUS_REG

Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R	0x0	LINE_ON_SYNC Line number(when sync reached)
15	R/W	0x0	WB_ERR_SYNC Sync reach flag when capture in process
14	R/W	0x0	WB_ERR_LOSEDATA Lose data flag when capture in process
13	/	/	/
12	R	0x0	WB_ERR_STATUS write-back error status 0: valid write back 1: un-valid write back This bit is cleared through write 0 to reset/start bit in frame control register
11:6	/	/	/
5	R	0x0	LCD_FIELD LCD field status 0: top field 1: bottom field
4	R	0x0	DRAM_STATUS Access dram status 0: idle 1: busy This flag indicates whether DEFE is accessing dram
3	/	/	/
2	R	0x0	CFG_PENDING Register configuration pending 0: no pending 1: configuration pending This bit indicates the registers for the next frame has been configured. This bit will be set when configuration ready bit is set and this bit will be cleared when a new frame process begin.
1	R	0x0	WB_STATUS Write-back process status 0: write-back end or write-back disable 1: write-back in process

			This flag indicates that a full frame has not been written back to memory. The bit will be set when write-back enable bit is set, and be cleared when write-back process end.
0	R	0x0	FRM_BUSY Frame busy. This flag indicates that the frame is being processed. The bit will be set when frame process reset & start is set, and be cleared when frame process reset or disabled.

7.2.5.26. DEFE_CSC_COEF00_REG

Offset: 0x70			Register Name: DEFE_CSC_COEF00_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	COEF the Y/G coefficient the value equals to coefficient*2^{10}

7.2.5.27. DEFE_CSC_COEF01_REG

Offset: 0x74			Register Name: DEFE_CSC_COEF01_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	COEF the Y/G coefficient the value equals to coefficient*2^{10}

7.2.5.28. DEFE_CSC_COEF02_REG

Offset: 0x78			Register Name: DEFE_CSC_COEF02_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	COEF the Y/G coefficient the value equals to coefficient*2^{10}

7.2.5.29. DEFE_CSC_COEF03_REG

Offset: 0x7C	Register Name: DEFE_CSC_COEF03_REG

Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0x0	CONT the Y/G constant the value equals to coefficient*2^4

7.2.5.30. DEFE_CSC_COEF10_REG

Offset: 0x80			Register Name: DEFE_CSC_COEF10_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	COEF the U/R coefficient the value equals to coefficient*2^{10}

7.2.5.31. DEFE_CSC_COEF11_REG

Offset: 0x84			Register Name: DEFE_CSC_COEF11_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	COEF the U/R coefficient the value equals to coefficient*2^{10}

7.2.5.32. DEFE_CSC_COEF12_REG

Offset: 0x88			Register Name: DEFE_CSC_COEF12_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	COEF the U/R coefficient the value equals to coefficient*2^{10}

7.2.5.33. DEFE_CSC_COEF13_REG

Offset: 0x8C			Register Name: DEFE_CSC_COEF13_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:00	R/W	0x0	CONT the U/R constant the value equals to coefficient*2^4

7.2.5.34. DEFE_CSC_COEF20_REG

Offset: 0x90			Register Name: DEFE_CSC_COEF20_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	COEF the V/B coefficient the value equals to coefficient*2^{10}

7.2.5.35. DEFE_CSC_COEF21_REG

Offset: 0x94			Register Name: DEFE_CSC_COEF21_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	COEF the V/B coefficient the value equals to coefficient*2^{10}

7.2.5.36. DEFE_CSC_COEF22_REG

Offset: 0x98			Register Name: DEFE_CSC_COEF22_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	COEF the V/B coefficient the value equals to coefficient*2^{10}

7.2.5.37. DEFE_CSC_COEF23_REG

Offset: 0x9C			Register Name: DEFE_CSC_COEF23_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:00	R/W	0x0	CONT the V/B constant the value equals to coefficient*2^{4}

7.2.5.38. DEFE_DI_CTRL_REG

Offset: 0xA0			Register Name: DEFE_DI_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/

25	R/W	0x0	TEMPDIFF_EN Temporal difference compare enable 0: disable 1: enable
24	R/W	0x0	DIAGINTP_EN De-interlacing diagonal interpolate enable 0: disable 1: enable
23:18	/	/	/
17:16	R/W	0x0	MOD De-interlacing mode select 00: weave 01: bob 10: reserverd 11: pixel-motion-adaptive
15:9	/	/	/
8	R/W	0x0	FLAG_OUT_EN 0: deinterlace flag out enable 1: deinterlace flag out disable
7:1	/	/	/
0	R/W	0x0	EN De-interlacing enable 0: de-interlacing disable 1: de-interlacing enable

7.2.5.39. DEFE_DI_DIAGINTP_REG

Offset: 0xA4			Register Name: DEFE_DI_DIAGINTP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x8	TH3 Diagintp_th3
23:15	/	/	/
14:8	R/W	0x5	TH1 Diagintp_th1
7	/	/	/
6:0	R/W	0x28	TH0 Diagintp_th0

7.2.5.40. DEFE_DI_TEMPDIFF_REG

Offset: 0xA8			Register Name: DEFE_DI_TEMPDIFF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:16	R/W	0xF	DIRECT_DITHER_TH
15	/	/	/
14:8	R/W	0xA	AMBIGUITY_TH
7	/	/	/
6:0	R/W	0xA	SAD_CENTRAL_TH

7.2.5.41. DEFE_DI_LUMA_TH_REG

Offset: 0xAC			Register Name: DEFE_DI_LUMA_TH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x3	Pixel_Static_TH
23:16	R/W	0x6	AvgLumaShifter
15:8	R/W	0x10	MaxLumaTh
7:0	R/W	0x9	MinLumaTh

7.2.5.42. DEFE_DI_SPATCOMP_REG

Offset: 0xB0			Register Name: DEFE_DI_SPATCOMP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x14	TH3 spatial_th3
15:8	/	/	/
7:0	R/W	0xA	TH2 spatial_th2

7.2.5.43. DEFE_DI_CHROMADIFF_REG

Offset: 0xB4			Register Name: DEFE_DI_CHROMADIFF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:24	R/W	0x1F	CHROMA Chroma burst length
23:22	/	/	/
21:16	R/W	0x1F	LUMA

			Luma burst length
15:8	/	/	/
7:0	R/W	0x5	CHROMA_DIFF_TH

7.2.5.44. DEFE_DI_PRELUMA_REG

Offset: 0xB8			Register Name: DEFE_DI_PRELUMA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	PREFRM_ADDR Pre-frame buffer address of luma

7.2.5.45. DEFE_DI_PRECHROMA_REG

Offset: 0xBC			Register Name: DEFE_DI_ PRECHROMA _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	PREFRM_ADDR Pre-frame buffer address of chroma

7.2.5.46. DEFE_DI_TILEFLAG0_REG

Offset: 0xC0			Register Name: DEFE_DI_TILEFLAG0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TILE_FLAG_ADDR0 Current frame tile flag buffer address

7.2.5.47. DEFE_DI_TILEFLAG1_REG

Offset: 0xC4			Register Name: DEFE_DI_TILEFLAG1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TILE_FLAG_ADDR1 Current frame tile flag buffer address

7.2.5.48. DEFE_DI_FLAGLINESTRD_REG

Offset: 0xC8			Register Name: DEFE_DI_FLAGLINESTRD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x200	TILE_FLAG_LINESTRD tile flag line-stride

7.2.5.49. DEFE_DI_ FLAG_SEQ_REG

Offset: 0xCC	Register Name: DEFE_DI_SEQ_REG

Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	FIELD_LOOP_MOD Field loop mode for deinterlace flag 0：the last field； 1：the full frame
11	/	/	/
10:8	R/W	0x0	VALID_FIELD_CNT Valid field counter bit for deinterlace flag the valid value = this value + 1；
7:0	R/W	0x0	FIELD_CNT Field counter for deinterlace flag each bit specify a field to display，0：flag0，1：flag1

7.2.5.50. DEFE_WB_LINESTRD_EN_REG

Offset: 0xD0			Register Name: DEFE_WB_LINESTRD_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	EN Write back line-stride enable 0: disable 1: enable

7.2.5.51. DEFE_WB_LINESTRD0_REG

Offset: 0xD4			Register Name: DEFE_WB_LINESTRD0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LINE_STRD Ch3 write back line-stride

7.2.5.52. DEFE_WB_LINESTRD1_REG

Offset: 0xD8			Register Name: DEFE_WB_LINESTRD1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LINE_STRD Ch4 write back line-stride

7.2.5.53. DEFE_WB_LINESTRD2_REG

Offset: 0xDC			Register Name: DEFE_WB_LINESTRD2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:0	R/W	0x0	LINE_STRD Ch5 write back line-stride

7.2.5.54. DEFE_3D_CTRL_REG

Offset: 0xE0			Register Name: DEFE_3D_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	TB_OUT_MOD_FIELD Top/bottom output mode field number 0: left or left 1st field(determined by reg0x2c) 1: right or right 1st field 2: left 2nd field 3: right 2nd field
23:19	/	/	/
18:16	R/W	0x0	CI_OUT_MOD 3D column interleaved mode 0: CI_1 1: CI_2 2: CI_3 3: CI_4 Other: reserved
15:13	/	/	/
12	R/W	0x0	TB_OUT_SCAN_MOD Output top/bottom scan mode selection 0: progressive 1: interlace
11	R/W	0x0	LI_IN_EN 3D input line interleaved enable
10	R/W	0x0	SS_OUT_EN 3D output side by side mode enable
9	/	/	/
8	R/W	0x0	CI_OUT_EN 3D Column interleaved mode output enable
7:2	/	/	/
1:0	R/W	0x0	MOD_SEL 3D mode select 00: normal output mode(2D mode)

			01: 3D side by side/line interleaved/column interleaved output mode 10: 3D top/bottom output mode 11: reserved When 3D mode is enable, DEFE will enter 3D mode(source will be composed of left and right frame, output will be composed of left and right frame).

7.2.5.55. DEFE_3D_BUF_ADDR0_REG

Offset: 0xE4			Register Name: DEFE_3D_BUF_ADDR0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RIGHT_CH0_ADDR 3D mode channel 0 buffer address This address is the start address of right image in 3D mode

7.2.5.56. DEFE_3D_BUF_ADDR1_REG

Offset: 0xE8			Register Name: DEFE_3D_BUF_ADDR1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RIGHT_CH1_ADDR 3D mode channel 1 buffer address This address is the start address of right image in 3D mode

7.2.5.57. DEFE_3D_BUF_ADDR2_REG

Offset: 0xEC			Register Name: DEFE_3D_BUF_ADDR2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RIGHT_CH2_ADDR 3D mode channel 2 buffer address This address is the start address of right image in 3D mode

7.2.5.58. DEFE_3D_TB_OFF0_REG

Offset: 0xF0			Register Name: DEFE_3D_ TB_OFF0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x0	X_OFFSET1 The x offset of the bottom-right point in the first tile
15:13	/	/	/
12:8	R/W	0x0	Y_OFFSET0

			The y offset of the top-left point in the first tile
7:5	/	/	/
4:0	R/W	0x0	X_OFFSET0 The x offset of the top-left point in the first tile This value is the start offset of right image in 3D mode

7.2.5.59. DEFE_3D_TB_OFF1_REG

Offset: 0xF4			Register Name: DEFE_3D_ TB_OFF1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x0	X_OFFSET1 The x offset of the bottom-right point in the first tile
15:13	/	/	/
12:8	R/W	0x0	Y_OFFSET0 The y offset of the top-left point in the first tile
7:5	/	/	/
4:0	R/W	0x0	X_OFFSET0 The x offset of the top-left point in the first tile This value is the start offset of right image in 3D mode

7.2.5.60. DEFE_3D_TB_OFF2_REG

Offset: 0xF8			Register Name: DEFE_3D_ TB_OFF2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x0	X_OFFSET1 The x offset of the bottom-right point in the first tile
15:13	/	/	/
12:8	R/W	0x0	Y_OFFSET0 The y offset of the top-left point in the first tile
7:5	/	/	/
4:0	R/W	0x0	X_OFFSET0 The x offset of the top-left point in the first tile This value is the start offset of right image in 3D mode

7.2.5.61. DEFE_3D_WB_STRD_REG

Offset: 0xFC			Register Name: DEFE_3D_WB_STRD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:0	R/W	0x0	WB_STRIDE Write back stride length The stride length is the distance between the firt point of left image and the first point of right image for 3D top-bottom mode write back

7.2.5.62. DEFE_CH0_INSIZE_REG

Offset: 0x100			Register Name: DEFE_CH0_INSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	IN_HEIGHT Input image Y/G component height Input image height = The value of these bits add 1
15:13	/	/	/
12:0	R/W	0x0	IN_WIDTH Input image Y/G component width The image width = The value of these bits add 1 When line buffer result selection is original data, the maximum width is 4096 for yuv420 format and 2560 for others.

7.2.5.63. DEFE_CH0_OUTSIZE_REG

Offset: 0x104			Register Name: DEFE_CH0_OUTSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	OUT_HEIGHT Output layer Y/G component height The output layer height = The value of these bits add 1
15:13	/	/	/
12:0	R/W	0x0	OUT_WIDTH Output layer Y/G component width The output layer width = The value of these bits add 1 When line buffer result selection is horizontal filtered result, the

			maximum width is 4096 for yuv420 and 2560 for others

7.2.5.64. DEFE_CH0_HORZFACT_REG

Offset: 0x108			Register Name: DEFE_CH0_HORZFACT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	FACTOR_INT The integer part of the horizontal scaling ratio the horizontal scaling ratio = input width/output width
15:0	R/W	0x0	FACTOR_FRAC The fractional part of the horizontal scaling ratio the horizontal scaling ratio = input width/output width

7.2.5.65. DEFE_CH0_VERTFACT_REG

Offset: 0x10C			Register Name: DEFE_CH0_VERTFACT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	FACTOR_INT The integer part of the vertical scaling ratio the vertical scaling ratio = input height/output height
15:0	R/W	0x0	FACTOR_FRAC The fractional part of the vertical scaling ratio the vertical scaling ratio = input height /output height

7.2.5.66. DEFE_CH0_HORZPHASE_REG

Offset: 0x110			Register Name: DEFE_CH0_HORZPHASE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	PHASE Y/G component initial phase in horizontal (complement) This value equals to initial phase * 2^{16}

7.2.5.67. DEFE_CH0_VERTPHASE0_REG

Offset: 0x114			Register Name: DEFE_CH0_VERTPHASE0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	PHASE Y/G component initial phase in vertical for top field (complement) This value equals to initial phase * 2^{16}

7.2.5.68. DEFE_CH0_VERTPHASE1_REG

Offset: 0x118			Register Name: DEFE_CH0_VERTPHASE1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	PHASE Y/G component initial phase in vertical for bottom field (complement) This value equals to initial phase * 2^{16}

7.2.5.69. DEFE_CH0_HORZTAP0_REG

Offset: 0x120			Register Name: DEFE_CH0_HORZTAP0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:24	R/W	0x1	TAP3 Tap 3 offset in horizontal
23	/	/	/
22:16	R/W	0x1	TAP2 Tap 2 offset in horizontal
15	/	/	/
14:8	R/W	0x1	TAP1 Tap 1 offset in horizontal
7	/	/	/
6:0	R/W	0x7D	TAP0 Tap 0 offset in horizontal

7.2.5.70. DEFE_CH0_HORZTAP1_REG

Offset: 0x124			Register Name: DEFE_CH0_HORZTAP1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31	/	/	/
30:24	R/W	0x1	TAP7 Tap 7 offset in horizontal
23	/	/	/
22:16	R/W	0x1	TAP6 Tap 6 offset in horizontal
15	/	/	/
14:8	R/W	0x1	TAP5 Tap 5 offset in horizontal
7	/	/	/
6:0	R/W	0x1	TAP4 Tap 4 offset in horizontal

7.2.5.71. DEFE_CH0_VERTTAP_REG

Offset: 0x128			**Register Name:** DEFE_CH0_VERTTAP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:24	R/W	0x1	TAP3 Tap 3 offset in vertical
23	/	/	/
22:16	R/W	0x1	TAP2 Tap 2 offset in vertical
15	/	/	/
14:8	R/W	0x1	TAP1 Tap 1 offset in vertical
7	/	/	/
6:0	R/W	0x7F	TAP0 Tap 0 offset in vertical

7.2.5.72. DEFE_CH1_INSIZE_REG

Offset: 0x200			**Register Name:** DEFE_CH1_INSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	IN_HEIGHT Input image U/R component height Input image height = The value of these bits add 1

15:13	/	/	/
12:0	R/W	0x0	IN_WIDTH Input image U/R component width The image width = The value of these bits add 1 When line buffer result selection is original data, the maximum width is 4096 for yuv420 format and 2560 for others

7.2.5.73. DEFE_CH1_OUTSIZE_REG

Offset: 0x204			Register Name: DEFE_CH1_OUTSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	OUT_HEIGHT Output layer U/R component height The output layer height = The value of these bits add 1
15:13	/	/	/
12:0	R/W	0x0	OUT_WIDTH Output layer U/R component width The output layer width = The value of these bits add 1 When line buffer result selection is horizontal filtered result, the maximum width is 4096 for yuv420 and 2560 for others

7.2.5.74. DEFE_CH1_HORZFACT_REG

Offset: 0x208			Register Name: DEFE_CH1_HORZFACT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	FACTOR_INT The integer part of the horizontal scaling ratio the horizontal scaling ratio = input width/output width
15:0	R/W	0x0	FACTOR_FRAC The fractional part of the horizontal scaling ratio the horizontal scaling ratio = input width/output width

7.2.5.75. DEFE_CH1_VERTFACT_REG

Offset: 0x20C			Register Name: DEFE_CH1_VERTFACT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	FACTOR_INT The integer part of the vertical scaling ratio the vertical scaling ratio = input height/output height
15:0	R/W	0x0	FACTOR_FRAC The fractional part of the vertical scaling ratio the vertical scaling ratio = input height /output height

7.2.5.76. DEFE_CH1_HORZPHASE_REG

Offset: 0x210			Register Name: DEFE_CH1_HORZPHASE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	PHASE U/R component initial phase in horizontal (complement) This value equals to initial phase * 2^{16}

7.2.5.77. DEFE_CH1_VERTPHASE0_REG

Offset: 0x214			Register Name: DEFE_CH1_VERTPHASE0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	PHASE U/R component initial phase in vertical for top field (complement) This value equals to initial phase * 2^{16}

7.2.5.78. DEFE_CH1_VERTPHASE1_REG

Offset: 0x218			Register Name: DEFE_CH1_VERTPHASE1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	PHASE U/R component initial phase in vertical for bottom field

			(complement) This value equals to initial phase * 2^{16}

7.2.5.79. DEFE_CH1_HORZTAP0_REG

Offset: 0x220			Register Name: DEFE_CH1_HORZTAP0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:24	R/W	0x1	TAP3 Tap 3 offset in horizontal
23	/	/	/
22:16	R/W	0x1	TAP2 Tap 2 offset in horizontal
15	/	/	/
14:8	R/W	0x1	TAP1 Tap 1 offset in horizontal
7	/	/	/
6:0	R/W	0x7D	TAP0 Tap 0 offset in horizontal

7.2.5.80. DEFE_CH1_HORZTAP1_REG

Offset: 0x224			Register Name: DEFE_CH1_HORZTAP1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:24	R/W	0x1	TAP7 Tap 7 offset in horizontal
23	/	/	/
22:16	R/W	0x1	TAP6 Tap 6 offset in horizontal
15	/	/	/
14:8	R/W	0x1	TAP5 Tap 5 offset in horizontal
7	/	/	/
6:0	R/W	0x1	TAP4 Tap 4 offset in horizontal

7.2.5.81. DEFE_CH1_VERTTAP_REG

Offset: 0x228			Register Name: DEFE_CH1_VERTTAP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:24	R/W	0x1	TAP3 Tap 3 offset in vertical
23	/	/	/
22:16	R/W	0x1	TAP2 Tap 2 offset in vertical
15	/	/	/
14:8	R/W	0x1	TAP1 Tap 1 offset in vertical
7	/	/	/
6:0	R/W	0x7F	TAP0 Tap 0 offset in vertical

7.2.5.82. DEFE_CH0_HORZCOEF0_REGN (N=0 :31)

Offsetn: 0x400+N*4			Register Name: DEFE_CH0_HORZCOEF0_REGN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	TAP3 Horizontal tap3 coefficient The value equals to coefficient*2^6
23:16	R/W	0x0	TAP2 Horizontal tap2 coefficient The value equals to coefficient*2^6
15:8	R/W	0x0	TAP1 Horizontal tap1 coefficient The value equals to coefficient*2^6
7:0	R/W	0x0	TAP0 Horizontal tap0 coefficient The value equals to coefficient*2^6

7.2.5.83. DEFE_CH0_HORZCOEF1_REGN (N=0 :31)

Offsetn: 0x480+N*4			Register Name: DEFE_CH0_HORZCOEF1_REGN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	TAP7 Horizontal tap7 coefficient

			The value equals to coefficient*2^6
23:16	R/W	0x0	TAP6 Horizontal tap6 coefficient The value equals to coefficient*2^6
15:8	R/W	0x0	TAP5 Horizontal tap5 coefficient The value equals to coefficient*2^6
7:0	R/W	0x0	TAP4 Horizontal tap4 coefficient The value equals to coefficient*2^6

7.2.5.84. DEFE_CH0_VERTCOEF_REGN (N=0 :31)

Offsetn: 0x500+N*4			**Register Name:** DEFE_CH0_VERTCOEF_REGN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	TAP3 Vertical tap3 coefficient The value equals to coefficient*2^6
23:16	R/W	0x0	TAP2 Vertical tap2 coefficient The value equals to coefficient*2^6
15:8	R/W	0x0	TAP1 Vertical tap1 coefficient The value equals to coefficient*2^6
7:0	R/W	0x0	TAP0 Vertical tap0 coefficient The value equals to coefficient*2^6

7.2.5.85. DEFE_CH1_HORZCOEF0_REGN (N=0 :31)

Offsetn: 0x600+N*4			**Register Name:** DEFE_CH1_HORZCOEF0_REGN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	TAP3 Horizontal tap3 coefficient The value equals to coefficient*2^6
23:16	R/W	0x0	TAP2 Horizontal tap2 coefficient The value equals to coefficient*2^6
15:8	R/W	0x0	TAP1

			Horizontal tap1 coefficient The value equals to coefficient*2^6
7:0	R/W	0x0	TAP0 Horizontal tap0 coefficient The value equals to coefficient*2^6

7.2.5.86. DEFE_CH1_HORZCOEF1_REGN (N=0 :31)

Offsetn: 0x680+N*4			Register Name: DEFE_CH1_HORZCOEF1_REGN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	TAP7 Horizontal tap7 coefficient The value equals to coefficient*2^6
23:16	R/W	0x0	TAP6 Horizontal tap6 coefficient The value equals to coefficient*2^6
15:8	R/W	0x0	TAP5 Horizontal tap5 coefficient The value equals to coefficient*2^6
7:0	R/W	0x0	TAP4 Horizontal tap4 coefficient The value equals to coefficient*2^6

7.2.5.87. DEFE_CH1_VERTCOEF_REGN (N=0 :31)

Offsetn: 0x700+N*4			Register Name: DEFE_CH1_VERTCOEF_REGN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	TAP3 Vertical tap3 coefficient The value equals to coefficient*2^6
23:16	R/W	0x0	TAP2 Vertical tap2 coefficient The value equals to coefficient*2^6
15:8	R/W	0x0	TAP1 Vertical tap1 coefficient The value equals to coefficient*2^6
7:0	R/W	0x0	TAP0 Vertical tap0 coefficient The value equals to coefficient*2^6

7.2.5.88. DEFE_CH3_HORZCOEF0_REGN (N=0 :31)

Offsetn: 0x800+N*4			Register Name: DEFE_CH3_HORZCOEF0_REGN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	TAP3 Horizontal tap3 coefficient The value equals to coefficient*2^6
23:16	R/W	0x0	TAP2 Horizontal tap2 coefficient The value equals to coefficient*2^6
15:8	R/W	0x0	TAP1 Horizontal tap1 coefficient The value equals to coefficient*2^6
7:0	R/W	0x0	TAP0 Horizontal tap0 coefficient The value equals to coefficient*2^6

7.2.5.89. DEFE_CH3_HORZCOEF1_REGN (N=0 :31)

Offsetn: 0x880+N*4			Register Name: DEFE_CH3_HORZCOEF1_REGN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	TAP7 Horizontal tap7 coefficient The value equals to coefficient*2^6
23:16	R/W	0x0	TAP6 Horizontal tap6 coefficient The value equals to coefficient*2^6
15:8	R/W	0x0	TAP5 Horizontal tap5 coefficient The value equals to coefficient*2^6
7:0	R/W	0x0	TAP4 Horizontal tap4 coefficient The value equals to coefficient*2^6

7.2.5.90. DEFE_CH3_VERTCOEF_REGN (N=0 :31)

Offsetn: 0x900+N*4			Register Name: DEFE_CH3_VERTCOEF_REGN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	TAP3 Vertical tap3 coefficient

			The value equals to coefficient*2^6
23:16	R/W	0x0	TAP2 Vertical tap2 coefficient The value equals to coefficient*2^6
15:8	R/W	0x0	TAP1 Vertical tap1 coefficient The value equals to coefficient*2^6
7:0	R/W	0x0	TAP0 Vertical tap0 coefficient The value equals to coefficient*2^6

7.3. DEBE

7.3.1. OVERVIEW

- Support four moveable and size-adjustable layers
- Layer size up to 8192*8192 pixels
- Support alpha blending
- Support color key
- Support gamma correction
- Support hardware cursor
- Pre-multiply image input function
- Mixed data scaling function
- Support multi-format input data
  - Support 1/2/4/8 bpp mono / palette
  - Support 16/24/32 bpp color (external frame buffer)
  - Support YUV input channel
- Support 3D format image data
- Support output color correction
- Support write back function

7.3.2. DEBE BLOCK DIAGRAM

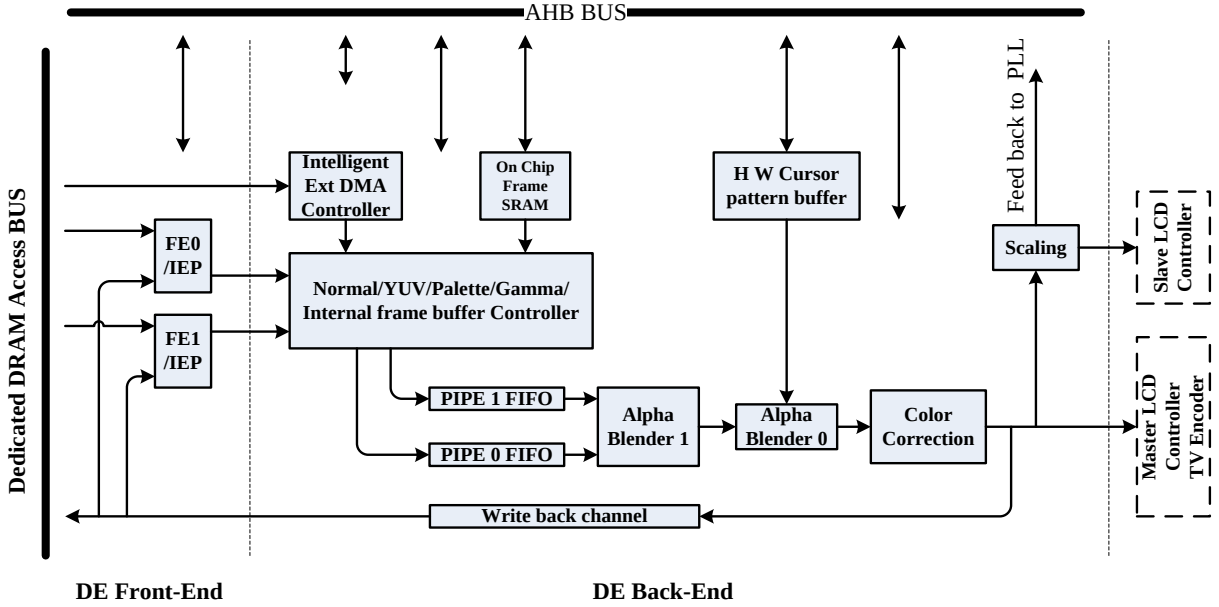


Figure 7-3 DEBE Block Diagram

7.3.3. DEBE DESCRIPTION

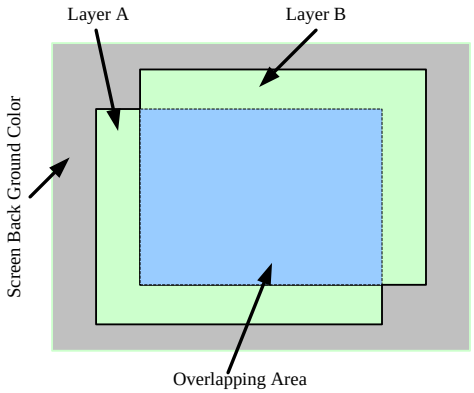
7.3.3.1. ALPHA BLENDING

Alpha blending is a convex combination of two colors allowing for transparency effects in computer graphics. The value of alpha in the color code ranges from 0.0 to 1.0, where 0.0 represents a fully transparent color, and 1.0 represents a fully opaque color.

In the display engine:

If setting the alpha register value (ARV) = 0B xxxxxxxx (8 bit value)

Then the alpha value (AV) = ARV/256



In the above diagram, layer A and layer B are not in same channel.

The alpha value of layer A : AV_a

The alpha value of layer A : AV_b

The RGB value of layer A : R_a, G_a, B_a

The RGB value of layer B : R_b, G_b, B_b

The RGB value of Background color : R_bg, G_bg, B_bg

In the only layer A area:

R = R_a * AV_a + R_bg * (1-AV_a)

G = G_a * AV_a + G_bg * (1-AV_a)

B = B_a * AV_a + B_bg * (1-AV_a)

In the only layer B area:

R = R_b * AV_b + R_bg * (1-AV_b)

G = G_b * AV_b + G_bg * (1-AV_b)

B = B_b * AV_b + B_bg * (1-AV_b)

In the overlapping area:

If the priority of layer A is higher than layer B

R = R_a * AV_a + (R_b * AV_b +R_bg * (1-AV_b)) * (1-AV_a)

G = G_a * AV_a + (G_b * AV_b +G_bg * (1-AV_b)) * (1-AV_a)

B = B_a * AV_a + (B_b * AV_b +B_bg * (1-AV_b)) * (1-AV_a)

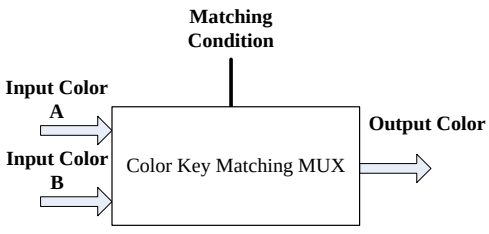
If the priority of layer A is lower than layer B

R = (R_a * AV_a +R_bg * (1-AV_a)) * (1-AV_b) + R_b * AV_b

G = (G_a * AV_a +G_bg * (1-AV_a)) * (1-AV_b) + G_b * AV_b

B = (B_a * AV_a +B_bg * (1-AV_a)) * (1-AV_b) + B_b * AV_b

7.3.3.2. COLOR KEY

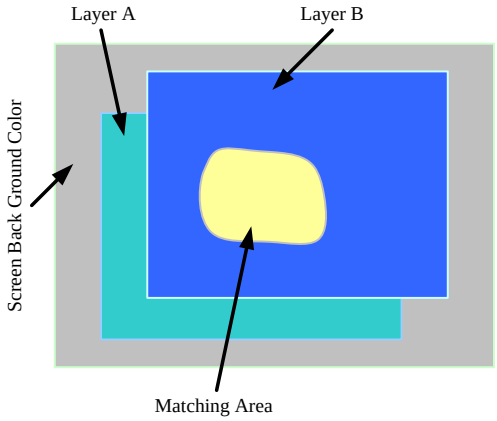


Color Key Theory Block

In display engine, color key process will be done in Alpha Blender1 block. Only 2 channels can process color key at the same coordinate of screen. If both channels are set into color key mode, the channel with higher

priority will match another channel.

See following diagram:



The alpha value of layer A : AV_a

The alpha value of layer A : AV_b

The RGB value of layer A : R_a, G_a, B_a

The RGB value of layer B : R_b, G_b, B_b

The RGB value of Background color : R_bg, G_bg, B_bg

In none matching area:

As same as normal alpha blending process

In matching area:

If priority of layer A > priority of layer B

Layer A color key setting status: True

Layer B color key setting status: True or false

Color key selection: Layer A match layer B

R = R_a * AV_a + R_bg * (1-AV_a)

G = G_a * AV_a + G_bg * (1-AV_a)

B = B_a * AV_a + B_bg * (1-AV_a)

If priority of layer A > priority of layer B

Layer A color key setting status: False

Layer B color key setting status: True

Color key selection: Layer B match layer A

R = R_b * AV_b + R_bg * (1-AV_b)

G = G_b * AV_b + G_bg * (1-AV_b)

B = B_b * AV_b + B_bg * (1-AV_b)

7.3.3.3. PIPE

There are 2 normal pipes in the engine, pipe 0 and pipe1.

In normal mode, the dedicated layer will get the data from system DRAM direct or DE front-end by setting dedicated **Layer video channel selection** bit in **DE-layer Attribute control register**. In other work mode, the layer data source also come from internal frame buffer.

In the same pipe, the highest layer pixel data can pass.

7.3.4. DEBE REGISTER LIST

Module name	Base address
BE0	0x01e60000
BE1	0x01e40000

Register name	Offset	Description
DEBE_MODCTL_REG	0x800	DEBE Mode Control Register
DEBE_BACKCOLOR_REG	0x804	DEBE Color Control Register
DEBE_DISSIZE_REG	0x808	DE-Back Display Size Setting Register
DEBE_LAYSIZE_REG	0x810 – 0x81C	DE-Layer Size Register
DEBE_LAYCOOR_REG	0x820 – 0x82C	DE-Layer Coordinate Control Register
DEBE_LAYLINEWIDTH_REG	0x840 – 0x84C	DE-Layer Frame Buffer Line Width Register
DEBE_LAYFB_L32ADD_REG	0x850 – 0x85C	DE-Layer Frame Buffer Low 32 Bit Address Register
DEBE_LAYFB_H4ADD_REG	0x860	DE-Layer Frame Buffer High 4 Bit Address Register
DEBE_REGBUFFCTL_REG	0x870	DE-Register Buffer Control Register
DEBE_CKMAX_REG	0x880	DE-Color Key MAX Register
DEBE_CKMIN_REG	0x884	DE-Color Key MIN Register
DEBE_CKCFG_REG	0x888	DE-Color Key Configuration Register
DEBE_ATTCTL_REG0	0x890 – 0x89C	DE-Layer Attribute Control Register0
DEBE_ATTCTL_REG1	0x8A0 – 0x8AC	DE-Layer Attribute Control Register1
DEBE_HWCCTL_REG	0x8D8	DE-HWC Coordinate Control Register
DEBE_HWCFBCTL_REG	0x8E0	DE-HWC Frame Buffer Format Register
DEBE_WBCTL_REG	0x8F0	DEBE Write Back Control Register
DEBE_WBADD_REG	0x8F4	DEBE Write Back Address Register

DEBE_WBLINEWIDTH_REG	0x8F8	DEBE Write Back Buffer Line Width Register
DEBE_IYUVCTL_REG	0x920	DEBE Input YUV Channel Control Register
DEBE_IYUVADD_REG	0x930 – 0x938	DEBE YUV Channel Frame Buffer Address Register
DEBE_IYUVLINEWIDTH_REG	0x940 – 0x948	DEBE YUV Channel Buffer Line Width Register
DEBE_YGCOEF_REG	0x950 – 0x958	DEBE Y/G Coefficient Register
DEBE_YGCONS_REG	0x95C	DEBE Y/G Constant Register
DEBE_URCOEF_REG	0x960 – 0x968	DEBE U/R Coefficient Register
DEBE_URCONS_REG	0x96C	DEBE U/R Constant Register
DEBE_VBCOEF_REG	0x970 – 0x978	DEBE V/B Coefficient Register
DEBE_VBCONS_REG	0x97C	DEBE V/B Constant Register
DEBE_OCCTL_REG	0x9C0	DEBE Output Color Control Register
DEBE_OCRCOEF_REG	0x9D0-0x9D8	DEBE Output Color R Coefficient Register
DEBE_OCRCONS_REG	0x9DC	DEBE Output Color R Constant Register
DEBE_OCGCOEF_REG	0x9E0-0x9E8	DEBE Output Color G Coefficient Register
DEBE_OCGCONS_REG	0x9EC	DEBE Output Color G Constant Register
DEBE_OCBCOEF_REG	0x9F0-0x9F8	DEBE Output Color B Coefficient Register
DEBE_OCBCONS_REG	0x9FC	DEBE Output Color B Constant Register
Memories		
0x4400-0x47FF	Gamma Table	
0x4800-0x4BFF	DE-HWC Pattern Memory Block	
0x4C00-0x4FFF	DE-HWC Color Palette Table	
0x5000-0x53FF	Pipe0 Palette Table	
0x5400-0x57FF	Pipe1 Palette Table	

7.3.5. DEBE REGISTER DESCRIPTION

7.3.5.1. DEBE MODE CONTROL REGISTER

Offset: 0x800			Register Name: DEBE_MODCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0	**LINE_SEL** Start top/bottom line selection in interlace mode
28	R/W	0	**ITLMOD_EN** Interlace mode enable 0:disable 1:enable
27	/	/	/
22:20	R/W	0	**OUT_SEL** Output selection 000:LCD 110:FE0 only 111:FE1 only Other: reserved
19:18	/	/	/
17	R/W	0	**OSCA_EN** Output scaling function enable 0:disable 1:enable
16	R/W	0	**HWC_EN** Hardware cursor enabled/disabled control 0: Disabled 1: Enabled Hardware cursor has the highest priority, in the alpha blender0,

			the alpha value of cursor will be selected
15:12	/	/	/
11	R/W	0	**LAY3_EN** Layer3 Enable/Disable 0: Disabled 1: Enabled
10	R/W	0	**LAY2_EN** Layer2 Enable/Disable 0: Disabled 1: Enabled
9	R/W	0	**LAY1_EN** Layer1 Enable/Disable 0: Disabled 1: Enabled
8	R/W	0	**LAY0_EN** Layer0 Enable/Disable 0: Disabled 1: Enabled
7:2	/	/	/
1	R/W	0	**START_CTL** Normal output channel Start & Reset control 0: reset 1: start
0	R/W	0	**DEBE_EN** DE back-end enable/disable 0: disable 1: enable

7.3.5.2. DE-BACK COLOR CONTROL REGISTER

Offset: 0x804			Register Name: DEBE_BACKCOLOR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	UDF	**BK_RED** Red Red screen background color value
15:8	R/W	UDF	**BK_GREEN** Green Green screen background color value
7:0	R/W	UDF	**BK_BLUE** Blue Blue screen background color value

7.3.5.3. DE-BACK DISPLAY SIZE SETTING REGISTER

Offset: 0x808			Register Name: DEBE_DISSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	UDF	**DIS_HEIGHT** Display height The real display height = The value of these bits add 1
15:0	R/W	UDF	**DIS_WIDTH** Display width The real display width = The value of these bits add 1

7.3.5.4. DE-LAYER SIZE REGISTER

Offset: Layer 0: 0x810 Layer 1: 0x814 Layer 2: 0x818	Register Name: DEBE_LAYSIZE_REG

Layer 3: 0x81C			
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	UDF	**LAY_HEIGHT** Layer Height The Layer Height = The value of these bits adds 1
15:13	/	/	/
12:0	R/W	UDF	**LAY_WIDTH** Layer Width The Layer Width = The value of these bits adds 1

7.3.5.5. DE-LAYER COORDINATE CONTROL REGISTER

Offset: **Layer 0: 0x820** **Layer 1: 0x824** **Layer 2: 0x828** **Layer 3: 0x82C**			**Register Name: DEBE_LAYCOOR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	UDF	**LAY_YCOOR** Y coordinate Y is the left-top y coordinate of layer on screen in pixels The Y represents the two's complement
15:0	R/W	UDF	**LAY_XCOOR** X coordinate X is left-top x coordinate of the layer on screen in pixels The X represents the two's complement

Notes: Setting the layer0-layer3 the coordinate (left-top) on screen control information

7.3.5.6. DE-LAYER FRAME BUFFER LINE WIDTH REGISTER

Offset: Layer 0: 0x840 Layer 1: 0x844 Layer 2: 0x848 Layer 3: 0x84C			Register Name: DEBE_LAYLINEWIDTH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	UDF	**LAY_LINEWIDTH** Layer frame buffer line width in bits

Notes: If the layer is selected by video channel or YUV channel, the setting of this register will be ignored.

7.3.5.7. DE-LAYER FRAME BUFFER LOW 32 BIT ADDRESS REGISTER

Offset: Layer 0: 0x850 Layer 1: 0x854 Layer 2: 0x858 Layer 3: 0x85C			Register Name: DEBE_LAYFB_L32ADD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	UDF	**LAYFB_L32ADD** Buffer start Address Layer Frame start Buffer Address in bit

Notes: If the layer is selected by video channel or YUV channel, the setting of this register will be ignored.

7.3.5.8. DE-LAYER FRAME BUFFER HIGH 4 BIT ADDRESS REGISTER

Offset: 0x860			Register Name: DEBE_LAYFB_H4ADD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	UDF	**LAY3FB_H4ADD** Layer3

			Layer Frame Buffer Address in bit
23:20	/	/	/
19:16	R/W	UDF	**LAY2FB_H4ADD** Layer2 Layer Frame Buffer Address in bit
15:12	/	/	/
11:8	R/W	UDF	**LAY1FB_H4ADD** Layer1 Layer Frame Buffer Address in bit
7:4	/	/	/
3:0	R/W	UDF	**LAY0FB_H4ADD** Layer0 Layer Frame Buffer Address in bit

Notes: If the layer is selected by video channel or YUV channel, the setting of this register will be ignored.

7.3.5.9. DE-REGISTER BUFFER CONTROL REGISTER

Offset: 0x870			**Register Name: DEBE_REGBUFFCTL_REG**
Bit	Read/Write	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0X00	**REGAUTOLOAD_DIS** Module registers loading auto mode disable control 0: registers auto loading mode 1: disable registers auto loading mode, the registers will be loaded by write 1 to bit0 of this register
0	R/W	0X00	**REGLOADCTL** Register load control When the Module registers loading auto mode disable control bit is set, the registers will be loaded by write 1 to the bit, and the bit will self clean when the registers is loading done.

7.3.5.10. DE-COLOR KEY MAX REGISTER

Offset: 0x880			Register Name: DEBE_CKMAX_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	UDF	**CKMAX_R** Red Red color key max
15:8	R/W	UDF	**CKMAX_G** Green Green color key max
7:0	R/W	UDF	**CKMAX_B** Blue Blue color key max

7.3.5.11. DE-COLOR KEY MIN REGISTER

Offset: 0x884			Register Name: DEBE_CKMIN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	UDF	**CKMIN_R** Red Red color key min
15:8	R/W	UDF	**CKMIN_G** Green Green color key min
7:0	R/W	UDF	**CKMIN_B** Blue Blue color key min

7.3.5.12. DE-COLOR KEY CONFIGURATION REGISTER

Offset: 0x888			Register Name: DEBE_CKCFG_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5:4	R/W	UDF	**CKR_MATCH** Red Match Rule 00: always match 01: always match 10: match if (Color Min=<Color<=Color Max) 11: match if (Color>Color Max or Color<Color Min)
3:2	R/W	UDF	**CKG_MATCH** Green Match Rule 00: always match 01: always match 10: match if (Color Min=<Color<=Color Max) 11: match if (Color>Color Max or Color<Color Min)
1:0	R/W	UDF	**CKB_MATCH** Blue Match Rule 00: always match 01: always match 10: match if (Color Min=<Color<=Color Max) 11: match if (Color>Color Max or Color<Color Min)

7.3.5.13. DE-LAYER ATTRIBUTE CONTROL REGISTER0

Offset: Layer0: 0x890 Layer1: 0x894 Layer2: 0x898 Layer3: 0x89C	Register Name: DEBE_ATTCTL_REG0

Bit	Read/Write	Default/Hex	Description
31:24	R/W	UDF	**LAY_GLBALPHA** Alpha value Alpha value is used for this layer
23:22	R/W	UDF	**LAY_WORKMOD** Layer working mode selection 00: normal mode (Non-Index mode) 01: palette mode (Index mode) 10: internal frame buffer mode 11: gamma correction Except the normal mode, if the other working mode is selected, the on chip SRAM will be enabled.
21:20	R/W	UDF	**PREMUL** 0: normal input layer 1: pre-multiply input layer Other: reserved
19:18	R/W	UDF	**CKEN** Color key Mode 00: disabled color key 01: The layer color key match another channel pixel data in Alpha Blender1. 1x: Reserved Only 2 channels pixel data can get to Alpha Blender1 at the same screen coordinate.
17:16	/	/	/
15	R/W	UDF	**LAY_PIPESEL** Pipe Select

			0: select Pipe 0 1: select Pipe 1
14:12	/	/	/
11:10	R/W	UDF	**LAY_PRISEL** Priority The rule is: 11>10>01>00 When more than 2 layers are enabled, the priority value of each layer must be different, soft designer must keep the condition. If more than 1 layer selects the same pipe, in the overlapping area, only the pixel of highest priority layer can pass the pipe to blender1. If both 2 pipes are selected by layers, in the overlapping area, the alpha value will use the alpha value of higher priority layer in the blender1.
9:5	/	/	/
4	R/W	UDF	**LAY_VDOSEL** Video channel selection control 0:select video channel 0 (FE0) 1:select video channel 1 (FE1) The selection setting is only valid when Layer video channel selection is enabled.
3	/	/	/
2	R/W	UDF	**LAY_YUVEN** YUV channel selection 0: disable

			1: enable Setting 2 or more layers YUV channel mode is illegal, programmer should confirm it.
1	R/W	UDF	**LAY_VDOEN** Layer video channel selection enable control 0: disable 1: enable Normally, one layer can not be set both video channel and YUV channel mode, if both 2 mode is set, the layer will work in video channel mode, YUV channel mode will be ignored, programmer should confirm it. Setting 2 or more layers video channel mode is illegal, programmer should confirm it.
0	R/W	UDF	**LAY_GLBALPHAEN** Alpha Enable 0: Disabled the alpha value of this register 1: Enabled the alpha value of this register for the layer

7.3.5.14. DE-LAYER ATTRIBUTE CONTROL REGISTER1

Offset: **Layer0: 0x8A0** **Layer1: 0x8A4** **Layer2: 0x8A8** **Layer3: 0x8AC**			**Register Name: DEBE_ATTCTL_REG1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/

15:14	R/W	UDF	**LAY_HSCAFCT** Setting the internal frame buffer scaling factor, only valid in internal frame buffer mode SH Height scale factor 00: no scaling 01: *2 10: *4 11: Reserved
13:12	R/W	UDF	**LAY_WSCAFCT** Setting the internal frame buffer scaling factor, only valid in internal frame buffer mode SW Width scale factor 00: no scaling 01: *2 10: *4 11: Reserved
11:8	R/W	UDF	**LAY_FBFMT** Frame buffer format Normal mode data format 0000: mono 1-bpp 0001: mono 2-bpp 0010: mono 4-bpp 0011: mono 8-bpp 0100: color 16-bpp (R:6/G:5/B:5) 0101: color 16-bpp (R:5/G:6/B:5) 0110: color 16-bpp (R:5/G:5/B:6) 0111: color 16-bpp (Alpha:1/R:5/G:5/B:5)

			1000: color 16-bpp (R:5/G:5/B:5/Alpha:1) 1001: color 24-bpp (Padding:8/R:8/G:8/B:8) 1010: color 32-bpp (Alpha:8/R:8/G:8/B:8) 1011: color 24-bpp (R:8/G:8/B:8) 1100: color 16-bpp (Alpha:4/R:4/G:4/B:4) 1101: color 16-bpp (R:4/G:4/B:4/Alpha:4) Other: Reserved Palette Mode data format In palette mode, the data of external frame buffer is regarded as pattern. 0000: 1-bpp 0001: 2-bpp 0010: 4-bpp 0011: 8-bpp other: Reserved Internal Frame buffer mode data format 0000: 1-bpp 0001: 2-bpp 0010: 4-bpp 0011: 8-bpp Other: Reserved
7:3	/	/	/
2	R/W	UDF	**LAY_BRSWAPEN** B R channel swap 0: RGB. Follow the bit[11:8]----RGB 1: BGR. Swap the B R channel in the data format.
1:0	R/W	UDF	**LAY_FBPS**

			PS Pixels Sequence See following “Pixels Sequence Table”

7.3.5.15. PIXELS SEQUENCE TABLE

DE-layer attribute control register1 [11:08] = FBF (frame buffer format)

DE-layer attribute control register1 [01:00] = PS (pixels sequence)

MONO OR INTERNAL FRAME BUFFER 1-BPP OR PALETTE 1-BPP MODE : FBF = 0000

PS=00

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16
P15	P14	P13	P12	P11	P10	P09	P08	P07	P06	P05	P04	P03	P02	P01	P00
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=01

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P24	P25	P26	P27	P28	P29	P30	P31	P16	P17	P18	P19	P20	P21	P22	P23
P08	P09	P10	P11	P12	P13	P14	P15	P00	P01	P02	P03	P04	P05	P06	P07
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=10

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P07	P06	P05	P04	P03	P02	P01	P00	P15	P14	P13	P12	P11	P10	P09	P08

P23	P22	P21	P20	P19	P18	P17	P16	P31	P30	P29	P28	P27	P26	P25	P24
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=11

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P00	P01	P02	P03	P04	P05	P06	P07	P08	P09	P10	P11	P12	P13	P14	P15
P16	P17	P18	P19	P20	P21	P22	P23	P24	P25	P26	P27	P28	P29	P30	P31
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

MONO OR INTERNAL FRAME BUFFER 2-BPP OR PALETTE 2-BPP MODE : FBF = 0001

PS=00

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P15		P14		P13		P12		P11		P10		P09		P08	
P07		P06		P05		P04		P03		P02		P01		P00	
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=01

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P12		P13		P14		P15		P08		P09		P10		P11	
P04		P05		P06		P07		P00		P01		P02		P03	
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=10

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P03		P02		P01		P00		P07		P06		P05		P04	

P11	P10	P09	P08	P15	P14	P13	P12
15 14	13 12	11 10	09 08	07 06	05 04	03 02	01 00

PS=11

Bit

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16
P00	P01	P02	P03	P04	P05	P06	P07
P08	P09	P10	P11	P12	P13	P14	P15
15 14	13 12	11 10	09 08	07 06	05 04	03 02	01 00

MONO 4-BPP OR PALETTE 4-BPP MODE : FBF = 0010

PS=00

Bit

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16
P07		P06		P05		P04	
P03		P02		P01		P00	
15 14	13 12	11 10	09 08	07 06	05 04	03 02	01 00

PS=01

Bit

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16
P06		P07		P04		P05	
P02		P03		P00		P01	
15 14	13 12	11 10	09 08	07 06	05 04	03 02	01 00

PS=10

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P01				P00				P03				P02			
P05				P04				P07				P06			
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=11

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P00				P01				P02				P03			
P04				P05				P06				P07			
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

MONO 8-BPP MODE OR PALETTE 8-BPP MODE : FBF = 0011

PS=00/11

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P3								P2							
P1								P0							
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=01/10

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P0								P1							
P2								P3							
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

COLOR 16-BPP MODE : FBF = 0100 OR 0101 OR 0110 OR 0111 OR 1000

PS=00

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P1															
P0															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=01

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P0															
P1															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=10/11

Invalid

COLOR 24-BPP OR 32-BPP MODE : FBF = 1001 OR 1010

PS=00/01

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P0															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

The bytes sequence is ARGB

PS=10/11

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P0															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

The bytes sequence is BGRA

7.3.5.16. DE-HWC COORDINATE CONTROL REGISTER

Offset: 0x8D8			Register Name: DEBE_HWCCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	UDF	**HWC_YCOOR** Hardware cursor Y coordinate
15:0	R/W	UDF	**HWC_XCOOR** Hardware cursor X coordinate

7.3.5.17. DE-HWC FRAME BUFFER FORMAT REGISTER

Offset: 0x8E0			Register Name: DEBE_HWCFBCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	UDF	**HWC_YCOOROFF** Y coordinate offset The hardware cursor is 32*32 2-bpp pattern, this value represent the start position of the cursor in Y coordinate
23:16	R/W	UDF	**HWC_XCOOROFF** X coordinate offset The hardware cursor is 32*32 2-bpp pattern, this value represent the start position of the cursor in X coordinate
15:6	/	/	/
5:4	R/W	UDF	**HWC_YSIZE** Y size control 00: 32pixels per line 01: 64pixels per line

			Other: reserved
3:2	R/W	UDF	**HWC_XSIZE** X size control 00: 32pixels per row 01: 64pixels per row Other: reserved
1:0	R/W	UDF	**HWC_FBFMT** Pixels format control 00: 1bpp 01: 2bpp 10: 4bpp 11: 8bpp

7.3.5.18. DEBE WRITE BACK CONTROL REGISTER

Offset: 0x8F0			Register Name: DEBE_WBCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12	R/W	UDF	**WB_FMT** Write back data format setting 0: ARGB (little endian system) 1: BGRA (little endian system)
11:10	/	/	/
9	R/W	UDF	**WB_EFLAG** Error flag 0: 1: write back error
8	R/W	UDF	**WB_STATUS**

			Write-back process status 0: write-back end or write-back disable 1: write-back in process This flag indicates that a full frame has not been written back to memory. The bit will be set when write-back enable bit is set, and be cleared when write-back process end.
7:2	/	/	/
1	R/W	UDF	**WB_WOC** Write back only control 0: disable the write back only control, the normal channel data of back end will transfer to LCD/TV controller too. 1: enable the write back only function, the all output data will by pass the LCD/TV controller.
0	R/W	UDF	**WB_EN** Write back enable 0: Disable 1: Enable If normal channel of back-end is selected by LCD/TV controller (write back only function is disabled), the writing back process will start when write back enable bit is set and a new frame processing begins. The bit will be cleared when the new writing-back frame start to process.

7.3.5.19. DEBE WRITE BACK ADDRESS REGISTER

Offset: 0x8F4			Register Name: DEBE_WBADD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	UDF	**WB_ADD** The start address of write back data in WORD

7.3.5.20. DEBE WRITE BACK BUFFER LINE WIDTH REGISTER

Offset: 0x8F8			Register Name: DEBE_WBLINEWIDTH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	UDF	**WB_LINEWIDTH** Write back image buffer line width in bits

7.3.5.21. DEBE INPUT YUV CHANNEL CONTROL REGISTER

Offset: 0x920			Register Name: DEBE_IYUVCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:12	R/W	UDF	**IYUV_FBFMT** Input data format 000: planar YUV 411 001: planar YUV 422 010: planar YUV 444 011: interleaved YUV 422 100: interleaved YUV 444 Other: illegal
11:10	/	/	/
9:8	R/W	UDF	**IYUV_FBPS** Pixel sequence **In planar data format mode:** 00: Y3Y2Y1Y0

			01: Y0Y1Y2Y3 (the other 2 components are same) Other: illegal **In interleaved YUV 422 data format mode:** 00: UYVY 01: YUYV 10: VYUY 11: YVYU **In interleaved YUV 444 data format mode:** 00: AYUV 01: VUYA Other: illegal
7:5	/	/	/
4	R/W	UDF	**IYUV_LINNEREN** 0: linner 1:
3:1	/	/	/
0	R/W	UDF	**IYUV_EN** YUV channel enable control 0: disable 1: enable

SOURCE DATA INPUT DATA PORTS:

Input buffer channel	Planar YUV	Interleaved YUV
Channel0	Y	YUV
Channel1	U	-
Channel2	V	-

7.3.5.22. DEBE YUV CHANNEL FRAME BUFFER ADDRESS REGISTER

Offset: Channel 0 : 0x930 Channel 1 : 0x934 Channel 2 : 0x938			Register Name: DEBE_IYUVADD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	UDF	**IYUV_ADD** Buffer Address Frame buffer address in BYTE

7.3.5.23. DEBE YUV CHANNEL BUFFER LINE WIDTH REGISTER

Offset: Channel 0 : 0x940 Channel 1 : 0x944 Channel 2 : 0x948			Register Name: DEBE_IYUVLINEWIDTH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	UDF	**IYUV_LINEWIDTH** Line width The width is the distance from the start of one line to the start of the next line. Description in bits

YUV TO RGB CONVERSION ALGORITHM FORMULA:

R =

(R Y component coefficient * Y) +

(R U component coefficient * U) +

(R V component coefficient * V) +

R constant

G = (G Y component coefficient * Y) + (G U component coefficient * U) + (G V component coefficient * V) + G constant B = (B Y component coefficient * Y) + (B U component coefficient * U) + (B V component coefficient * V) + B constant

7.3.5.24. DEBE Y/G COEFFICIENT REGISTER

Offset: G/Y component: 0x950 R/U component: 0x954 B/V component: 0x958			Register Name: DEBE_YGCOEF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	UDF	**IYUV_YGCOEF** the Y/G coefficient the value equals to coefficient*2^{10}

7.3.5.25. DEBE Y/G CONSTANT REGISTER

Offset: 0x95C			Register Name: DEBE_YGCONS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	/	/	/
15:14	/	/	/

13:0	R/W	UDF	**IYUV_YGCONS** the Y/G constant the value equals to coefficient*2^4

7.3.5.26. DEBE U/R COEFFICIENT REGISTER

Offset: **G/Y component: 0x960** **R/U component: 0x964** **B/V component: 0x968**			**Register Name: DEBE_URCOEF_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	/	/	/
15:13	/	/	/
12:0	R/W	UDF	**IYUV_URCOEF** the U/R coefficient the value equals to coefficient*2^{10}

7.3.5.27. DEBE U/R CONSTANT REGISTER

Offset: 0x96C			**Register Name: DEBE_URCONS_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	/	/	/
15:14	/	/	/
13:0	R/W	UDF	**IYUV_URCONS** the U/R constant the value equals to coefficient*2^4

7.3.5.28. DEBE V/B COEFFICIENT REGISTER

Offset:	**Register Name: DEBE_VBCOEF_REG**

G/Y component: 0x970 R/U component: 0x974 B/V component: 0x978			
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	/	/	/
15:13	/	/	/
12:0	R/W	UDF	**IYUV_VBCOEF** the V/B coefficient the value equals to coefficient*2^{10}

7.3.5.29. DEBE V/B CONSTANT REGISTER

Offset: 0x97C			Register Name: DEBE_VBCONS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	/	/	/
15:14	/	/	/
13:0	R/W	UDF	**IYUV_VBCONS** the V/B constant the value equals to coefficient*2^{4}

7.3.5.30. DEBE OUTPUT COLOR CONTROL REGISTER

Offset: 0x9C0			Register Name: DEBE_OCCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	UDF	**OC_EN** Color control module enable control 0: disable 1: enable

COLOR CORRECTION CONVERSION ALGORITHM FORMULA:

R =

(R R component coefficient * R) +

(R G component coefficient * G) +

(R B component coefficient * B) +

R constant

G =

(G R component coefficient * R) +

(G G component coefficient * G) +

(G B component coefficient * B) +

G constant

B =

(B R component coefficient * R) +

(B G component coefficient * G) +

(B B component coefficient * B) +

B constant

7.3.5.31. DEBE OUTPUT COLOR R COEFFICIENT REGISTER

Offset: R component: 0x9D0 G component: 0x9D4 B component: 0x9D8			Register Name: DEBE_OCRCOEF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	UDF	**OC_RCOEF** the R coefficient

			the value equals to coefficient*2^{10}

7.3.5.32. DEBE OUTPUT COLOR R CONSTANT REGISTER

Offset: 0x9DC			Register Name: DEBE_OCRCONS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:0	R/W	UDF	**OC_RCONS** the R constant the value equals to coefficient*2^4

7.3.5.33. DEBE OUTPUT COLOR G COEFFICIENT REGISTER

Offset: R component: 0x9E0 G component: 0x9E4 B component: 0x9E8			Register Name: DEBE_OCGCOEF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	UDF	**OC_GCOEF** the G coefficient the value equals to coefficient*2^{10}

7.3.5.34. DEBE OUTPUT COLOR G CONSTANT REGISTER

Offset: 0x9EC			Register Name: DEBE_OCGCONS_REG
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14:0	R/W	UDF	**OC_GCONS** the G constant the value equals to coefficient*2^4

7.3.5.35. DEBE OUTPUT COLOR B COEFFICIENT REGISTER

Offset: G/Y component: 0x9F0 R/U component: 0x9F4 B/V component: 0x9F8			Register Name: DEBE_OCBCOEF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	UDF	**OC_BCOEF** the B coefficient the value equals to coefficient*2^{10}

7.3.5.36. DEBE OUTPUT COLOR B CONSTANT REGISTER

Offset: 0x9FC			Register Name: DEBE_OCBCONS_REG
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14:0	R/W	UDF	**OC_BCONS** the B constant the value equals to coefficient*2^{4}

7.3.5.37. DE-HWC PATTERN MEMORY BLOCK

Function:

1bpp:

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16
P15	P14	P13	P12	P11	P10	P09	P08	P07	P06	P05	P04	P03	P02	P01	P00
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

2bpp:

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P15		P14		P13		P12		P11		P10		P09		P08	
P07		P06		P05		P04		P03		P02		P01		P00	
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

4bpp:

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P07				P06				P05				P04			
P03				P02				P01				P00			
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

8bpp:

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P3								P2							
P1								P0							
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Offset: **0x4800-0x4BFF**			**DE-HW cursor pattern memory block**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	UDF	Hardware cursor pixel pattern Specify the color displayed for each of the hardware cursor pixels.

7.3.5.38. DE-HWC PALETTE TABLE

Offset: 0x4C00-0x4FFF			DE-HW palette table
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	UDF	Alpha value
23:16	R/W	UDF	Red value
15:8	R/W	UDF	Green value
7:0	R/W	UDF	Blue value

Following figure (only with 2bpp mode) shows the RAM array used for hardware cursor palette lookup and the corresponding colors output.

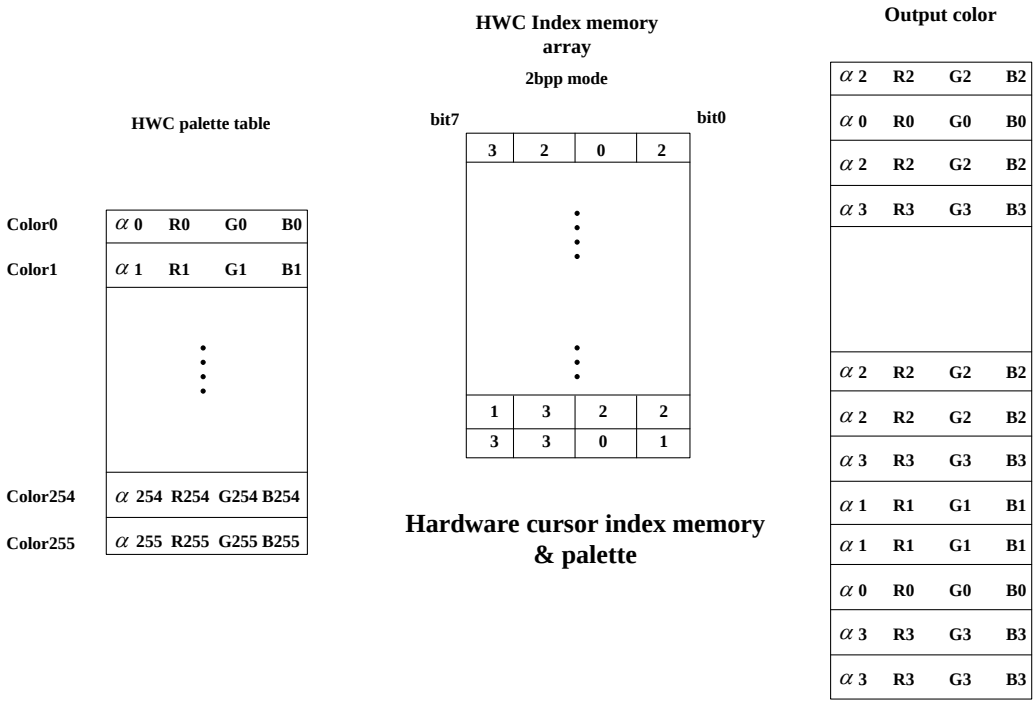


Figure 7-4 Hardware Cursor Index Memory and Palette

7.3.5.39. PALETTE MODE

Offset: Pipe0:0x5000-0x53FF Pipe1:0x5400-0x57FF	Pipe palette color table SRAM block

Bit	Read/Write	Default/Hex	Description
31:24	R/W	UDF	Alpha value
23:16	R/W	UDF	Red value
15:8	R/W	UDF	Green value
7:0	R/W	UDF	Blue value

In this mode, RAM array is used for palette lookup table, each pixel in the layer frame buffer is treated as an index into the RAM array to select the actual color.

The follow figure shows the RAM array used for palette lookup and the corresponding colors output.

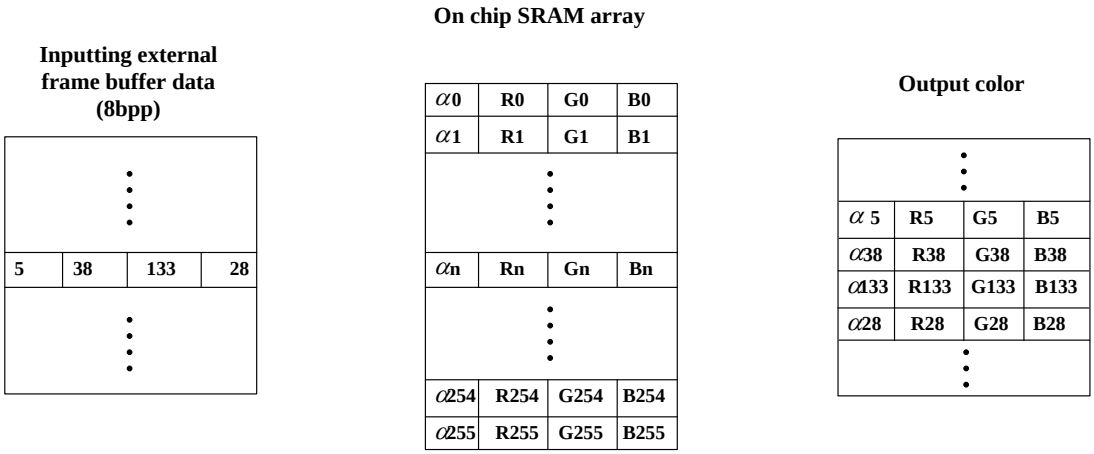


Figure 7-5 On-Chip SRAM for Palette Lookup

7.3.5.40. INTERNAL FRAME BUFFER MODE:

In internal frame buffer mode, the RAM array is used as an on-chip frame buffer, each pixel in the RAM array is used to select one of the palette 32-bit colors.

1bpp:

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16
P15	P14	P13	P12	P11	P10	P09	P08	P07	P06	P05	P04	P03	P02	P01	P00
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

2bpp:

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P15		P14		P13		P12		P11		P10		P09		P08	
P07		P06		P05		P04		P03		P02		P01		P00	
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

4bpp:

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P07				P06				P05				P04			
P03				P02				P01				P00			
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

8bpp:

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P3								P2							
P1								P0							
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Offset: **0x4000-0x57FF**			**DE-on chip SRAM block**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	UDF	Internal frame buffer pixel pattern Specify the color displayed for each of the internal frame buffer pixels.

7.3.5.41. INTERNAL FRAME BUFFER MODE PALETTE TABLE

Address: Pipe0:0x5000-0x53FF Pipe1:0x5400-0x57FF			Pipe palette table
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	UDF	Alpha value
23:16	R/W	UDF	Red value
15:8	R/W	UDF	Green value
7:0	R/W	UDF	Blue value

Following figure shows the RAM array used for internal frame buffer mode and the corresponding colors output.

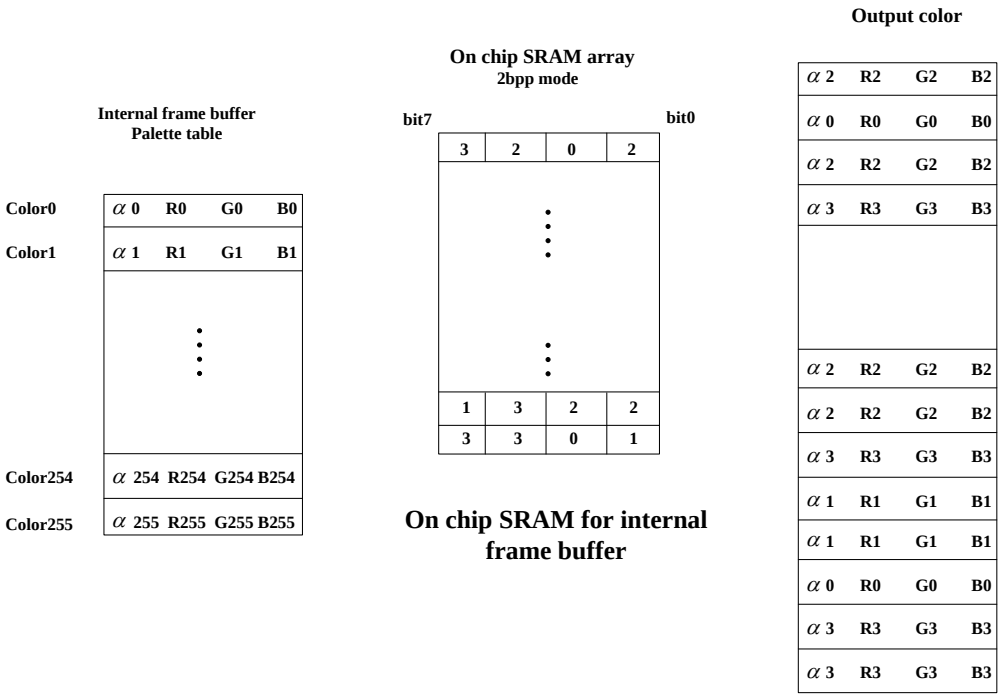


Figure 7-6 On-chip SRAM for Internal Frame Buffer

7.3.5.42. GAMMA CORRECTION MODE

Offset: 0x4400-0x47FF	DE-on chip SRAM block

Bit	Read/Write	Default/Hex	Description
31:24	R/W	UDF	Alpha channel intensity
23:16	R/W	UDF	Red channel intensity
15:8	R/W	UDF	Green channel intensity
7:0	R/W	UDF	Blue channel intensity

In gamma correction mode, the RAM array is used for gamma correction, each pixel's alpha, red, green, and blue color component is treated as an index into the SRAM array. The corresponding alpha, red, green, or blue channel intensity value at that index is used in the actual color.

Following figure shows the RAM array used for gamma correction and the corresponding colors output.

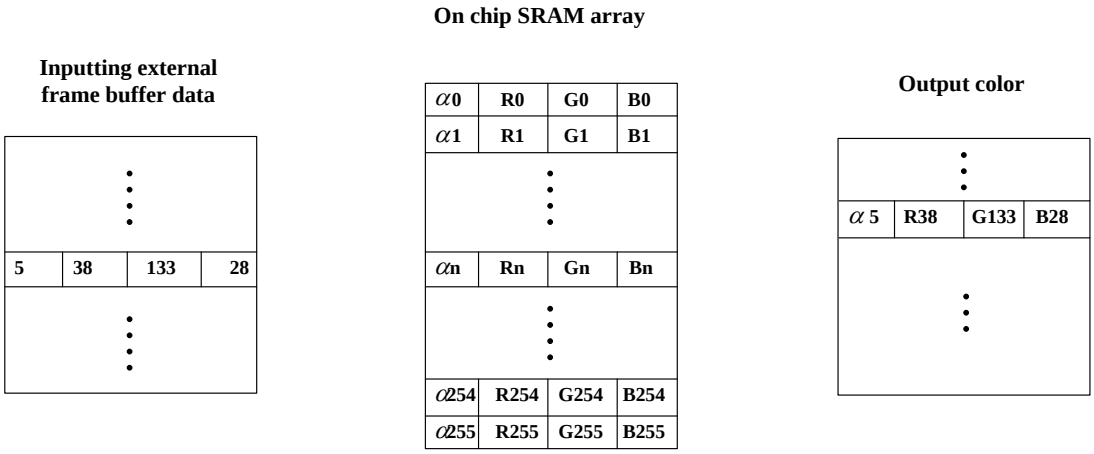


Figure 7-7 On-Chip SRAM foR Gamma Correction

7.4. DISPLAY ENGINE MEMORY MAPPING

Base Address:
BE0: 0x01e60000
BE1: 0x01e40000

Offset:	
0x0000 0x07FF	**Reserved**
0x0800 0x0DFF	**Registers**
0x0E00 0x3FFF	**Reserved**
0x4000 0x43FF	**Reserved**
0x4400 0x47FF	**Gamma Table**
0x4800 0x4BFF	**HWC Memory Block**
0x4C00 0x4FFF	**HWC Palette Table**
0x5000 0x53FF	**PIPE0 Palette Table**
0x5400 0x57FF	**PIPE1 Palette Table**
0x5800 0xFFFF	**Reserved**

7.5. HDMI

7.5.1. OVERVIEW

The HDMI features:

- Comply with HDMI V1.4
- Standard DDC master
- Support up to 148.5M pixel/second
- Support Max 1080P resolution
- Support 3D format display up to 1080P
- Support 480I/576I/480P/576P/720P/1080I/1080P at 24/25/30/50/59.9hz
- Support 24-bit RGB data format, with 2X repeater
- Support up to 8 channels , 24bit PCM(IEC60958)
- Hardware Receiver active sense and Hot plug detection

7.5.2. HDMI BLOCK DIAGRAM

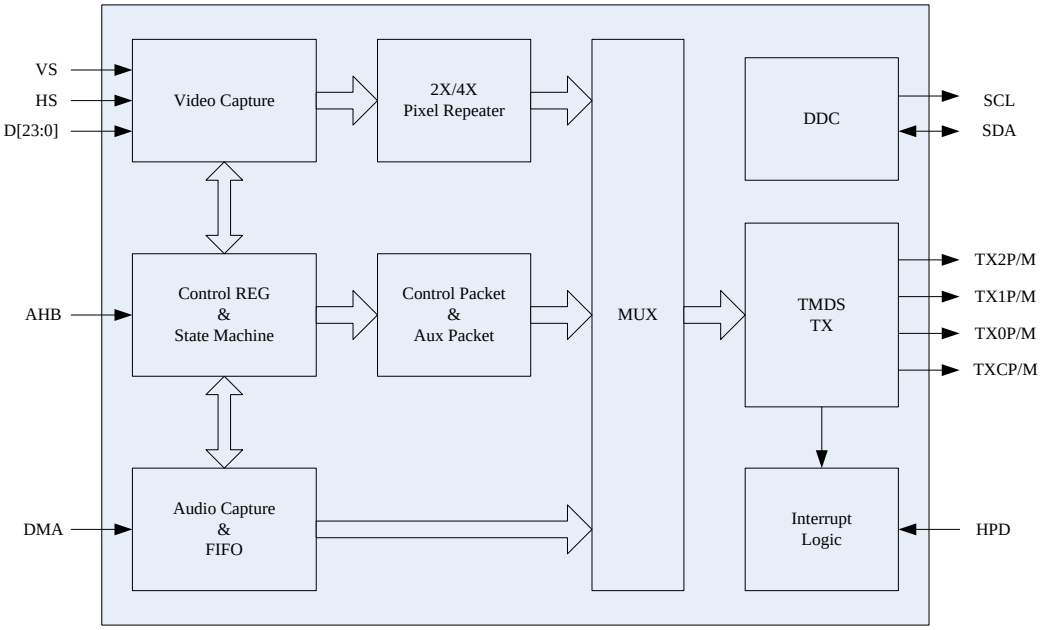


Figure 7-8 HDMI Block Diagram

7.5.3. HDMI CONTROL REGISTER LIST

Module Name	Base Address
HDMI	0x01C16000

Register Name	Offset	Description
HDMI_VERSION_ID	0x000	Version ID register
HDMI_CTRL	0x004	System control register
HDMI_INT_STATUS	0x008	Interrupt register
HDMI_HPD	0x00c	Hot plug detect register
HDMI_VID_CTRL	0x010	Video control register
HDMI_VID_TIMING_0	0x014	Video timing register 0
HDMI_VID_TIMING_1	0x018	Video timing register 1
HDMI_VID_TIMING_2	0x01c	Video timing register 2

HDMI_VID_TIMING_3	0x020	Video timing register 3
HDMI_VID_TIMING_4	0x024	Video timing register 4
HDMI_AUD_CTRL	0x040	Audio control register
HDMI_ADMA_CTRL	0x044	Audio DMA&FIFO control register
HDMI_AUD_FMT	0x048	Audio Format control register
HDMI_AUD_PCM_CTRL	0x04c	Audio PCM control register
HDMI_AUD_CTS	0x050	ACR CTS
HDMI_AUD_N	0x054	ACR N
HDMI_AUD_CH_STATUS0	0x058	Audio channel Status register 0
HDMI_AUD_CH_STATUS1	0x05c	Audio channel Status register 1
HDMI_AVI_INFO_PKT	0x080	AVI Info Frame
HDMI_AUD_INFO_PKT	0x0a0	Audio Info Frame
HDMI_ACP_PKT	0x0c0	ACP packet
HDMI_GP_PKT	0x0e0	General Control Packet
HDMI_PAD_CTRL0	0x200	PLL/DRV Setting 0
HDMI_PAD_CTRL1	0x204	PLL/DRV Setting 1
HDMI_PLL_CTRL	0x208	PLL/DRV Setting 2
HDMI_PLL_DBG0	0x20c	PLL/DRV Setting 3
HDMI_PLL_DBG1	0x210	PLL/DRV Setting 4
HDMI_HPD_CEC	0x214	PLL/DRV Setting 5
HDMI_SPD_PKT	0x240	SPD packet
HDMI_PKT_CTRL0	0x2f0	PACKET_CONTROL0
HDMI_PKT_CTRL1	0x2f4	PACKET_CONTROL1
HDMI_AUD_TX_FIFO	0x400	Audio Normal DMA Port
HDMI_DDC_CTRL	0x500	DDC Control Register
HDMI_DDC_EXREG	0x504	DDC Extended Register
HDMI_DDC_COMMAND	0x508	DDC Access Command Register
HDMI_DDC_SLAVE_ADDR	0x50C	DDC Slave Address Register
HDMI_DDC_INT_MASK	0x510	DDC Interrupt Mask Register

HDMI_DDC_INT_STATUS	0x514	DDC Interrupt Status Register
HDMI_DDC_FIFO_CTRL	0x518	DDC FIFO Control Register
HDMI_DDC_FIFO_STATUS	0x51C	DDC FIFO Status Register
HDMI_DDC_CLOCK	0x520	DDC Clock Register
HDMI_DDC_TIMOUT	0x524	DDC Timeout Register
HDMI_DDC_DBG	0x540	DDC Slave Address Register
HDMI_DDC_FIFO_ACCESS	0X580	DDC FIFO Access Register

7.5.4. HDMI REGISTER DESCRIPTION

7.5.4.1. HDMI VERSION ID:

Offset: 0x000			**Register name:** HDMI_VERSION_ID
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R	0x0001	VER_ID_H Version number of the core
15:0	R	0x0003	VER_ID_L Version number of the core

7.5.4.2. SYSTEM CONTROL REGISTER:

Offset: 0x004			**Register name:** HDMI_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0	MODULE_EN 0:disable 1:enable
30	R/W	0	HDCP_EN: 0:disable 1:reserved
29:2	/	/	reserved

1	R/W	0	CLR_AVMUTE: General control packet Clear_AVMUTE flag
0	R/W	0	SET_AVMUTE: General control packet Set_AVMUTE flag

7.5.4.3. INTERRUPT STATUS REGISTER:

Offset: 0x008			Register name: HDMI_INT_STATUS
Bits	**Read /Write**	**Default /Hex**	**Description**
31:23	/	/	reserved
22	R/W	0	AUD_FIFO_UNDER_FLOW_MASK 0: interrupt disable 1: interrupt enable
21	R/W	0	AUD_FIFO_OVER_FLOW_MASK 0: interrupt disable 1: interrupt enable
20	R/W	0	AUD_TRANS_BUSY_MASK 0: interrupt disable 1: interrupt enable
19:18	/	/	reserved
17	R/W	0	VID_FIFO_OVER_FLOW_MASK 0: interrupt disable 1: interrupt enable
16	R/W	0	VID_FIFO_UNDER_FLOW_MASK 0: interrupt disable 1: interrupt enable
15:7	/	/	reserved
6	R/Clear	0	AUD_FIFO_UNDER_FLOW Audio input fifo under flow flag

			0: normal 1: under flow happen
5	R/Clear	0	AUD_FIFO_OVER_FLOW Audio input fifo over flow flag 0: normal 1: over flow happen
4	R/Clear	0	AUD_TRANS_BUSY Audio output transmit flag 0: audio data are transmitted as request 1: audio data are not transmitted as request
3:2	/	/	reserved
1	R/Clear	0	VID_FIFO_OVER_FLOW Video input fifo over flow flag 0: normal 1: over flow happen
0	R/Clear	0	VID_FIFO_UNDER_FLOW Video input fifo under flow flag 0: normal 1: under flow happen

7.5.4.4. HOT PLUG REGISTER

Offset: 0x00c			Register name: HDMI_HPD
Bits	**Read /Write**	**Default /Hex**	**Description**
31:16	/	/	reserved
15	R	/	RX_ACTIVE_SENSE_TX2P 1: RX pull high 0: RX pull low
14	R	/	RX_ACTIVE_SENSE_TX2N

			1: RX pull high 0: RX pull low
13	R	/	RX_ACTIVE_SENSE_TX1P 1: RX pull high 0: RX pull low
12	R	/	RX_ACTIVE_SENSE_TX1N 1: RX pull high 0: RX pull low
11	R	/	RX_ACTIVE_SENSE_TX0P 1: RX pull high 0: RX pull low
10	R	/	RX_ACTIVE_SENSE_TX0N 1: RX pull high 0: RX pull low
9	R	/	RX_ACTIVE_SENSE_TXCP 1: RX pull high 0: RX pull low
8	R	/	RX_ACTIVE_SENSE_TXCN 1: RX pull high 0: RX pull low
7:1	/	/	Reserved
0	R	0	HOTPLUG_DET 1: HPD Detect high 0: HPD Detect low

7.5.4.5. VIDEO CONTROL REGISTER:

Offset: 0x010			Register name: HDMI_VID_CTRL
Bits	**Read**	**Default**	**Description**

	/Write	/Hex	
31	R/W	0	VID_EN 0:Video module disable 1:Video module operating
30	R/W	0	HDMI_MODE: 0:DVI 1:HDMI
29:6	/	/	reserved
5	R/W	0	VID_SRC_SEL 0: Video data from RGB inputs 1: Video data from embedded ColorBar Generator
4	R/W	0	VID_OUTPUT_FMT: video output format 0: progress 1: interlace
3:2	R/W	00	VID_COLOR_MODE: video output color mode 00: 24-bit RGB 01: 30-bit RGB 10: 36-bit RGB 11: 48-bit RGB
1:0	R/W	00	VID_REPEATER_SEL: pixel repeater selection 00: normal 01: 2X 10: 4X 11: reserved

7.5.4.6. VIDEO TIMING REGISTER0:

Offset: 0x014			Register name: HDMI_VID_TIMING_0
Bits	Read /Write	Default /Hex	Description
31:28	/	/	reserved
27:16	R/W	0	VID_ACT_V: Video active vertical resolution is : VID_ACT_V+1 pixels
15:12	/	/	reserved
11:0	R/W	0	VID_ACT_H: Video active horizontal resolution is: VID_ACT_H+1 pixels

7.5.4.7. VIDEO TIMING REGISTER1:

Offset: 0x018			Register name: HDMI_VID_TIMING_1
Bits	Read /Write	Default /Hex	Description
31:28	/	/	reserved
27:16	R/W	0	VID_VBP: Vertical back porch is VID_VBP+1 TMDS clock
15:12	/	/	reserved
11:0	R/W	0	VID_HBP: Horizontal back porch is: VID_HBP+1 TMDS clock

7.5.4.8. VIDEO TIMING REGISTER2:

Offset: 0x01c			Register name: HDMI_VID_TIMING_2
Bits	Read	Default	Description

	/Write	/Hex	
31:28	/	/	reserved
27:16	R/W	0	VID_VFP: Vertical front porch is: VID_VFP+1 TMDS clock
15:12	/	/	reserved
11:0	R/W	0	VID_HFP: Horizontal front porch is: VID_HFP+1 TMDS clock

7.5.4.9. VIDEO TIMING REGISTER3:

Offset: 0x020			Register name: HDMI_VID_TIMING_3
Bits	**Read /Write**	**Default /Hex**	**Description**
31:28	/	/	reserved
27:16	R/W	0	VID_VSPW: Vertical sync plus width is: VID_VSPW+1 TMDS clock
15:12	/	/	reserved
11:0	R/W	0	VID_HSPW: Horizontal sync plus width is: VID_HSPW+1 TMDS clock

7.5.4.10. VIDEO TIMING REGISTER4:

Offset: 0x024			Register name: HDMI_VID_TIMING_4
Bits	**Read /Write**	**Default /Hex**	**Description**
31:26	/	/	reserved

25:16	R/W	0	TX_CLOCK Note: normal 10'b11_1110_0000
15:2	/	/	reserved
1	R/W	0	VID_VSYNC_ACTIVE_SEL: Vsync priority selection 0: active low 1: active high
0	R/W	0	VID_HSYNC_ACTIVE_SEL: Hsync priority selection 0: active low 1: active high

7.5.4.11. AUDIO CONTROL REGISTER:

Offset: 0x040			Register name: HDMI_AUD_CTRL
Bits	**Read /Write**	**Default /Hex**	**Description**
31	R/W	0	AUD_EN: 0:disable 1:enable Audio module enable
30	R/W	0	AUD_RST: 0: normal 1: reset Audio module soft reset Write 1 to reset Audio module, and automatically clear to 0 after reset. Write 0 to this bit has no effect.

			Note: before change the audio parameters, first disable the AUD_EN, then write 1 to AUD_RST to reset the audio module, when this reset bit return to 0, then configure the parameters and enable the AUD_EN.
29:0	/	/	reserved

7.5.4.12. AUDIO DMA&FIFO CONTROL REGISTER:

Offset: 0x044			Register name: HDMI_ADMA_CTRL
Bits	**Read /Write**	**Default /Hex**	**Description**
31	R/W	0	AUD_SRC_DMA_MODE 0: dedicated DMA 1: normal DMA
30:26	/	/	Reserved
25:24	R/W	0	DMA_REQ_CRTL 00: 1/2 FIFO empty 01: 1/4 FIFO empty 10: 1/8 FIFO empty 11: reserved
23:20	/	/	Reserved
19	R/W	0	AUD_SRC_DMA_SAMPLE_RATE: 0: 2 sample per transfer(only AUD_SRC_WORD_LEN = 00) 1: 1 sample per transfer
18	R/W	0	AUD_SRC SAMPLE_LAYOUT 0: LSB Align 1: MSB Align
17:16	R/W	0	AUD_SRC_WORD_LEN: 00: 16-bit 01: 20-bit 10: 24-bit

			11: reserved
15	R/W	0	AUD_FIFO_CLEAR: AUD_FIFO_FLUSH_EN 0:normal 1:clear the audio input FIFO
14:1	/	/	Reserved
0	R/W	0	**A**UD_DATA_SEL: 0: last sample 1: all 0's Audio data to send when FIFO is underflow

7.5.4.13. AUDIO FORMAT CONTROL REGISTER:

Offset: 0x048			Register name: HDMI_AUD_FMT
Bits	**Read /Write**	**Default /Hex**	**Description**
31	R/W	0	AUD_SRC_SEL 0: Audio data from DMA inputs 1: Audio data from embedded Audio Signal Generator Note: DMA input should be 32bit wide
30:27	/	/	reserved
26:24	R/W	0	AUD_FMT_SEL Audio format selection 000: liner PCM 001: IEC61937 compress formats 010: HBR audio 011: one bit audio 1xx: reserved
23:5	/	/	Reserved

4	R/W	0	DSD_FMT 0: LSB first 1:MSB first
3	R/W	0	AUD_LAYOUT PCM/1-bit Audio layout selection 0: layout 0（2 channels） 1: layout 1（up to 8 channels）
2:0	R/W	0	PCM_SRC_CH_CFG Source pcm/1-bit audio configuration 000: 1channel 001: 2 channel 010: 3 channel 011: 4 channel 100: 5 channel 101: 6 channel 110: 7 channel 111: 8 channel Note: 1. For LPCM & One Bit Audio 2. This only indicates how many channels of input PCM stream; it does not mean the sink can accept it. So the source should check the CA field of the audio info-frame to decide which channel will be output.

7.5.4.14. AUDIO PCM CONTROL REGISTER:

Offset: 0x04c			Register name: HDMI_AUD_PCM_CTRL
Bits	**Read /Write**	**Default /Hex**	**Description**
31	/	/	Reserved

30:28	R/W	7	PCM_CH7_MAP 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample
27	/	/	reserved
26:24	R/W	6	PCM_CH6_MAP 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample
23	/	/	Reserved
22:20	R/W	5	PCM_CH5_MAP 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample

19	/	/	Reserved
18:16	R/W	4	PCM_CH4_MAP 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample
15	/	/	Reserved
14:12	R/W	3	PCM_CH3_MAP 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample
11	/	/	Reserved
10:8	R/W	2	PCM_CH2_MAP 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample

			111: 8th sample
7	/	/	Reserved
6:4	R/W	1	PCM_CH1_MAP 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample
3	/	/	Reserved
2:0	R/W	0	PCM_CH0_MAP 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample

7.5.4.15. AUDIO CTS REGISTER:

Offset: 0x050			Register name: HDMI_AUD_CTS
Bits	**Read /Write**	**Default /Hex**	**Description**
31:20	/	/	reserved
19:0	R/W	0	AUDIO_CLK_GEN_CTS Audio clock regeneration factor CTS

7.5.4.16. AUDIO N REGISTER:

Offset: 0x054			Register name: HDMI_AUD_N
Bits	Read /Write	Default /Hex	Description
31:20	/	/	reserved
19:0	R/W	0	AUD_CLK_GEN_N Audio clock regeneration factor N

7.5.4.17. AUDIO PCM CHANNEL STATUS 0:

Offset: 0x058			Register name: HDMI_AUD_CH_STATUS0
Bits	Read /Write	Default /Hex	Description
31:30	R/W	0x00	CHNL_BIT1 (reserved)
29:28	R/W	0x00	CLK_ACCUR: Clock accuracy tolerance
27:24	R/W	0x00	FS_FREQ: Sampling frequency setting 0000 = 44.1 KHz 0010 = 48 KHz 0011 = 32 KHz 1000 = 88.2 KHz 1010 = 96 KHz 1100 =176.4 KHz 1110 = 192 KHz others = reserved
23:20	R/W	0x00	CH_NUM

			Channel number
19:16	R/W	0x00	SOURCE_NUM Source number
15:8	R/W	0x00	CATEGORY CODE Category code
7:6	R/W	0x00	MODE 00: Default Mode 01~11: Reserved
5:3	R/W	0x00	EMPHASIS Additional format information For bit 1 = “0”, Linear PCM audio mode: 000: 2 audio channels without pre-emphasis 001: 2 audio channels with 50 μs / 15 μs pre-emphasis 010: Reserved (for 2 audio channels with pre-emphasis) 011: Reserved (for 2 audio channels with pre-emphasis) 100~111: Reserved For bit 1 = “1”, other than Linear PCM applications: 000: Default state 001~111: Reseved
2	R/W	0x00	CP Copyright 0: copyright is asserted 1: no copyright is asserted
1	R/W	0x00	AUD_DATA_TYPE Audio Data Type 0: Linear PCM Samples 1: For none-linear PCM audio such as AC3, DTS, MPEG audio
0	R/W	0x00	APP_TYPE Application type

			0: Consumer Application 1: Professional Application Note: This bit must be fixed to “0”

7.5.4.18. AUDIO PCM CHANNEL STATUS 1:

Offset: 0x05c			Register name: HDMI_AUD_CH_STATUS1
Bits	**Read /Write**	**Default /Hex**	**Description**
31:10	/	/	Reserved
9:8	R/W	0x00	CGMS_A 00: Copying is permitted without restriction 01: One generation of copies may be made 10: Condition not be used 11: No copying is permitted
7:4	R/W	0x00	ORIGINAL_FS Original sampling frequency 0000: not indicated 0001: 192kHz 0010: 12kHz 0011: 176.4kHz 0100: Reserved 0101: 96kHz 0110: 8kHz 0111: 88.2kHz 1000: 16kHz 1001: 24kHz 1010: 11.025kHz 1011: 22.05kHz 1100: 32kHz

			1101: 48kHz 1110: Reserved 1111: 44.1kHz
3:1	R/W	0x00	WORD_LEN Sample word length For bit 0 = “0”: 000: not indicated 001: 16 bits 010: 18 bits 100: 19 bits 101: 20 bits 110: 17 bits 111: Reserved For bit 0 = “1”: 000: not indicated 001: 20 bits 010: 22 bits 100: 23 bits 101: 24 bits 110: 21 bits
0	R/W	0x00	WORD_LEN_MAX Max word length 0: Maximum audio sample word length is 20 bits 1: Maximum audio sample word length is 24 bits

Notes:

Channel status is 192-bit, bits that not list above should set to 0

7.5.4.19. AVI_INFO_FRMAE_PACKET:

Offset: 0x080			Register name: HDMI_AVI_INFO_PKT
BYTE	Read /Write	Default /Hex	Description
0x00	R/W	0x00	AVI_HB0 Packet type
0x01	R/W	0x00	AVI_HB1 Packet version
0x02	R/W	0x00	AVI_HB2 Packet length
0x03	R/W	0x00	AVI_PB0 checksum
0x04	R/W	0x00	AVI_PB1 AVI data byte 1
0x05	R/W	0x00	AVI_PB2 AVI data byte 2
0x06	R/W	0x00	AVI_PB3 AVI data byte 3
0x07	R/W	0x00	AVI_PB4 AVI data byte 4
0x08	R/W	0x00	AVI_PB5 AVI data byte 5
0x09	R/W	0x00	AVI_PB6 AVI data byte 6
0x0a	R/W	0x00	AVI_PB7 AVI data byte 7
0x0b	R/W	0x00	AVI_PB8 AVI data byte 8
0x0c	R/W	0x00	AVI_PB9

			AVI data byte 9
0x0d	R/W	0x00	AVI_PB10 AVI data byte 10
0x0e	R/W	0x00	AVI_PB11 AVI data byte 11
0x0f	R/W	0x00	AVI_PB12 AVI data byte 12
0x10	R/W	0x00	AVI_PB13 AVI data byte 13

7.5.4.20. AUDIO_INFO_FRMAE_PACKET:

Offset: 0x0a0			**Register name: HDMI_AUD_INFO_PKT**
BYTE	**Read /Write**	**Default /Hex**	**Description**
0x00	R/W	0x00	**AUD_HB0** Packet type
0x01	R/W	0x00	**AUD_HB1** Packet version
0x02	R/W	0x00	**AUD_HB2** Packet length
0x03	R/W	0x00	**AUD_PB0** checksum
0x04	R/W	0x00	**AUD_PB1** AUD data byte 1
0x05	R/W	0x00	**AUD_PB2** AUD data byte 2
0x06	R/W	0x00	**AUD_PB3** AUD data byte 3
0x07	R/W	0x00	**AUD_PB4**

			AUD data byte 4
0x08	R/W	0x00	**AUD_PB5** AUD data byte 5
0x09	R/W	0x00	**AUD_PB6** AUD data byte 6
0x0a	R/W	0x00	**AUD_PB7** AUD data byte 7
0x0b	R/W	0x00	**AUD_PB8** AUD data byte 8
0x0c	R/W	0x00	**AUD_PB9** AUD data byte 9
0x0d	R/W	0x00	**AUD_PB10** AUD data byte 10

7.5.4.21. ACP_PACKET:

Offset: 0x0c0			**Register name: HDMI_ACP_PKT**
BYTE	**Read /Write**	**Default /Hex**	**Description**
0x00	R/W	0x00	ACP_HB1 ACP_Type
0x01	R/W	0x00	ACP_HB2 Reseved
0x02	R/W	0x00	ACP_PB0
0x03	R/W	0x00	ACP_PB1
0x04	R/W	0x00	ACP_PB2
0x05	R/W	0x00	ACP_PB3
0x06	R/W	0x00	ACP_PB4
0x07	R/W	0x00	ACP_PB5
0x08	R/W	0x00	ACP_PB6

0x09	R/W	0x00	ACP_PB7
0x0a	R/W	0x00	ACP_PB8
0x0b	R/W	0x00	ACP_PB9
0x0c	R/W	0x00	ACP_PB10
0x0d	R/W	0x00	ACP_PB11
0x0e	R/W	0x00	ACP_PB12
0x0f	R/W	0x00	ACP_PB13
0x10	R/W	0x00	ACP_PB14
0x11	R/W	0x00	ACP_PB15
0x12	R/W	0x00	ACP_EN 0: disable ACP packet TX 1: enable ACP packet TX

7.5.4.22. GENERAL_CONTROL_PACKET:

Offset: 0x0e0			Register name: HDMI_GP_PKT
BYTE	**Read /Write**	**Default /Hex**	**Description**
0x00	R/W	0x00	GCP_HB0 Packet type
0x01	R/W	0x00	GCP _HB1 Packet version
0x02	R/W	0x00	GCP _HB2 Packet length
0x03	R/W	0x00	GCP _PB0
0x04	R/W	0x00	GCP _PB1
0x05	R/W	0x00	GCP _PB2
0x06	R/W	0x00	GCP _PB3
0x07	R/W	0x00	GCP _PB4
0x08	R/W	0x00	GCP _PB5

0x09	R/W	0x00	GCP _PB6

7.5.4.23. SPD_PACKET

Offset: 0x240			Register name: HDMI_SPD_PKT
BYTE	Read /Write	Default /Hex	Description
0x00	R/W	0x00	DATA_HB1
0x01	R/W	0x00	USER_HB2
0x02	R/W	0x00	USER_HB3
0x03	R/W	0x00	USER_PB0
0x04	R/W	0x00	USER_PB1
0x05	R/W	0x00	USER_PB2
0x06	R/W	0x00	USER_PB3
0x07	R/W	0x00	USER_PB4
0x08	R/W	0x00	USER_PB5
0x09	R/W	0x00	USER_PB6
0x0a	R/W	0x00	USER_PB7
0x0b	R/W	0x00	USER_PB8
0x0c	R/W	0x00	USER_PB9
0x0d	R/W	0x00	USER_PB10
0x0e	R/W	0x00	USER_PB11
0x0f	R/W	0x00	USER_PB12
0x10	R/W	0x00	USER_PB13
0x11	R/W	0x00	USER_PB14
0x12	R/W	0x00	USER_PB15
0x13	R/W	0x00	USER_PB16
0x14	R/W	0x00	USER_PB17
0x15	R/W	0x00	USER_PB18
0x16	R/W	0x00	USER_PB19

0x17	R/W	0x00	USER_PB20
0x18	R/W	0x00	USER_PB21
0x19	R/W	0x00	USER_PB22
0x1a	R/W	0x00	USER_PB23
0x1b	R/W	0x00	USER_PB24
0x1c	R/W	0x00	USER_PB25
0x1d	R/W	0x00	USER_PB26
0x1e	R/W	0x00	USER_PB27

7.5.4.24. PLL/DRV SETTING 0: PAD CTRL0

Offset: 0x200			Register name: HDMI_PAD_CTRL0
Bits	**Read /Write**	**Default /Hex**	**Description**
31	R/W	0	BIASEN
30	R/W	0	LDOCEN
29	R/W	0	LDODEN
28	R/W	0	PWENC
27	R/W	0	PWEND
26	/	/	/
25	R/W	0	CKEN
24	R/W	0	SEN
23	R/W	0	TXEN
22	R/W	0	Autosync_dis 0: enable auto sync 1:
21	R/W	0	LSB_MSB
20:0	/	/	reserved

7.5.4.25. PLL/DRV SETTING 1: PAD CTRL1

Offset: 0x204			Register name: HDMI_PAD_CTRL1
Bits	Read /Write	Default /Hex	Description
31:24	/	/	reserved
23	R/W	0	AMP_OPT
22	R/W	0	AMPCK_OPT
21	R/W	0	DMPOPT
20	R/W	0	EMP_OPT
19	R/W	0	EMPCK_OPT
18	R/W	0	PWSCK
17	R/W	0	PWSDT
16	R/W	0	REG_CSMPS
15	R/W	0	REG_DEN
14	R/W	0	REG_DENCK
13	R/W	0	REG_PLRCK
12:10	R/W	0	REG_EMP
9:8	R/W	0	REG_CD
7:6	R/W	0	REG_CKSS
5:3	R/W	0	REG_AMP
2:0	R/W	0	REG_PLR

7.5.4.26. PLL/DRV SETTING 2: PLL CTRL0

Offset: 0x208			Register name: HDMI_PLL_CTRL
Bits	Read /Write	Default /Hex	Description
31	R/W	0	PLL_EN
30	R/W	0	BWS
29	R/W	0	HV_IS_33

28	R/W	0	LDO1_EN
27	R/W	0	LDO2_EN
26	R/W	0	S6P25_7P5
25	R/W	0	SDIV2
24	R/W	0	SINT_FRAC
23	R/W	0	VCO_GAIN_EN
22:20	R/W	0	VCO_GAIN
19:17	R/W	0	S
16:12	R/W	0	CP_S
11:8	R/W	0	CS
7:4	R/W	0	PREDIV
3:0	R/W	0	VCO_S

7.5.4.27. PLL/DRV SETTING 3: PLL DBG0

Offset: 0x20c			Register name: HDMI_PLL_DBG0
Bits	**Read /Write**	**Default /Hex**	**Description**
31	R/W	0	PLL_DBG_EN
30:28	R/W	0	PSET
27:26	R/W	0	CLKSTEP
25:24	R/W	0	PDCLKSEL
23	R/W	0	S5_7
22	R/W	0	/
21	R/W	0	CKIN_SEL
20	R/W	0	VCO_RST_IN
19	R/W	0	VREG2_OUT_EN
18	R/W	0	VREG1_OUT_EN
17	R/W	0	REG_OD1
16	R/W	0	REG_OD

15:14	/	/	reserved
13:8	R/W	0	B_IN
7:6	/	/	reserved
5:0	R/W	0	CNT_INT

7.5.4.28. PLL/DRV SETTING 4: PLL DBG0

Offset: 0x210			Register name: HDMI_PLL_DBG1
Bits	**Read /Write**	**Default /Hex**	**Description**
31:25	/	/	reserved
24	R/W	0	LOCK_FLAG2
23:17	/	/	reserved
16	R/W	0	LOCK_FLAG1
15:10	/	/	reserved
9	R/W	0	ERROR_SF
8	R/W	0	ERROR_SFDET
7:6	/	/	reserved
5:0	R/W	0	PLL_BNSI

7.5.4.29. PLL/DRV SETTING 5: HPD/CEC

Offset: 0x214			Register name: HDMI_HPD_CEC
Bits	**Read /Write**	**Default /Hex**	**Description**
31:12	/	/	reserved
11	R/W	0	REG_CEC_EN
10	R/W	0	REG_CECPS
9	R/W	0	W_CEC
8	R	/	R_CEC
7:4	/	/	reserved

3	R/W	0	REG_HPD_EN
2	R/W	0	REG_HPDPD
1	R/W	0	W_HPD
0	R	/	R_HPD

7.5.4.30. PACKET_CONTROL0

Offset: 0x2f0			Register name: HDMI_PKT_CTRL0
Bits	**Read /Write**	**Default /Hex**	**Description**
31:28	R/W	0	PKT_4_FREQ 0: 1 1: 2 2: 4 3: 8 4: 16 5: 32 6: 64 7: 128 Others: reserved Note: unit: frame
27:24	R/W	0	PKT_3_FREQ 0: 1 1: 2 2: 4 3: 8 4: 16 5: 32 6: 64 7: 128

			Others: reserved Note: unit: frame
23:20	R/W	0	PKT_2_FREQ 0: 1 1: 2 2: 4 3: 8 4: 16 5: 32 6: 64 7: 128 Others: reserved Note: unit: frame
19:16	R/W	0	PKT_1_FREQ 0: 1 1: 2 2: 4 3: 8 4: 16 5: 32 6: 64 7: 128 Others: reserved Note: unit: frame
15:12	R/W	0	PKT_4 0: NULL packet 1: gc_packet 2: avi_infoframe 3: audio_infoframe

			4: audio_related 5: spd_infoframe 6: user_define(reserved) 7: acp_pkt(reserved) 8: mpeg_info(reserved) 15:arbiter table end Others: reserved
11:8	R/W	0	PKT_3 0: NULL packet 1: gc_packet 2: avi_infoframe 3: audio_infoframe 4: audio_related 5: spd_infoframe 6: user_define(reserved) 7: acp_pkt(reserved) 8: mpeg_info(reserved) 15:arbiter table end Others: reserved
7:4	R/W	0	PKT_2 0: NULL packet 1: gc_packet 2: avi_infoframe 3: audio_infoframe 4: audio_related 5: spd_infoframe 6: user_define(reserved) 7: acp_pkt(reserved) 8: mpeg_info(reserved)

			15:arbiter table end Others: reserved
3:0	R/W	0	PKT_1 0: NULL packet 1: gc_packet 2: avi_infoframe 3: audio_infoframe 4: audio_related 5: spd_infoframe 6: user_define(reserved) 7: acp_pkt(reserved) 8: mpeg_info(reserved) 15:arbiter table end Others: reserved

7.5.4.31. PACKET CONTROL1

Offset address: 0x2f4			Register name: HDMI_PKT_CTRL1
Bits	**Read /Write**	**Default /Hex**	**Description**
31:28	R/W	0	PKT_8_FREQ 0: 1 1: 2 2: 4 3: 8 4: 16 5: 32 6: 64 7: 128 Others: reserved

			Note: unit: frame
27:24	R/W	0	PKT_7_FREQ 0: 1 1: 2 2: 4 3: 8 4: 16 5: 32 6: 64 7: 128 Others: reserved Note: unit: frame
23:20	R/W	0	PKT_6_FREQ 0: 1 1: 2 2: 4 3: 8 4: 16 5: 32 6: 64 7: 128 Others: reserved Note: unit: frame
19:16	R/W	0	PKT_5_FREQ 0: 1 1: 2 2: 4 3: 8 4: 16

			5: 32 6: 64 7: 128 Others: reserved Note: unit: frame
15:12	R/W	0	PKT_8 0: NULL packet 1: gc_packet 2: avi_infoframe 3: audio_infoframe 4: audio_related 5: spd_infoframe 6: user_define(reserved) 7: acp_pkt(reserved) 8: mpeg_info(reserved) 15:arbiter table end Others: reserved
11:8	R/W	0	PKT_7 0: NULL packet 1: gc_packet 2: avi_infoframe 3: audio_infoframe 4: audio_related 5: spd_infoframe 6: user_define(reserved) 7: acp_pkt(reserved) 8: mpeg_info(reserved) 15:arbiter table end Others: reserved

7:4	R/W	0	PKT_6 0: NULL packet 1: gc_packet 2: avi_infoframe 3: audio_infoframe 4: audio_related 5: spd_infoframe 6: user_define(reserved) 7: acp_pkt(reserved) 8: mpeg_info(reserved) 15:arbiter table end Others: reserved
3:0	R/W	0	PKT_5 0: NULL packet 1: gc_packet 2: avi_infoframe 3: audio_infoframe 4: audio_related 5: spd_infoframe 6: user_define(reserved) 7: acp_pkt(reserved) 8: mpeg_info(reserved) 15:arbiter table end Others: reserved

7.5.4.32. AUDIO NORMAL DMA PORT:

Offset: 0x400			**Register name: HDMI_AUD_TX_FIFO**
Bits	**Read /Write**	**Default /Hex**	**Description**

31:0	W	/	TX_FIFO Audio input FIFO port for normal DMA

Notes: DMA assume that all sample data are organized as 32-bit/sub-frame.

7.5.4.33. DDC CONTROL REGISTER:

Offset address: 0x500			**Register name:** HDMI_DDC_CTRL
Bits	**Read /Write**	**Default /Hex**	**Description**
31	R/W	0	DDC_SW_RST DDC soft reset Write “1” to this bit will clear the DDC controller, and auto clear to “0”when completing soft reset operation, write ‘0’ to this bit has no effect.
30:28	R	0	Reserved
27	R/W	0	DDC_XCH DDC Access Command Start Write “1” to this bit will start the DDC Access Command, and will auto clear when command complete. Write “1” to DDC_SW_RST or disable HDMI module enable will also clear this bit. Write ‘0’ to this bit has no effect.
26:8	R	0	Reserved
7	R/W	0	DDC SDA PAD pull down enable 0：Disable 1：Enable
6	R/W	0	DDC SDA PAD enable 0：Disable 1：Enable

5	R/W	0	DDC SCL PAD pull down enable 0：Disable 1：Enable
4	R/W	0	DDC SCL PAD enable 0：Disable 1：Enable
3:1	R	0	Reserved
0	R/W	0	DDC_EN DDC module enable 0：Disable 1：Enable

7.5.4.34. DDC EXTENDED CONTROL REGISTER:

Offset address: 0x504			**Register name:** HDMI_DDC_EXREG
Bits	**Read /Write**	**Default /Hex**	**Description**
31:11	R	0	Reserved
10	R	0	Bus Busy
9	R	0	SCL status
8	R	0	SDA status
7	R/W	0	Segment select 0: select segment 0 1: select segment 1~n(n>0)
6	R/W	0	Segment 0 detection mode

			0: auto detection 1: decide by segment select
5	R/W	0	Initial sequence mode 0: scl 9 cycle low 1: scl 10 cycle low
4	R/W	0	Initial sequence enable 0：Disable 1：Enable
3	R/W	0	DDC_SW_SCL DDC_SCL line state control bit 0: output low level 1: output high level Note: When DDC_SW_SCL_EN is set to ‘1’, the value of this bit decide the output level of DDC_SCL
2	R/W	0	DDC_SW_SCL_EN DDC_SCL line state control enable 0：Disable 1：Enable
1	R/W	0	DDC_SW_SDA DDC_SDA line state software control bit 0: output low level 1: output high level Note: When DDC_SW_SDA_EN is set to ‘1’, the value of this bit decides the output level of DDC_ SDA.
0	R/W	0	DDC_SW_SDA_EN DDC_SDA line state control enable

			0：Disable 1：Enable

7.5.4.35. DDC ACCESS COMMAND REGISTER

Offset address: 0x508			**Register name:** HDMI_DDC_COMMAND
Bits	**Read /Write**	**Default /Hex**	**Description**
31:26	R	0	Reserved
25:16	R/W	0	DDC_DTC DDC Access Data Byte Number
15:3	R	0	Reserved
2:0	R/W	0	DDC_CMD DDC Access Command 000 = Abort Current Operation 001 = Special Offset Address Read 010 = Explicit Offset Address Write 011 = Implicit Offset Address Write 100 = Explicit Offset Address Read 101 = Implicit Offset Address Read 110 = Explicit Offset Address E-DDC Read 111 = Implicit Offset Address E-DDC Read

7.5.4.36. DDC SLAVE ADDRESS REGISTER:

Offset address: 0x50C			**Register name:** HDMI_DDC_SLAVE_ADDR
Bits	**Read /Write**	**Default /Hex**	**Description**

31:24	R/W	0	SEG_PTR DDC slave segment pointer for E-DDC read operation
23:16	R/W	0	DDC_CMD DDC command slave segment address for E-DDC read operation Note: must be 0x60
15:8	R/W	0	OFF_ADR DDC slave offset address to be sent for non-implicit read、write operation.
7:1	R/W	0	DEV_ADR DDC slave device address Note: must be 0xa0
0	R	0	Reserved

7.5.4.37. DDC INTERRUPT MASK REGISTER:

Offset address: 0x510			**Register name:** HDMI_DDC_INT_MASK
Bits	**Read /Write**	**Default /Hex**	**Description**
31:6	R	0	Reserved
8	R/W	0	DDC_TRANSFER_TIMEOUT_MASK 0：Disable 1：Enable
7	R/W	0	ILLEGAL_FIFO_OP_INT_MASK Illegal FIFO operation interrupt mask 0：Disable 1：Enable
6	R/W	0	RX_FIFO_UF_INT_MASK

			DDC RX FIFO underflow interrupt mask 0：Disable 1：Enable
5	R/W	0	TX_FIFO_OF_INT_MASK DDC TX FIFO overflow interrupt mask 0：Disable 1：Enable
4	R/W	0	FIFO_REQ_INT_MASK DDC FIFO request interrupt enable 0：Disable 1：Enable
3	R/W	0	DDC_ARB_ERR_INT_MASK DDC Arbitration Error Interrupt mask 0：Disable 1：Enable
2	R/W	0	DDC_ACK_ERR_INT_MASK DDC ACK Error Interrupt mask 0：Disable 1：Enable
1	R/W	0	DDC_BUS_ERR_INT_MASK DDC Bus Error Interrupt mask 0：Disable 1：Enable
0	R/W	0	DDC_TC_INT_MASK DDC Transfer Complete Interrupt mask 0：Disable

			1：Enable

7.5.4.38. DDC INTERRUPT STATUS REGISTER:

Offset address: 0x514			Register name: HDMI_DDC_INT_STATUS
Bits	**Read /Write**	**Default /Hex**	**Description**
31:9	R	0	Reserved
8	R/W	0	DDC_TRANSFER_TIMEOUT
7	R/W	0	ILLEGAL_FIFO_OP_INT Illegal FIFO operation interrupt status bit 0: No illegal FIFO operation 1: Illegal FIFO operation happened Note: Write “1” to this bit will clear it.
6	R/W	0	RX_FIFO_UF_INT DDC RX FIFO underflow interrupt status bit 0: not underflow 1: underflow Note: Write “1” to this bit will clear it
5	R/W	0	TX_FIFO_OF_INT DDC TX FIFO overflow interrupt status bit 0: not overflow 1: overflow Note: Write “1” to this bit will clear it
4	R	0	FIFO_REQ_INT DDC FIFO request Interrupt status bit

			0: no FIFO request 1: FIFO request happened Note: This bit is set when TX FIFO level is at or below the TX trigger thresh in write operation, or when RX FIFO level is at or above the RX trigger thresh in read operation。Write “1” to this bit will clear it.
3	R/W	0	DDC_ARB_ERR_INT DDC Arbitration Error Interrupt status bit 0: no arbitration lost 1: arbitration lost happened Write “1” to this bit will clear it
2	R/W	0	DDC_ACK_ERR_INT DDC ACK Error Interrupt status bit 0: no ACK error 1: ACK error happened Note: This bit is set when NAK is received when expect ACK , write “1” to this bit will clear it。
1	R/W	0	DDC_BUS_ERR_INT DDC Bus Error Interrupt status bit 0: no bus error 1: bus error happened Note: Write “1” to this bit will clear it
0	R/W	0	DDC_TC_INT DDC Transfer Complete Interrupt Status bit 0: transfer not complete 1: transfer complete Note: Write “1” to this bit will clear it

7.5.4.39. DDC FIFO CONTROL REGISTER:

Offset address: 0x518			Register name: HDMI_DDC_FIFO_CTRL
Bits	**Read /Write**	**Default /Hex**	**Description**
31:16	R	0	Reserved
15	R/W	0	FIFO_RST FIFO software reset Write '1' to this bit will clear TX and RX FIFO, and auto clear to "0" when completing FIFO reset operation. Write '0' to this bit has no effect. Write "1" to DDC_SW_RST or disable HDMI module enable will also clear this bit.
14:12	R	0	Reserved
11	R/W	0	RX_FIFO_SYS_ACCESS_MASK RX FIFO system access mask 0：Disable 1：Enable Note: Write '1' to this bit will mask the RX FIFO operation from system bus.
10	R/W	0	TX_FIFO_SYS_ACCESS_MASK TX FIFO system access mask 0：Disable 1：Enable Note: Write '1' to this bit will mask the TX FIFO operation from system bus.
9	R	0	Reserved

8	R/W	0	DMA Request Enable 0：Disable 1：Enable
7:4	R/W	0	RX_FIFO_TRIGGER_THRESH When RX FIFO level is above this value in read mode, DMA request and FIFO request interrupt is assert if relative enable is on.
3:0	R/W	0	TX_FIFO_TRIGGER_THRESH When TX FIFO level is at or below this value in write mode, DMA request and FIFO request interrupt is assert if relative enable is on.

7.5.4.40. DDC FIFO STATUS REGISTER:

Offset address: 0x51C			**Register name:** HDMI_DDC_FIFO_STATUS
Bits	**Read /Write**	**Default /Hex**	**Description**
31:17	R	0	Reserved
16	R	0	FIFO Request Ready TX FIFO level is at or below TX_FIFO_TRIGGER_THRESH in write mode or is above RX_FIFO_TRIGGER_THRESH in read mode.
15	R	0	Reserved
14	R	0	RX FIFO FULL
13	R	1	RX FIFO EMPTY
12:8	R	0	RX FIFO LEVEL
7	R	0	Reserved
6	R	0	TX FIFO FULL

5	R	1	TX FIFO EMPTY
4:0	R	0	TX FIFO LEVEL

7.5.4.41. DDC CLOCK REGISTER:

Offset address: 0x520			**Register name:** HDMI_DDC_CLOCK
Bits	**Read /Write**	**Default /Hex**	**Description**
31:7	R	0	Reserved
6:3	R/W	0	M
2:0	R/W	0	N The DDC bus is sampled by the DCC controller at the frequency defined by F_s: $F_s = F_l/(2^N)$ The DDC output frequency is F_m /10: $F_m = F_s/(M+2)$ $F_{OSCL} = F_m/10 = F_l/((2^N)*(M+2)*10)$ Note: F_l is the source clock frequency, which is 24Mhz.

7.5.4.42. DDC TIMEOUT REGISTER:

Offset address: 0x524			**Register name:** HDMI_DDC_TIMOUT
Bits	**Read /Write**	**Default /Hex**	**Description**
31:8	R	0	Reserved
7:0	R/W	0	N (N+1) * 10ms

7.5.4.43. DDC FIFO ACCESS REGISTER:

Offset address: 0x580~0x5FF			Register name: DDC FIFO Access Register
Bits	**Read /Write**	**Default /Hex**	**Description**
31:0	R/W	0	DDC_DIO DDC data FIFO Access Register Write this register will write TX FIFO and read this register will read out the data in RX FIFO. Note: Address 0x580~0x5FF is mapping to FIFO address; operating any address in this range will generate relative operation to FIFO.

7.6. MIPI DSI

7.6.1. OVERVIEW

The MIPI DSI features:

- Comply with MIPI DSI v1.01 and MIPI D-PHY v1.00
- 1/2/3/4 data lane configuration and up to 1Gbps per lane
- Support ECC, CRC generation and EOT package
- Support up to 1920X1200@60fps with 4 data lanes
- Support video mode and command mode
- Support pixel format: RGB888, RGB666, RGB66 packed, and RGB565
- Support MIPI DCS, bidirectional configuration in LP

7.6.2. MIPI DSI DESCRIPTION

7.6.2.1. .ESCAPE ENTRY

Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)
Low-Power Data Transmission	mode	11100001
Ultra-Low Power State	mode	00011110
Undefined-1	mode	10011111
Undefined-2	mode	11011110
Reset-Trigger [Remote Application]	Trigger	01100010
Unknown-3 TE	Trigger	01011101
Unknown-4 ACK	Trigger	00100001
Unknown-5	Trigger	10100000

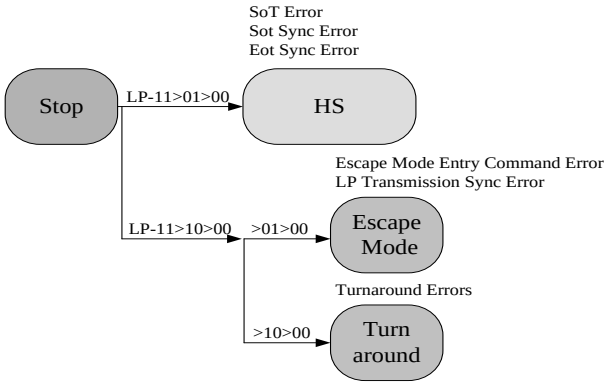


Figure 7-9 False Control Error

7.6.2.2. DATA TYPE

The set of transaction types sent from the host processor to a peripheral are shown below.

Data Types for Processor-sourced Packets

Data Type, hex	Data Type, binary	Description	Packet Size
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short
08h	00 1000	End of Transmission packet (EoTp)	Short
02h	00 0010	Color Mode (CM) Off Command	Short
12h	01 0010	Color Mode (CM) On Command	Short
22h	10 0010	Shut Down Peripheral Command	Short
32h	11 0010	Turn On Peripheral Command	Short
03h	00 0011	Generic Short WRITE, no parameters	Short
13h	01 0011	Generic Short WRITE, 1 parameter	Short
23h	10 0011	Generic Short WRITE, 2 parameters	Short
04h	00 0100	Generic READ, no parameters	Short
14h	01 0100	Generic READ, 1 parameter	Short
24h	10 0100	Generic READ, 2 parameters	Short
05h	00 0101	DCS Short WRITE, no parameters	Short
15h	01 0101	DCS Short WRITE, 1 parameter	Short
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set Maximum Return Packet Size	Short
09h	00 1001	Null Packet, no data	Long
19h	01 1001	Blanking Packet, no data	Long
29h	10 1001	Generic Long Write	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
x0h and xFh, unspecified	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved	

The table below presents the complete set of peripheral-to-processor Data Types.

Data Types for Peripheral-sourced Packets

Data Type, hex	Data Type, binary	Description	Packet Size
00h – 01h	00 000x	Reserved	Short
02h	00 0010	Acknowledge and Error Report	Short
03h – 07h	00 0011 – 00 0111	Reserved	
08h	00 1000	End of Transmission packet (EoTp)	Short
09h – 10h	00 1001 – 01 0000	Reserved	
11h	01 0001	Generic Short READ Response, 1 byte returned	Short
12h	01 0010	Generic Short READ Response, 2 bytes returned	Short
13h – 19h	01 0011 – 01 1001	Reserved	
1Ah	01 1010	Generic Long READ Response	Long
1Bh	01 1011	Reserved	
1Ch	01 1100	DCS Long READ Response	Long
1Dh – 20h	01 1101 – 10 0000	Reserved	
21h	10 0001	DCS Short READ Response, 1 byte returned	Short
22h	10 0010	DCS Short READ Response, 2 bytes returned	Short
23h – 3Fh	10 0011 – 11 1111	Reserved	

Table 7-1 Data Type for Peripheral-to-Processor Data Types

The table below shows the bit assignment for all error reporting.

Error Report Bit Definitions

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	HS Receive Timeout Error
6	False Control Error
7	Reserved
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	Invalid Transmission Length
14	Reserved
15	DSI Protocol Violation

Table 7-2 Error Report Bit Definitions

7.6.2.3. PIXEL FORMAT

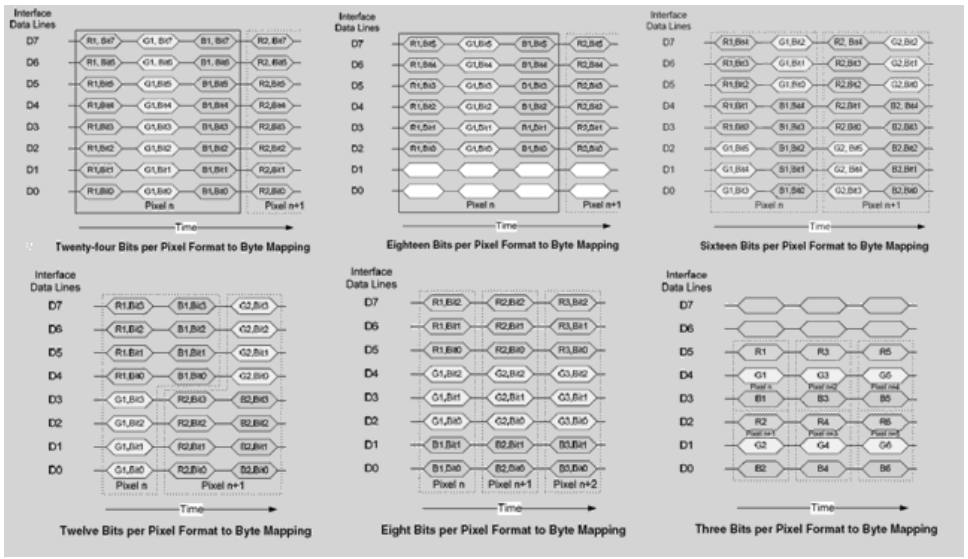


Figure 7-10 Pixel Format (Command mode)）

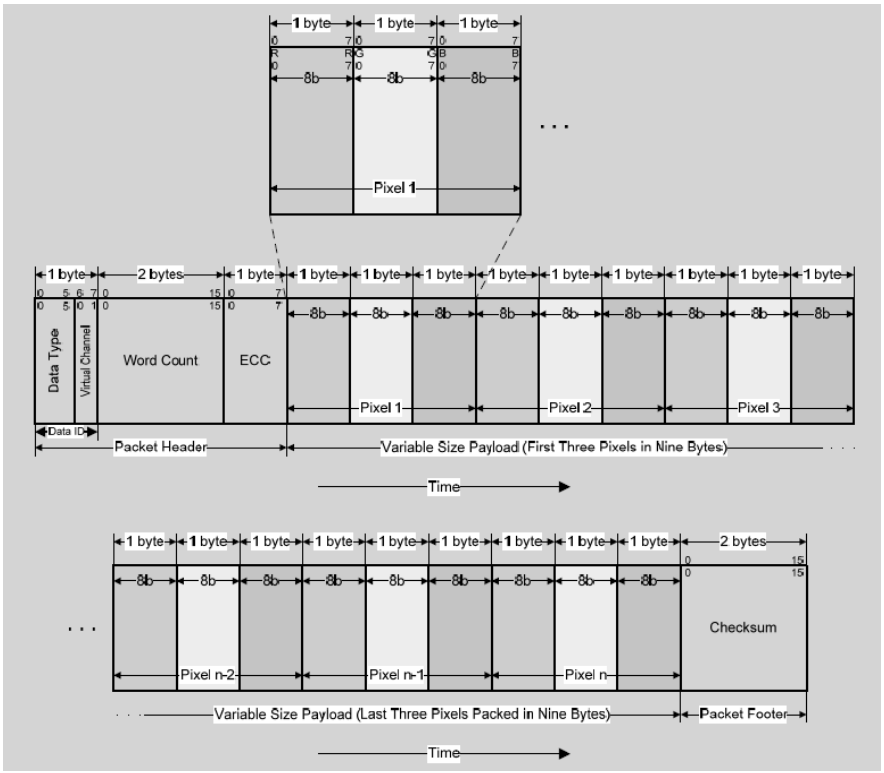


Figure 7-11 24-bit per Pixel-RGB Color Format, Long Packet（(Video mode)）

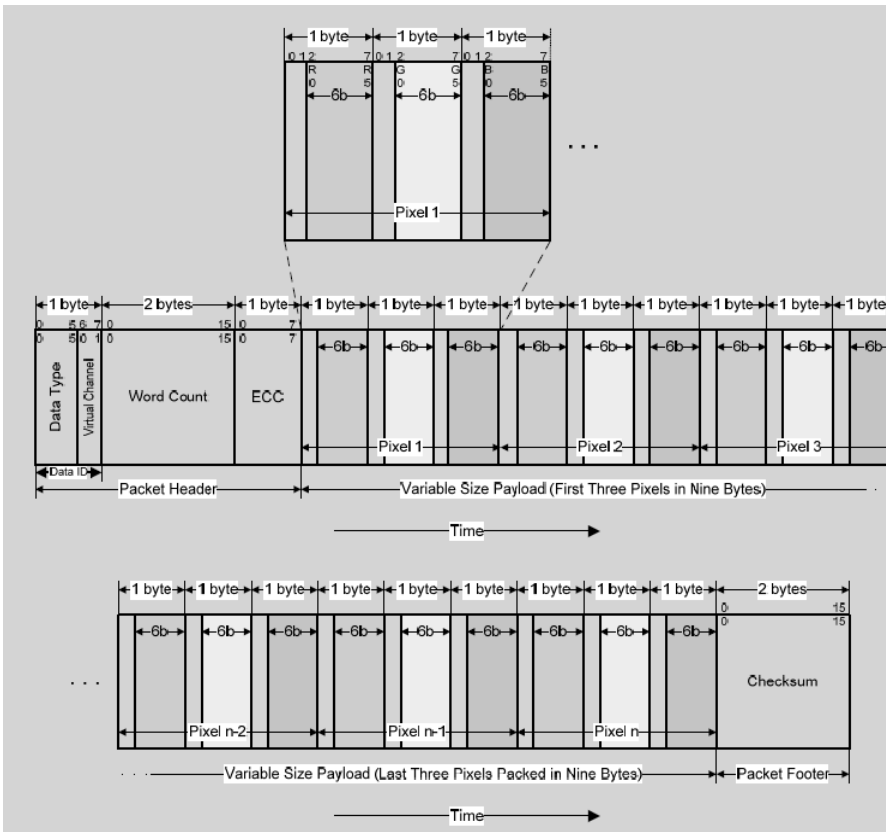


Figure 7-12 18-bit per Pixel (Loosely Packed) – RGB Color Format, Long Packet(Video mode)）

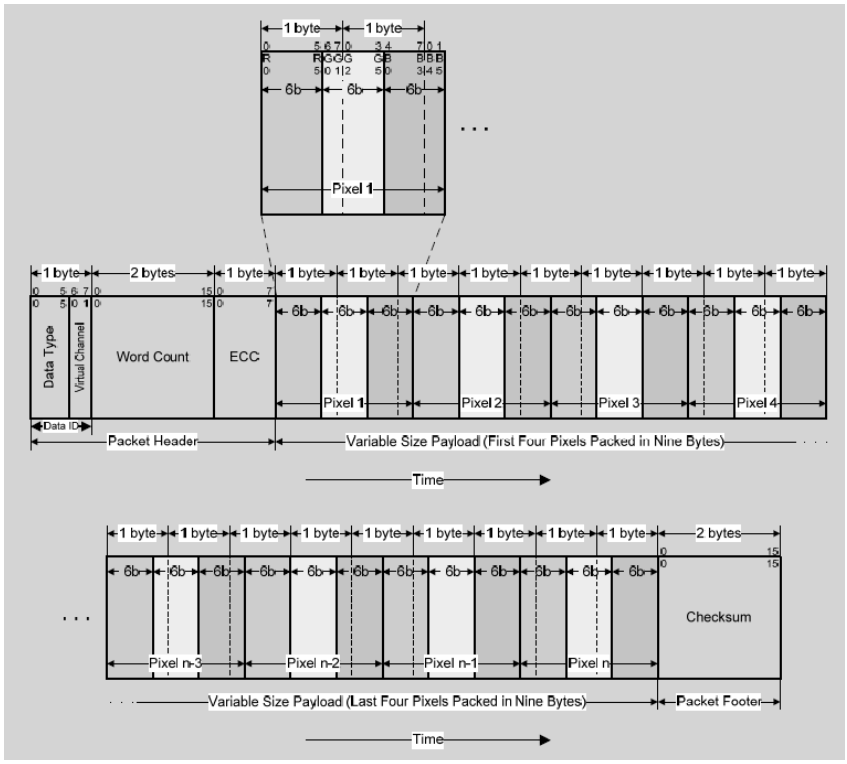


Figure 7-13 18-bit per Pixel (Packed) – RGB Color Format, Long Packet(Video mode)）

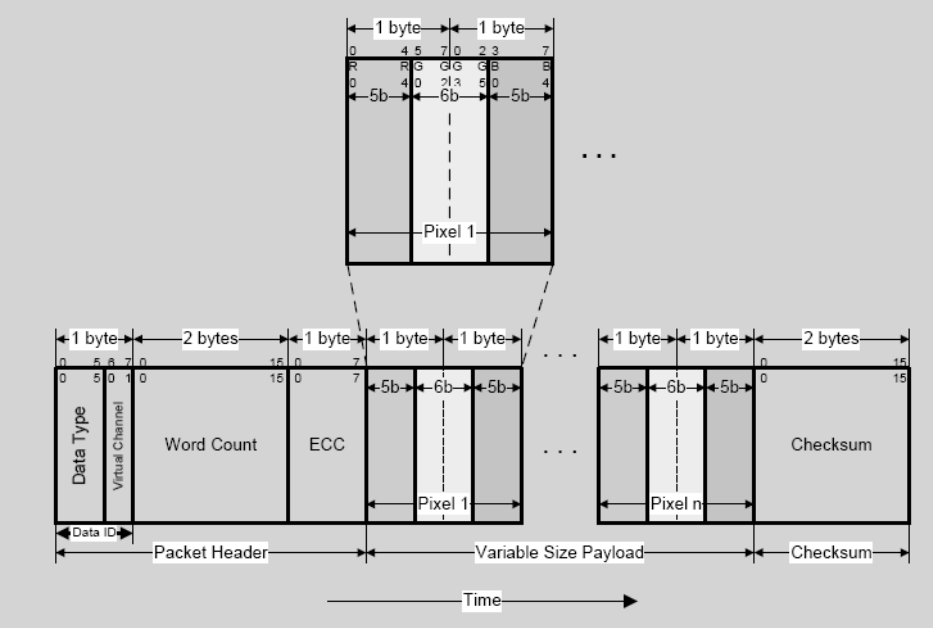
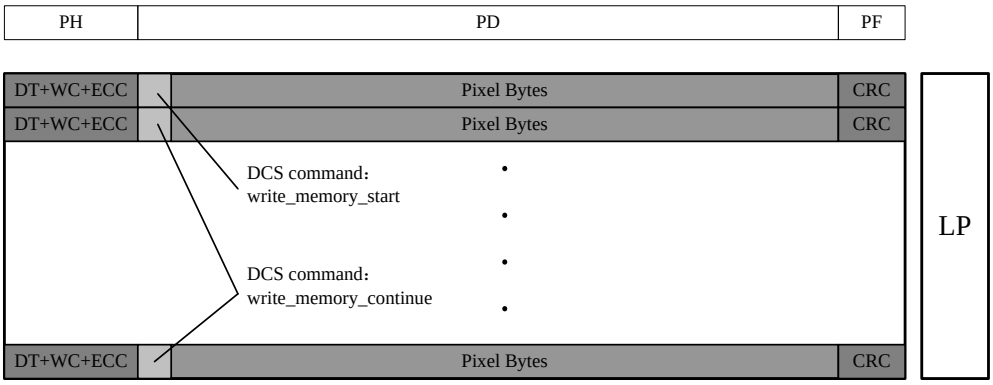


Figure 7-14 16-bit per Pixel – RGB Color Format, Long Packet(Video mode)）

7.6.2.4. COMMAND MODE



DT: DCS Long Write Command Packet

Figure 7-15 Command mode

7.6.2.5. VIDEO MODE

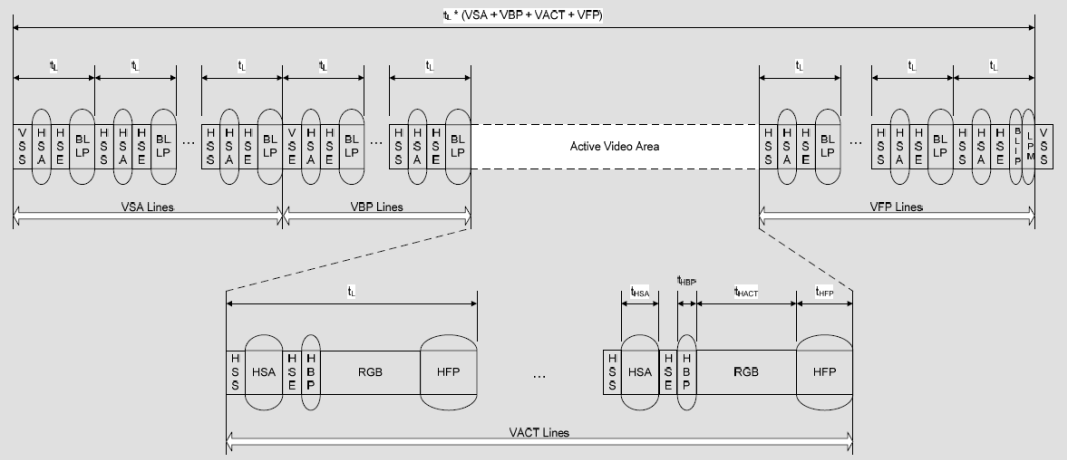


Figure 7-16 Video mode

7.6.3. MIPI DSI REGISTER LIST

Module Name	Base Address
DSI	0x01CA0000

Register Name	Offset	Description
DSI_CTL_REG	0x000	DSI Control Register
DSI_GINT0_REG	0x004	DSI Interrupt Register0
DSI_GINT1_REG	0x008	DSI Interrupt Register1
DSI_BASIC_CTL0_REG	0x010	DSI Configuration Register0
DSI_BASIC_CTL1_REG	0x014	DSI Configuration Register1
DSI_BASIC_SIZE0_REG	0x018	DSI Line Number Register0
DSI_BASIC_SIZE1_REG	0x01c	DSI Line Number Register1
DSI_PIXEL_CTL0_REG	0x080	DSI Pixel Format Register0
DSI_PIXEL_CTL1_REG	0x084	DSI Pixel Format Register1
DSI_PIXEL_PH_REG	0x090	DSI Pixel Package Register0
DSI_PIXEL_PD_REG	0x094	DSI Pixel Package Register1
DSI_PIXEL_PF0_REG	0x098	DSI Pixel Package Register2

DSI_PIXEL_PF1_REG	0x09C	DSI Pixel Package Register3
DSI_SYNC_HSS_REG	0x0B0	DSI Sync Package Register0
DSI_SYNC_HSE_REG	0x0B4	DSI Sync Package Register1
DSI_SYNC_VSS_REG	0x0B8	DSI Sync Package Register2
DSI_SYNC_VSE_REG	0x0BC	DSI Sync Package Register3
DSI_BLK_HSA0_REG	0x0C0	DSI Blank Package Register0
DSI_BLK_HSA1_REG	0x0C4	DSI Blank Package Register1
DSI_BLK_HBP0_REG	0x0C8	DSI Blank Package Register2
DSI_BLK_HBP1_REG	0x0CC	DSI Blank Package Register3
DSI_BLK_HFP0_REG	0x0D0	DSI Blank Package Register4
DSI_BLK_HFP1_REG	0x0D4	DSI Blank Package Register5
DSI_BLK_HBLK0_REG	0x0E0	DSI Blank Package Register6
DSI_BLK_HBLK1_REG	0x0E4	DSI Blank Package Register7
DSI_BLK_VBLK0_REG	0x0E8	DSI Blank Package Register8
DSI_BLK_VBLK1_REG	0x0EC	DSI Blank Package Register9
DSI_CMD_CTL_REG	0x200	DSI LP Control Register
DSI_CMD_RX_REG	0x240+N*0x04(N=0~7)	DSI LP RX Package Register
DSI_CMD_TX_REG	0x300+N*0x04(N=0~63)	DSI LP TX Package Register

7.6.4. MIPI DSI REGISTER DESCRIPTION

7.6.4.1. DSI_CTL_REG

Offset: 0x000			**Register Name: DSI_CTL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	**/**
0	R/W	0	**DSI_En** 0: disable 1: enable

			When it's disabled, the module will be reset to idle state.

7.6.4.2. DSI_GINT0_REG

Offset: 0x004			Register Name: DSI_INT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	**/**
19	R/W	0	**Video_Line_Int_Flag**
18	R/W	0	**Video_Vb_Int_Flag**
17	R/W	0	**Instru_Step_Flag**
16	R/W	0	**Instru_End_Flag**
15:4	/	/	**/**
3	R/W	0	**Video_Line_Int_En** 0: disable 1: enable
2	R/W	0	**Video_Vb_Int_En** 0: disable 1: enable
1	R/W	0	**Instru_Step_En** 0: disable 1: enable
0	R/W	0	**Instru_End_En** 0: disable 1: enable

7.6.4.3. DSI_GINT1_REG

Offset: 0x008			Register Name: DSI_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0	**Video_Line_Int_Num**

7.6.4.4. DSI_BASIC_CTL0_REG

Offset: 0x010			Register Name: DSI_BASIC_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	**/**
28	/	/	**/**
27:18	/	/	**/**
18	R/W	0	**HS_Eotp_En** 0: disable 1: enable enable eotp packet at the end of every HS transmission format: “08h” “0fh” “0fh” “01h”
17	R/W	0	**CRC_En** 0: disable 1: enable
16	R/W	0	**ECC_En** 0: disable 1: enable
15:13	/	/	**/**
12	R/W	0	**FIFO_Gating** 0: disable 1: enable Gating data from TCON, note that TCON data is gating in frame unit.
11	/	/	**/**
10	R/W	0	**FIFO_Manual_Reset** write ‘1’ to reset all correlation FIFO, write’0’ has no effect.
9:6	/	/	**/**
5:4	R/W	0	**Src_Sel**

			00: tcon data 01: test data 1x: reserved write ‘1’ to reset all correlation FIFO, write’0’ has no effect.
3:1	/	/	**/**
0	R/W	0	**Instru_En** 0: disable 1: enable When instruction enable, dsi process from instruction0.

7.6.4.5. DSI_BASIC_CTL1_REG

Offset: 0x014			**Register Name: DSI_BASIC_CTL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	0	**reserved**
11:4	R/W	0	**Video_Start_Delay** delay by lines,only valid in video mode
3	/	/	**/**
2	R/W	0	**Video_Precision_Mode_Align** 0: cut mode 1: fill mode
1	R/W	0	**Video_Frame_Start** 0：normal mode 1：precision mode set ‘0’ start new frame by inst, set ‘1’ start new frame by cntr.
0	R/W	0	**DSI_Mode** 0: command mode 1: video mode in video mode,enable timing define in basic size

7.6.4.6. DSI_BASIC_SIZE0_REG

Offset: 0x018			Register Name: DSI_BASIC_SIZE0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0	**Video_VBP**
15:12	/	/	/
11:0	R/W	0	**Video_VSA**

7.6.4.7. DSI_BASIC_SIZE1_REG

Offset: 0x01C			Register Name: DSI_BASIC_SIZE1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0	**Video_VT**
15:13	/	/	/
11:0	R/W	0	**Video_VACT**

7.6.4.8. DSI_PIXEL_CTL0_REG

Offset: 0x080			Register Name: DSI_PIXEL_CTL0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0	**PD_Plug_Dis** disable PD plug before pixel bytes
15:5	/	/	/
4	R/W	0	**Pixel_Endian** 0: LSB first 1: MSB first

3:0	R/W	0	**Pixel_Format** Command mode 0: 24bit (rgb888) 1: 18bit (rgb666) 2: 16bit (rgb565) 3: 12bit (rgb444) 4: 8bit (rgb332) 5: 3bit (rgb111) Video mode 8: 24bit(rgb888) 9: 18bit(rgb666L) 10: 18bit (rgb666) 11: 16bit(rgb565) others: reserved

7.6.4.9. DSI_PIXEL_CTL1_REG

Offset: 0x084			Register Name: DSI_PIXEL_CTL1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

7.6.4.10. DSI_PIXEL_PH_REG

Offset: 0x090			Register Name: DSI_PIXEL_PH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0	**ECC** only valid when DSI ECC is disable
23:8	R/W	0	**WC** WC is byte numbers of PD in a pixel packet
7:6	R/W	0	**VC** Virtual Channel

5:0	R/W	0	**DT** video mode 24bit, set as “3eh” video mode L18bit, set as “2eh” video mode 18it, set as “1eh” video mode 16bit, set as “0eh” command mode, set as “39h”

7.6.4.11. DSI_PIXEL_PD_REG

Offset: 0x094			Register Name: DSI_PIXEL_PD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	**/**
23:16	R/W	0	**PD_TranN** Used in transmissions except 1st one, set as “3Ch”,only valid when PD_Plug_Dis is set to ‘0’
15:8	/	/	**/**
7:0	R/W	0	**PD_Tran0** Used in 1st transmission, set as “2Ch”, only valid when PD_Plug_Dis is set to ‘0’

7.6.4.12. DSI_PIXEL_PF0_REG

Offset: 0x098			Register Name: DSI_PIXEL_PF0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	**/**
15:0	R/W	0	**CRC_Force** CRC force to this value, this value is only valid when CRC is disable

7.6.4.13. DSI_PIXEL_PF1_REG

Offset: 0x09C	Register Name: DSI_PIXEL_PF1_REG

Bit	Read/Write	Default/Hex	Description
31:16	R/W	0xffff	**CRC_Init_LineN** CRC initial to this value in transmitions except 1st one,only valid when CRC is enable.
15:0	R/W	0xffff	**CRC_Init_Line0** CRC initial to this value in 1st transmition every frame, only valid when CRC is enable.

7.6.4.14. DSI_SYNC_HSS_REG

Offset: 0x0B0			Register Name: DSI_SYNC_HSS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0	**ECC** set as “12h”
23:16	R/W	0	**D1** set as “00h”
15:8	R/W	0	**D0** set as “00h”
7:6	R/W	0	**VC** Virtual Channel
5:0	R/W	0	**DT** HSS, set as “21h”

7.6.4.15. DSI_SYNC_HSE_REG

Offset: 0x0B4			Register Name: DSI_SYNC_HSE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0	**ECC** set as “01h”
23:16	R/W	0	**D1** set as “00h”

15:8	R/W	0	**D0** set as “00h”
7:6	R/W	0	**VC** Virtual Channel
5:0	R/W	0	**DT** HSE, set as “31h”

7.6.4.16. DSI_SYNC_VSS_REG

Offset: 0x0B8			Register Name: DSI_SYNC_VSS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0	**ECC** set as “07h”
23:16	R/W	0	**D1** set as “00h”
15:8	R/W	0	**D0** set as “00h”
7:6	R/W	0	**VC** Virtual Channel
5:0	R/W	0	**DT** VSS, set as “01h”

7.6.4.17. DSI_SYNC_VSE_REG

Offset: 0x0BC			Register Name: DSI_SYNC_VSE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0	**ECC** set as “14h”
23:16	R/W	0	**D1** set as “00h”
15:8	R/W	0	**D0**

			set as “00h”
7:6	R/W	0	**VC** Virtual Channel
5:0	R/W	0	**DT** VSE, set as “11h”

7.6.4.18. DSI_BLK_HSA0_REG

Offset: 0x0C0			Register Name: DSI_BLK_HSA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0	**HSA_PH** Note that bit23:8 is WC,define byte numbers of PD in a blank packet

7.6.4.19. DSI_BLK_HSA1_REG

Offset: 0x0C4			Register Name: DSI_BLK_HSA1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0	**HSA_PF**
15:8	/	/	**/**
7:0	R/W	0	**HSA_PD**

7.6.4.20. DSI_BLK_HBP0_REG

Offset: 0x0C8			Register Name: DSI_BLK_HBP0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0	**HBP_PH** Note that bit23:8 is WC,define byte numbers of PD in a blank packet

7.6.4.21. DSI_BLK_HBP1_REG

Offset: 0x0CC	Register Name: DSI_BLK_HBP1_REG

Bit	Read/Write	Default/Hex	Description
31:16	R/W	0	**HBP_PF**
15:8	/	/	**/**
7:0	R/W	0	**HBP_PD**

7.6.4.22. DSI_BLK_HFP0_REG

Offset: 0x0D0			Register Name: DSI_BLK_HFP0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0	**HFP_PH** Note that bit23:8 is WC,define byte numbers of PD in a blank packet

7.6.4.23. DSI_BLK_HFP1_REG

Offset: 0x0D4			Register Name: DSI_BLK_HFP1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0	**HFP_PF**
15:8	/	/	**/**
7:0	R/W	0	**HFP_PD**

7.6.4.24. DSI_BLK_HBLK0_REG

Offset: 0x0E0			Register Name: DSI_BLK_HBLK0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0	**HBLK_PH** Note that bit23:8 is WC,define byte numbers of PD in a blank packet

7.6.4.25. DSI_BLK_HBLK1_REG

Offset: 0x0E4			Register Name: DSI_HBLK_BLK1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:16	R/W	0	**HBLK_PF**
15:8	/	/	**/**
7:0	R/W	0	**HBLK_PD**

7.6.4.26. DSI_BLK_VBLK0_REG

Offset: 0x0E8			**Register Name: DSI_BLK_VBLK0_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0	**VBLK_PH** Note that bit23:8 is WC,define byte numbers of PD in a blank packet

7.6.4.27. DSI_BLK_VBLK1_REG

Offset: 0x0EC			**Register Name: DSI_BLK_VBLK1_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0	**VBLK_PF**
15:8	/	/	**/**
7:0	R/W	0	**VBLK_PD**

7.6.4.28. DSI_CMD_CTL_REG

Offset: 0x200			**Register Name: DSI_CMD_CTL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	**/**
26	R/W	0	**RX_Overflow** 1: rx data is overflow register buffer Note: Write‘1’ to clear this bit. Write’0’ has no effect.
25	R/W	0	**RX_Flag** 1: rx has happened Note: Write‘1’ to clear this bit. Write’0’ has no effect.
24	R	0	**RX_Status**

			0: rx is finish 1: rx is pending
20:16	R	0	**RX_Size** (RX_Size+1) is number of bytes in the last rx.
15:9	/	/	**/**
9	R/W	0	**TX_Flag** 1: tx has happened Note: Write‘1’ to clear this bit. Write’0’ has no effect.
8	R	0	**TX_Status** 0: tx is finish 1: tx is pending
7:0	R/W	0	**TX_Size** (TX_Size+1) is number of bytes ready to tx

7.6.4.29. DSI_CMD_RX_REG

Offset: 0x240+N*0x04 （N=0,1,2,3,4,5,6,7）			**Register Name: register**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0	**Data** Bit: 31:24 23:16 15:8 7:0 N=0: Byte03 Byte02 Byte01 Byte00 N=1: Byte07 Byte06 Byte05 Byte04 N=2: Byte11 Byte10 Byte09 Byte08 N=3: Byte15 Byte14 Byte13 Byte12 N=4: Byte19 Byte18 Byte17 Byte16 N=5: Byte23 Byte22 Byte21 Byte20 N=6: Byte27 Byte26 Byte25 Byte24 N=7: Byte31 Byte30 Byte29 Byte28 Data from rx, only in LPDT

			Only read when RX_Flag is setting. no way to clear this fifo.

7.6.4.30. DSI_CMD_TX_REG

Offset:0x300+N*0x04 (N=0,1,2…255)			Register Name: DSI_CMD_TX_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0	**Data** Bit: 31:24 23:16 15:8 7:0 N=0: Byte03 Byte02 Byte01 Byte00 N=1: Byte07 Byte06 Byte05 Byte04 N=2: Byte11 Byte10 Byte09 Byte08 N=3: Byte15 Byte14 Byte13 Byte12 N=4: Byte19 Byte18 Byte17 Byte16 N=5: Byte23 Byte22 Byte21 Byte20 N=6: Byte27 Byte26 Byte25 Byte24 N=7: Byte31 Byte30 Byte29 Byte28 Data for tx, transmission in HS and LPDT, defined by INST_REG

7.7. IEP

The IEP (Image Enhancement Processor) is capable of color management, detail enhancement, and dynamic range control.

7.7.1. CMU

IEP CMU (Color Management Unit) is used to adjust colors from DEBE so that a better vision effect can be achieved, and it is also capable of skin tones enhancement.

The CMU features:

- Support RGB888 input and output format
- Support window clipping up to 8192*8192 pixels
- Support global and local adjustment for hue/ saturation/ brightness in HSV space
- Support red/green/blue/cyan/magenta/yellow/flesh areas modification in local adjustment mode

7.7.2. DEU

IEP DEU(Detail Enhance Unit) is used for DEFE data post-processing, which contains 2D/1D Peaking (sharpening edges and textures of luma, and improving acutance), 1D CTI (detecting chroma horizontal transients and improving their steepness without generating overshoots), and WLE/BLE (expanding the white level and black level to improve contrast).

The DEU features:

- Require planar YUV444 color space input
- Support planar YUV444/RGB888 color space output
- Support input/output size up to 4096×4096
- 2D Luma peaking for luminance channel for maximum 2048 pixel/line input

- 1D Luma peaking for luminance channel for input 2048 pixel/line above
- 1D Dynamic color transient improvement for two chrominance channels
- White level expansion/ Black level expansion for luminance channel

7.7.3. DRC

IEP DRC (Dynamic Range Controller) can be used to adjust the image mapping curve based on the histogram frame by frame.

A typical application of IEP DRC is for content-based backlight control.

8 INTERFACE

This section details the A31 interface controllers, including

- SD/MMC
- TWI
- P2WI
- SPI
- UART
- CIR
- USB DRD
- USB HOST
- DIGITAL AUDIO
- TRANSPORT STREAM CONTROLLER
- EMAC

8.1. SD/MMC

8.1.1. OVERVIEW

The SD/MMC controller provides an interface between the host and SD/MMC/SDIO memory cards, and handles SD/MMC transactions with minimum local host intervention. Four SD/MMC host controllers are provided for different applications and compliance with SD physical layer specification v3.0 (SD3.0), eMMC standard specification v4.5 (eMMC4.5) and SDIO card specification v2.0 (SDIO2.0).

It features:

- Comply with eMMC standard specification v4.5 (eMMC4.5)
- Comply with SD physical layer specification v3.0 (SD3.0)
- Comply with SDIO card specification v2.0 (SDIO2.0)
- Support 1/4/8 bit bus width
- Support HS/DS/SDR12/SDR25/SDR50/HS200/DDR50 bus mode
- Support adjustable power supply for signal voltage, 1.8V/3.3V
- Support eMMC boot operation
- Support maximum 100MHz transmit clock
- Support SDIO interrput detection
- Support four independent SD/MMC/SDIO host controllers
- Support SDSC/SDHC/SDXC/UHS-I/MMC/RS-MMC card
- Support eMMC/iNand flash
- Support 7-bit command response CRC and 16-bit data CRC generation and error detection
- Support build-in 64-byte FIFO for buffered read or write operation
- Support descriptor-based internal DMA controller for efficient scatter and gather operations

8.1.2. BLOCK DIAGRAM

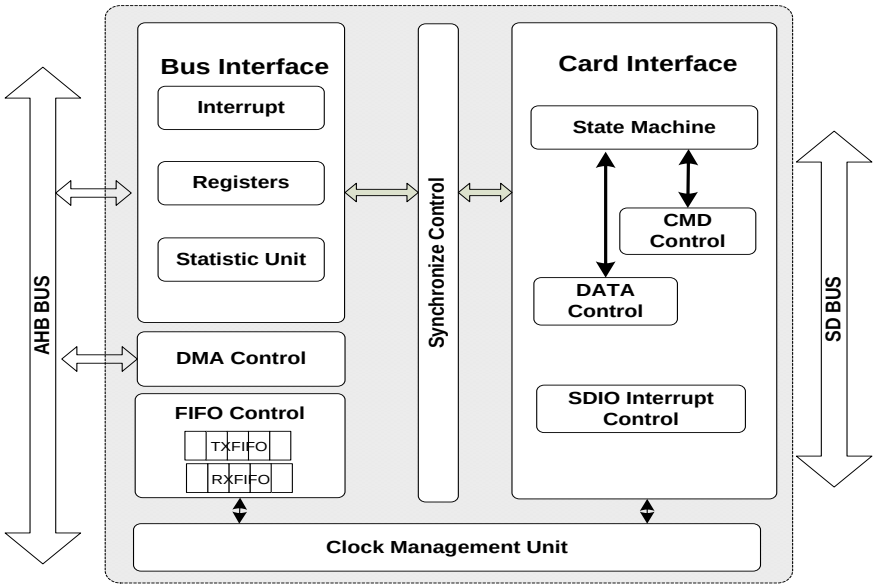


Figure 8-1 SD Host Controller Block Diagram

8.1.3. SD/MMC TIMING DIAGRAM

The SD/MMC host controller supports SD/MMC DS/HS/SDR12/SDR25/SDR50/HS200/DDR50 bus modes and supports 1/4/8bit bus width. Command and response signals are sampled on the rising edge of clock. Data timing diagrams for each bus mode are shown below:

- **Timing for SDR mode**

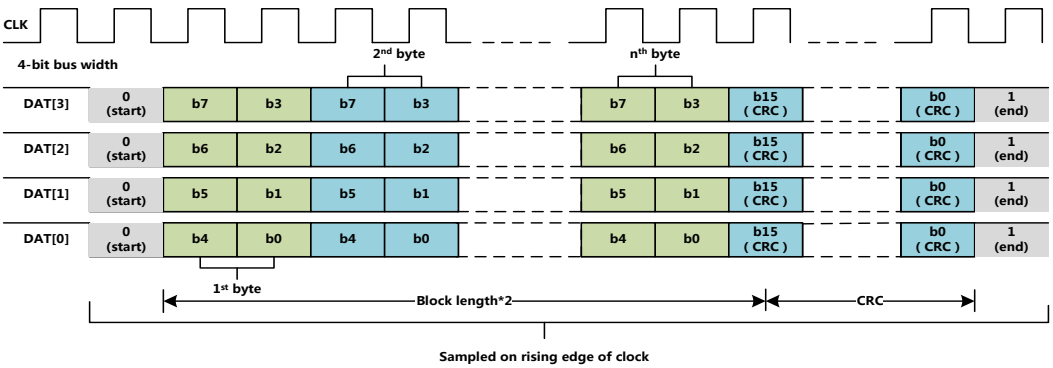


Figure 8-2 Timing for 4-bit SDR Mode

- **Timing for 8-bit SDR mode**

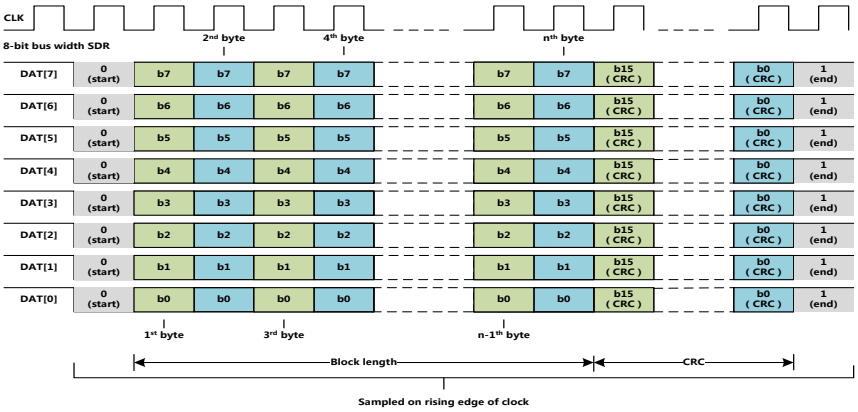


Figure 8-3 Timing for 8-bit SDR Mode

- **Timing for 4-bit DDR mode**

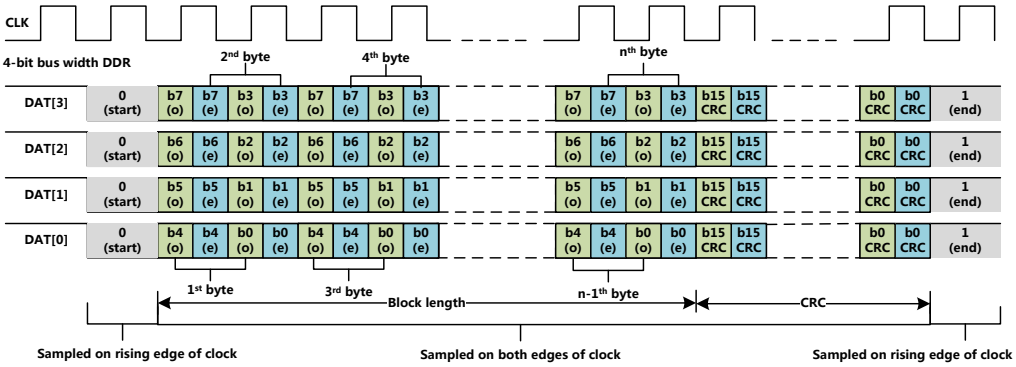


Figure 8-4 Timing for 4-bit DDR Mode

- **Timing for 8-bit DDR mode**

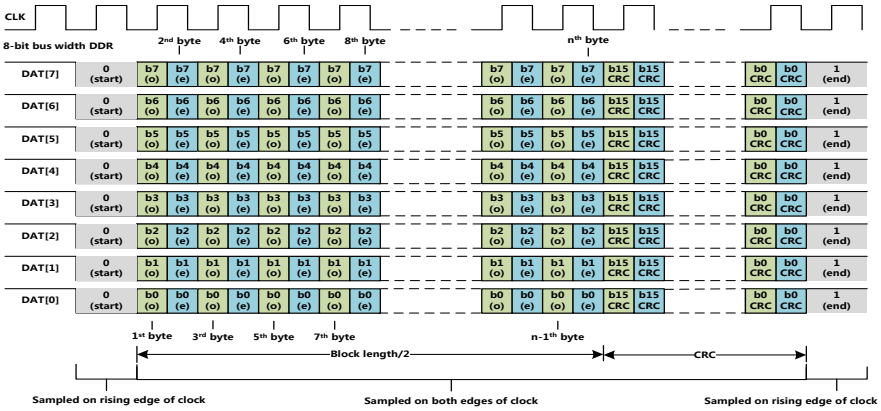


Figure 8-5 Timing for 8-bit DDR Mode

8.1.4. SD/MMC SPECIAL REQUIREMENT

8.1.4.1. SD/MMC PIN LIST

Port Name	Width	Direction	Description
SD_CCLK	1	OUT	Clock output for SD/SDIO/MMC card
SD_CCMD	1	IN/OUT	CMD line
SD_CDATA	4	IN/OUT	Data line

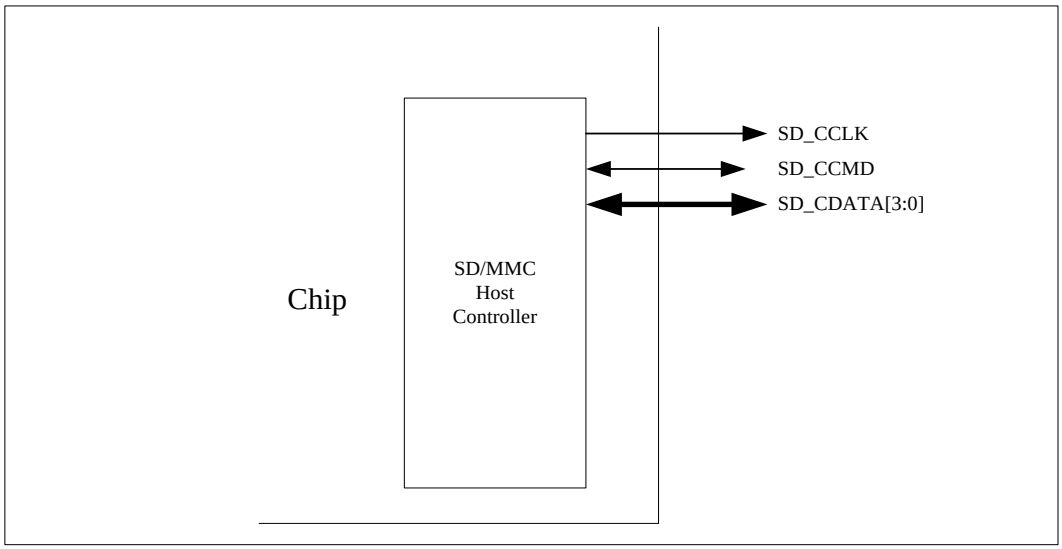


Figure 8-6 SD/MMC Pin Diagram

8.1.4.2. SD/MMC CLOCK REQUIREMENT

There are four clocks for the SD/MMC module.

CLOCK NAME	DESCRIPTION	REQUIREMENT
clk	AHB bus clock	clk>=1/10 cclk
cclk	Card input clock	100Mhz, 50/50 duty-cycle clock
cclk_n	Card outputs driving clock	Inverted cclk
cclk_in[1:0]	Card input sampling clock	Send cclk_out [1:0] through an output PAD and bring it back with an input PAD; connect it to cclk_in [1:0] (and additional delay-matching to correctly sample

		the data/cmd driven out by the cards).

8.2. TWI

8.2.1. OVERVIEW

The TWI Controller is used as an interface between CPU host and the serial TWI bus. It can support all standard TWI transfer, including Slave and Master. The communication to the TWI bus is carried out on a byte-wise basis using interrupt or polled handshaking. This TWI Controller can be operated in standard mode (100K bps) or fast-mode, supporting data rate up to 400K bps. Multiple Masters and 10-bit addressing Mode are supported for this specified application. General Call Addressing is also supported in Slave mode.

The TWI Controller includes the following features:

- Software-programmable for Slave or Master
- Support Repeated START signal
- Multi-master systems supported
- Allow 10-bit addressing with TWI bus
- Perform arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Support speeds up to 400Kbits/s (‘fast mode’)
- Allow operation from a wide range of input clock frequencies

8.2.2. TWI CONTROLLER TIMING DIAGRAM

Data transferred are always in a unit of 8-bit (byte), followed by an acknowledge bit. The number of bytes that can be transmitted per transfer is unrestricted. Data is transferred in serial with the MSB first. Between each byte of data transfer, a receiver device will hold the clock line SCL low to force the transmitter into a wait state while waiting the response from microprocessor.

Data transfer with acknowledge is obligatory. The clock line is driven by the master all the time, including the acknowledge-related clock cycle, except for the SCL holding between each bytes. After sending each byte, the transmitter releases the SDA line to allow the receiver to pull down the SDA line and send an acknowledge signal (or leave it high to send a "not acknowledge") to the transmitter.

When a slave receiver doesn't acknowledge the slave address (unable to receive because of no resource available), the data line must be left high by the slave so that the master can then generate a STOP condition to abort the transfer. Slave receiver can also indicate not to want to send more data during a transfer by leave the acknowledge signal high. And the master should generate the STOP condition to abort the transfer.

Following diagram provides an illustration the relation of SDA signal line and SCL signal line on the TWI serial bus.

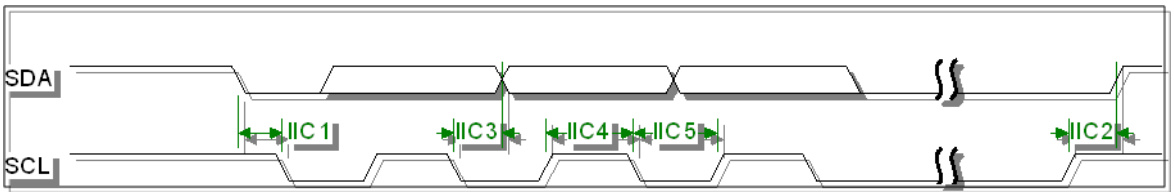


Figure 8-7 TWI Timing Diagram

8.2.3. TWI CONTROLLER REGISTER LIST

Module Name	Base Address
R_TWI	0x01F02400
TWI0	0x01C2AC00
TWI1	0x01C2B000
TWI2	0x01C2B400
TWI3	0x01C0B800

Register Name	Offset	Description
TWI_ADDR	0x0000	TWI Slave address

TWI_XADDR	0x0004	TWI Extended slave address
TWI_DATA	0x0008	TWI Data byte
TWI_CNTR	0x000C	TWI Control register
TWI_STAT	0x0010	TWI Status register
TWI_CCR	0x0014	TWI Clock control register
TWI_SRST	0x0018	TWI Software reset
TWI_EFR	0x001C	TWI Enhance Feature register
TWI_LCR	0x0020	TWI Line Control register

8.2.4. TWI CONTROLLER REGISTER DESCRIPTION

8.2.4.1. TWI SLAVE ADDRESS REGISTER

Offset: 0x00			**Register Name: TWI_ADDR** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7:1	R/W	0	SLA Slave address ● 7-bit addressing SLA6, SLA5, SLA4, SLA3, SLA2, SLA1, SLA0 ● 10-bit addressing 1, 1, 1, 1, 0, SLAX[9:8]
0	R/W	0	GCE General call address enable 0: Disable 1: Enable

Notes:

For 7-bit addressing:

SLA6 – SLA0 is the 7-bit address of the TWI when in slave mode. When the TWI receives this address after a START condition, it will generate an interrupt and enter slave mode. (SLA6 corresponds to the first bit received from the TWI bus.) If GCE is set to '1', the TWI will also recognize the general call address (00h).

For 10-bit addressing:

When the address received starts with 11110b, the TWI recognizes this as the first part of a 10-bit address and if the next two bits match ADDR[2:1] (i.e. SLAX9 and SLAX8 of the device's extended address), it sends an ACK. (The device does not generate an interrupt at this point.) If the next byte of the address matches the XADDR register (SLAX7 – SLAX0), the TWI generates an interrupt and goes into slave mode.

8.2.4.2. TWI EXTEND ADDRESS REGISTER

Offset: 0x04			**Register Name: TWI_XADDR** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7:0	R/W	0	SLAX Extend Slave Address SLAX[7:0]

8.2.4.3. TWI DATA REGISTER

Offset: 0x08			**Register Name: TWI_DATA** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7:0	R/W	0	TWI_DATA Data byte for transmitting or received

8.2.4.4. TWI CONTROL REGISTER

Offset: 0x0C	**Register Name: TWI_CNTR** **Default Value: 0x0000_0000**

Bit	Read/Write	Default	Description
31:8	/	/	/
7	R/W	0	INT_EN Interrupt Enable 1'b0: The interrupt line always low 1'b1: The interrupt line will go high when INT_FLAG is set.
6	R/W	0	BUS_EN TWI Bus Enable 1'b0: The TWI bus inputs ISDA/ISCL are ignored and the TWI Controller will not respond to any address on the bus 1'b1: The TWI will respond to calls to its slave address – and to the general call address if the GCE bit in the ADDR register is set. Notes: In master operation mode, this bit should be set to '1'
5	R/W	0	M_STA Master Mode Start When M_STA is set to '1', TWI Controller enters master mode and will transmit a START condition on the bus when the bus is free. If the M_STA bit is set to '1' when the TWI Controller is already in master mode and one or more bytes have been transmitted, then a repeated START condition will be sent. If the M_STA bit is set to '1' when the TWI is being accessed in slave mode, the TWI will complete the data transfer in slave mode then enter master mode when the bus has been released. The M_STA bit is cleared automatically after a START condition has been sent: writing a '0' to this bit has no effect.
4	R/W	0	M_STP Master Mode Stop If M_STP is set to '1' in master mode, a STOP condition is transmitted

			on the TWI bus. If the M_STP bit is set to '1' in slave mode, the TWI will behave as if a STOP condition has been received, but no STOP condition will be transmitted on the TWI bus. If both M_STA and M_STP bits are set, the TWI will first transmit the STOP condition (if in master mode) then transmit the START condition. The M_STP bit is cleared automatically: writing a '0' to this bit has no effect.
3	R/W	0	INT_FLAG Interrupt Flag INT_FLAG is automatically set to '1' when any of 28 (out of the possible 29) states is entered (see 'STAT Register' below). The only state that does not set INT_FLAG is state F8h. If the INT_EN bit is set, the interrupt line goes high when IFLG is set to '1'. If the TWI is operating in slave mode, data transfer is suspended when INT_FLAG is set and the low period of the TWI bus clock line (SCL) is stretched until '1' is written to INT_FLAG. The TWI clock line is then released and the interrupt line goes low.
2	R/W	0	A_ACK Assert Acknowledge When A_ACK is set to '1', an Acknowledge (low level on SDA) will be sent during the acknowledge clock pulse on the TWI bus if: 1. Either the whole of a matching 7-bit slave address or the first or the second byte of a matching 10-bit slave address has been received. 2. The general call address has been received and the GCE bit in the ADDR register is set to '1'. 3. A data byte has been received in master or slave mode.

			When A_ACK is '0', a Not Acknowledge (high level on SDA) will be sent when a data byte is received in master or slave mode. If A_ACK is cleared to '0' in slave transmitter mode, the byte in the DATA register is assumed to be the 'last byte'. After this byte has been transmitted, the TWI will enter state C8h then return to the idle state (status code F8h) when INT_FLAG is cleared. The TWI will not respond as a slave unless A_ACK is set.
1:0	R/W	0	/

8.2.4.5. TWI STATUS REGISTER

Offset: 0x10			**Register Name: TWI_STAT** **Default Value: 0x0000_00F8**
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7:0	R	0xF8	STA Status Information Byte **Code Status** 0x00: Bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received

			0x50: Data byte received in master mode, ACK transmitted 0x58: Data byte received in master mode, not ACK transmitted 0x60: Slave address + Write bit received, ACK transmitted 0x68: Arbitration lost in address as master, slave address + Write bit received, ACK transmitted 0x70: General Call address received, ACK transmitted 0x78: Arbitration lost in address as master, General Call address received, ACK transmitted 0x80: Data byte received after slave address received, ACK transmitted 0x88: Data byte received after slave address received, not ACK transmitted 0x90: Data byte received after General Call received, ACK transmitted 0x98: Data byte received after General Call received, not ACK transmitted 0xA0: STOP or repeated START condition received in slave mode 0xA8: Slave address + Read bit received, ACK transmitted 0xB0: Arbitration lost in address as master, slave address + Read bit received, ACK transmitted 0xB8: Data byte transmitted in slave mode, ACK received 0xC0: Data byte transmitted in slave mode, ACK not received 0xC8: Last byte transmitted in slave mode, ACK received 0xD0: Second Address byte + Write bit transmitted, ACK received 0xD8: Second Address byte + Write bit transmitted, ACK not received 0xF8: No relevant status information, INT_FLAG=0 Others: Reserved

8.2.4.6. TWI CLOCK REGISTER

Offset: 0x14			Register Name: TWI_CCR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:7	/	/	/
6:3	R/W	0	CLK_M
2:0	R/W	0	CLK_N The TWI bus is sampled by the TWI at the frequency defined by F0: Fsamp = F 0 = Fin / 2^CLK_N The TWI OSCL output frequency, in master mode, is F1 / 10: F1 = F0 / (CLK_M + 1) Foscl = F1 / 10 = Fin / (2^CLK_N * (CLK_M + 1)*10) For Example： Fin = 48Mhz (APB clock input) For 400kHz full speed 2Wire, CLK_N = 2, CLK_M=2 F0 = 48M/2^2=12Mhz, F1= F0/(10*(2+1)) = 0.4Mhz For 100Khz standard speed 2Wire, CLK_N=2, CLK_M=11 F0=48M/2^2=12Mhz, F1=F0/(10*(11+1)) = 0.1Mhz

8.2.4.7. TWI SOFT RESET REGISTER

Offset: 0x18			Register Name: TWI_SRST Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:1	/	/	/
0	R/W	0	SOFT_RST Soft Reset Write ‘1’ to this bit to reset the TWI and clear to ‘0’ when completing

			Soft Reset operation.

8.2.4.8. TWI ENHANCE FEATURE REGISTER

Offset: 0x1C			Register Name: TWI_EFR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:2	/	/	/
0:1	R/W	0	DBN Data Byte number follow Read Command Control 0—No Data Byte to be written after read command 1—Only 1 byte data to be written after read command 2—2 bytes data can be written after read command 3—3 bytes data can be written after read command

8.2.4.9. TWI LINE CONTROL REGISTER

Offset: 0x20			Register Name: TWI_LCR Default Value: 0x0000_003a
Bit	**Read/Write**	**Default**	**Description**
31:6	/	/	/
5	R	1	SCL_STATE Current state of TWI_SCL 0 – low 1 - high
4	R	1	SDA_STATE Current state of TWI_SDA 0 – low 1 - high
3	R/W	1	SCL_CTL TWI_SCL line state control bit

			When line control mode is enabled (bit[2] set), value of this bit decide the output level of TWI_SCL 0 – output low level 1 – output high level
2	R/W	0	SCL_CTL_EN TWI_SCL line state control enable When this bit is set, the state of TWI_SCL is control by the value of bit[3]. 0-disable TWI_SCL line control mode 1-enable TWI_SCL line control mode
1	R/W	1	SDA_CTL TWI_SDA line state control bit When line control mode is enabled (bit[0] set), value of this bit decide the output level of TWI_SDA 0 – output low level 1 – output high level
0	R/W	0	SDA_CTL_EN TWI_SDA line state control enable When this bit is set, the state of TWI_SDA is control by the value of bit[1]. 0-disable TWI_SDA line control mode 1-enable TWI_SDA line control mode

8.2.4.10. TWI DVFS CONTROL REGISTER

Offset: 0x24			**Register Name: TWI_DVFSCR** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:2	/	/	/

2	R/W	0	MS_PRIORITY CPU and DVFS BUSY set priority select 0: CPU has higher priority 1: DVFS has higher priority
1	R/W	0	CPU_BUSY_SET CPU Busy set
0	R/W	0	DVFC_BUSY_SET DVFS Busy set

Notes:

This register is only implemented in TWI0.

8.2.5. TWI CONTROLLER SPECIAL REQUIREMENT

8.2.5.1. TWI PIN LIST

Port Name	Width	Direction	Description
TWI_SCL	1	IN/OUT	TWI Clock line
TWI_SDA	1	IN/OUT	TWI Serial Data line

8.2.5.2. TWI CONTROLLER OPERATION

There are four operation modes on the TWI bus which dictates the communications method. They are Master Transmit, Master Receive, Slave Transmit and Slave Receive. In general, CPU host controls TWI by writing commands and data to it's registers. The TWI interrupts the CPU host for the attention each time a byte transfer is done or a START/STOP conditions is detected. The CPU host can also poll the status register for current status if the interrupt mechanism is not disabled by the CPU host.

When the CPU host wants to start a bus transfer, it initiates a bus START to enter the master mode by setting IM_STA bit in the 2WIRE_CNTR register to high (before it must be low). The TWI will assert INT line and INT_FLAG to indicate a completion for the START condition and each consequent byte transfer. At each

interrupt, the micro-processor needs to check the 2WIRE_STAT register for current status. A transfer has to be concluded with STOP condition by setting M_STP bit high.

In Slave Mode, the TWI also constantly samples the bus and look for its own slave address during addressing cycles. Once a match is found, it is addressed and interrupt the CPU host with the corresponding status. Upon request, the CPU host should read the status, read/write 2WIRE_DATA data register, and set the 2WIRE_CNTR control register. After each byte transfer, a slave device always halt the operation of remote master by holding the next low pulse on SCL line until the microprocessor responds to the status of previous byte transfer or START condition.

8.3. P2WI

8.3.1. OVERVIEW

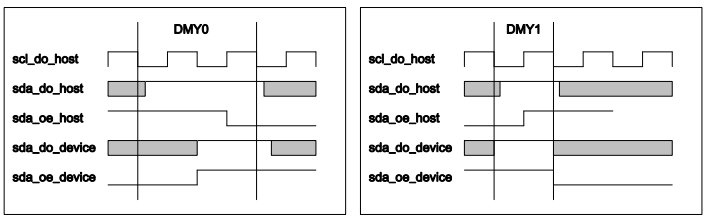
The P2WI (Push-Pull Two Wire Interface) controller is designed to communicate with a push-pull two wire bus for some of AXP serial PMU chips. It supports a special protocol with a simplified two wire protocol on a push-pull bus. The transfer speed can be up to 6MHz and the performance will be much improved. It works in the master mode.

It features:

- Support industry-standard AMBA Peripheral Bus (APB) and it is fully compliant with the AMBA Specification, Revision 2.0.
- Support Push-Pull bus
- Support Master Mode
- Support speed up to 6MHz
- Support programmable output delay of SDA signal
- Support parity check for address and data transmission

8.3.2. P2WI CONTROLLER TIMING DIAGRAM

The devices on the P2WI bus are either master or slave. The host is always the device that drives the SCL clock line. The slaves are the devices that respond to the master. It is the master that initiates a transfer. Both master and slave can transfer data over the P2WI bus, so there are two states, DMY0 and DMY1, for master and slave to convert the direction of data transmission.



When master wishes to initiate a transfer it begins by issuing a start sequence on the P2WI bus. A start sequence is one of two special sequences defined for the P2WI bus, the other being the stop sequence. The start sequence and stop sequence are special in that these are the only places where the SDA is allowed to change while the SCL is high. When data is being transferred, SDA must remain stable and not change whilst SCL is high. The start and stop sequences mark the beginning and end of a transaction with the slave device.

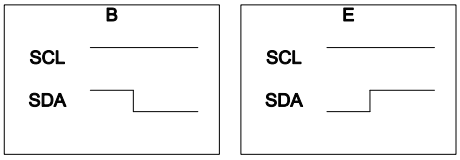
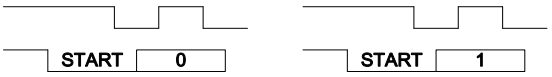
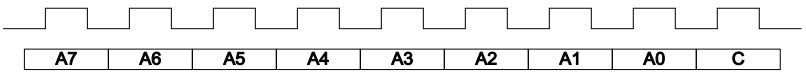


Figure 8-8 Timing Of Start and End Operation

When the start sequence is transferred on the P2WI bus, a direction bit will be transferred for the slave to realize the mode of this operation, with which bit ‘0’ means a write operation and bit ‘1’ means a read operation.



Data is transferred in sequences of 8 bits and the bits are placed on the SDA line starting with the MSB (most significant bit). The SCL line is then pulsed high, then low, which is driven by master. There are two forms with data transferred on the SDA, address and the real data. The address is always sent by master and specifies the address of one of registers of the slave. The real data written into or read from slave is in the second byte of a transaction. Every 8 bits data is followed by a parity bit, which is used by the receiver to check the correction of this byte of data.



Another ACK flag is needed in write operation, with which slave tells master that it has received the address and data successfully and will do some related operation when the stop sequence will has been transferred on the P2WI bus. The ACK flag is active low.

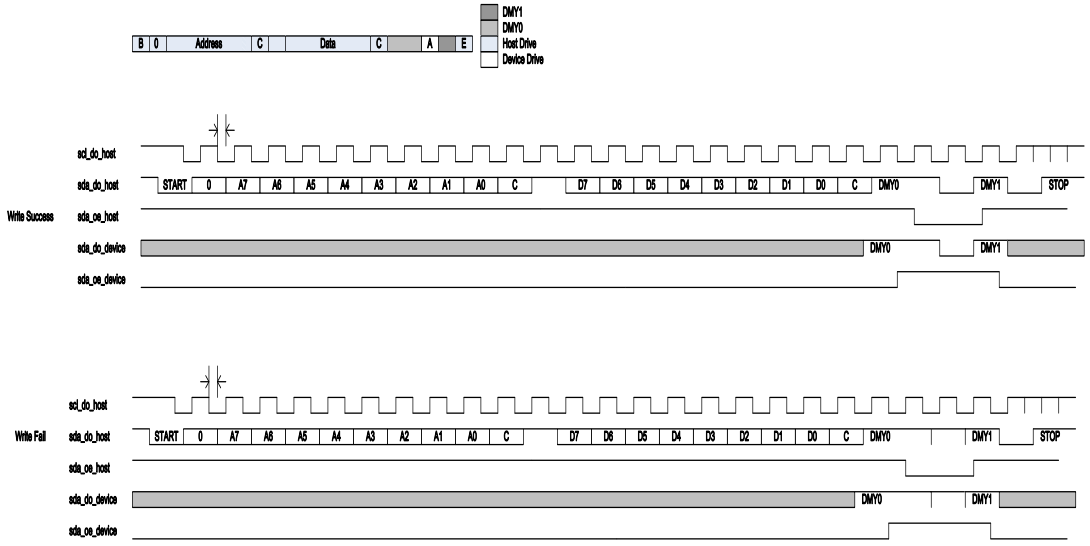


Figure 8-9 Timing Of Write Operation

ACK flag is not used in read operation. If slave finds that there is an error happened in the address transferring, it will drive the SDA line to high for 9 cycles, which include 8 bits of data and 1 bit of parity. Then master will receive an error parity bit and report this error after issuing the stop sesquence.

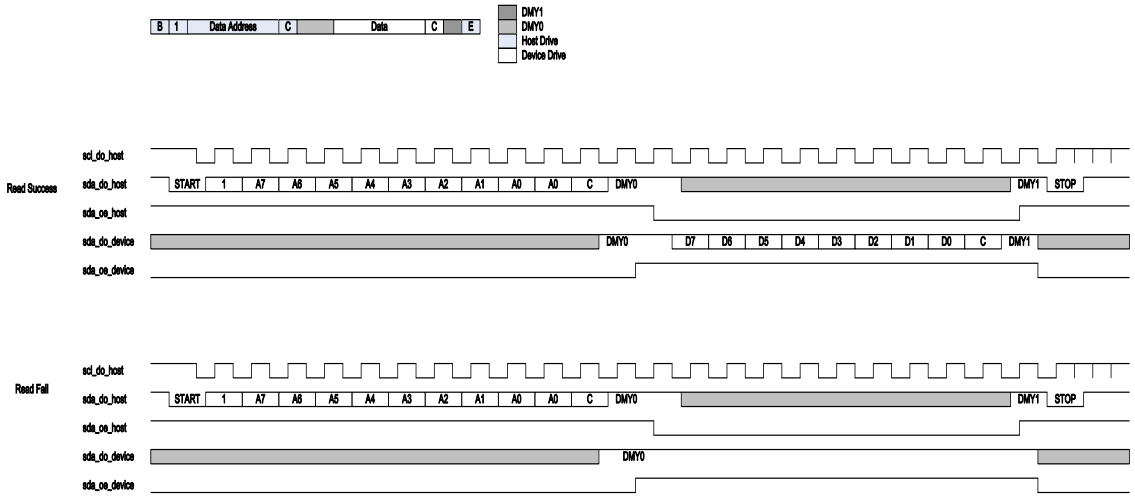


Figure 8-10 Timing of read operation

8.3.3. P2WI CONTROLLER REGISTER LIST

Module Name	Base Address
P2WI	0x01F03400

Register Name	Offset	Description
P2WI_CTRL	0x0000	P2WI Control Register
P2WI_CCR	0x0004	P2WI Clock Control Register
P2WI_INTE	0x0008	P2WI Interrupt Enable Register
P2WI_STAT	0x000c	P2WI Status Register
P2WI_DADDR0	0x0010	P2WI Data Access Address Register 0
P2WI_DADDR	0x0014	P2WI Data Access Address Register 1
P2WI_DLEN	0x0018	P2WI Data Length Register
P2WI_DATA0	0x001c	P2WI Data Buffer 0 Register
P2WI_DATA1	0x0020	P2WI Data Buffer 1 Register
P2WI_LCR	0x0024	P2WI Line Control register
P2WI_PMCR	0x0028	P2WI PMU Mode Control register

8.3.4. P2WI CONTROLLER REGISTER DESCRIPTION

8.3.4.1. P2WI CONTROL REGISTER

Offset: 0x00			Register Name: P2WI_CTRL Default Value: 0x0000_0000
Bit	**R/W**	**Default**	**Description**
7	R/W	0	START_TRANS Start transfer. 1 – start transfer 0 – neglect Setting this bit will start a new transmission with the configuration of other registers. It is cleared to '0' automatically when transfer completes or an error happens in the transmission. Setting this bit during an uncompleted transmission, a loading busy bit will be set in status register.

			Starting a new transmission with an invalid slave address or an invalid length, an invalid loading flag will be set in status register.
6	R/W	0	ABORT_TRANS 1 – Abort transmission 0 – don't care
5:2	/	/	/
1	R/W	0	GLOBAL_INT_ENB Global interrupt enable bit 1 – enable interrupt 0 – disable interrupt
0	R/W	0	Soft Reset Write '1' to this bit will reset the controller into default state. All of the status of controller will be cleared. And this bit will be cleared to '0' automatically when reset operation completes.

8.3.4.2. P2WI CLOCK CONTROL REGISTER

Offset: 0x04			**Register Name: P2WI_CCR** **Default Value: 0x0000_0000**
Bit	**R/W**	**Default**	**Description**
31:11	/	/	/
10:8	R/W	0	SDA_ODLY SDA output delay Delay time of n source clock cycles before output SDA signal.
7:0	R/W	0	CLK_DIV $F_{clk} = F_{source} / 2*(divider+1)$ The frequency of source clock must be more than 10MHz so that controller can make an accurate delay pull on SDA before releasing SDA line.

8.3.4.3. P2WI INTERRUPT ENABLE REGISTER

Offset: 0x08			Register Name: P2WI_INTE Default Value: 0x0000_0000
Bit	**R/W**	**Default**	**Description**
31:3	/	/	/
2	R/W	0	LOAD_BSY_ENB Loading Busy Interrupt Enable 1 – enable 0 – disable
1	R/W	0	TRANS_ERR_ENB Transfer Error Interrupt Enable 1 – enable 0 – disable
0	R/W	0	TRANS_OVER_ENB Transfer complete Interrupt Enable 1 – enable 0 – disable

8.3.4.4. P2WI STATUS REGISTER

Offset: 0x0c			Register Name: P2WI_INTS Default Value: 0x0000_0000
Bit	**R/W**	**Default**	**Description**
31:3	/	/	/
15:8	R/W	0	TRANS_ERR_ID. 8’b00000001 – error happened with the transmission of the 1st byte of data 8’b00000010 – error happened with the transmission of the 2nd byte of data 8’b00000100 – error happened with the transmission of the 3rd byte of data …

			8'b10000000 – error happened with the transmission of the 8th byte of data
7:3	/	/	/
2	R/W	0	LOAD_BSY Loading Busy Flag Writing any control registers during transmission will cause a busy status and this bit will be set. If LOAD_BSY_ENB=1, an interrupt will be generated. *Write '1' to clear*
1	R/W	0	TRANS_ERR Transfer Error Flag When an error happened during transmission, an error flag will be set in this bit and if TRANS_ERR_ENB=1, an interrupt will be generated. To know the detail information of error status please refers to the definition of TRANS_ERR_ID. *Write '1' to clear. Clear this bit will also clear the value of TRANS_ERR_ID.*
0	R/W	0	TRANS_OVER Transfer complete Flag After transferring a package successfully without any error, a transfer complete flag will be set and if TRANS_OVER_ENB=1, an interrupt will be generated. *Write '1' to clear*

8.3.4.5. P2WI DATA ACCESS ADDRESS REGISTER 0

Offset: 0x10			**Register Name: P2WI_DADDR0** **Default Value: 0x0000_0000**
Bit	**R/W**	**Default**	**Description**
31:24	R/W	0	Address of 4th Byte of Data
23:16	R/W	0	Address of 3rd Byte of Data

15:8	R/W	0	Address of 2nd Byte of Data
7:0	R/W	0	Address of 1st Byte of Data

8.3.4.6. P2WI DATA ACCESS ADDRESS REGISTER 1

Offset: 0x14			Register Name: P2WI_DADDR0 Default Value: 0x0000_0000
Bit	**R/W**	**Default**	**Description**
31:24	R/W	0	Address of 8th Byte of Data
23:16	R/W	0	Address of 7th Byte of Data
15:8	R/W	0	Address of 6th Byte of Data
7:0	R/W	0	Address of 5th Byte of Data

8.3.4.7. P2WI DATA LENGTH REGISTER

Offset: 0x18			Register Name: P2WI_DLEN Default Value: 0x0000_0000
Bit	**R/W**	**Default**	**Description**
31:5	/	/	/
4	R/W	0	READ_WRITE_FLAG Read/Write flag 1 – read 0 – write
3	/	/	/
2:0	R/W	0	Data Access Length 0~7 – Package length is n+1 bytes

8.3.4.8. P2WI DATA BUFFER 0 REGISTER

Offset: 0x1c			Register Name: P2WI_DATA0 Default Value: 0x0000_0000
Bit	**R/W**	**Default**	**Description**

31:24	R/W	0	Data Byte 4
23:16	R/W	0	Data Byte 3
15:8	R/W	0	Data Byte 2
7:0	R/W	0	Data Byte 1

8.3.4.9. P2WI DATA BUFFER 1 REGISTER

Offset: 0x20			Register Name: P2WI_DATA1 Default Value: 0x0000_0000
Bit	**R/W**	**Default**	**Description**
31:24	R/W	0	Data Byte 8
23:16	R/W	0	Data Byte 7
15:8	R/W	0	Data Byte 6
7:0	R/W	0	Data Byte 5

8.3.4.10. P2WI LINE CONTROL REGISTER

Offset: 0x24			Register Name: P2WI_LCR Default Value: 0x0000_003A
Bit	**R/W**	**Default**	**Description**
31:6	/	/	/
5	R	1	SCL_STATE Current state of TWI_SCL 0 – low 1 - high
4	R	1	SDA_STATE Current state of TWI_SDA 0 – low 1 – high
3	R/W	1	SCL_CTL TWI_SCL line state control bit

			When line control mode is enabled (bit[2] set), value of this bit decide the output level of TWI_SCL 0 – output low level 1 – output high level
2	R/W	0	SCL_CTL_EN TWI_SCL line state control enable When this bit is set, the state of TWI_SCL is control by the value of bit[3]. 0-disable TWI_SCL line control mode 1-enable TWI_SCL line control mode
1	R/W	1	SDA_CTL TWI_SDA line state control bit When line control mode is enabled (bit[0] set), value of this bit decide the output level of TWI_SDA 0 – output low level 1 – output high level
0	R/W	0	SDA_CTL_EN TWI_SDA line state control enable When this bit is set, the state of TWI_SDA is control by the value of bit [1]. 0-disable TWI_SDA line control mode 1-enable TWI_SDA line control mode

8.3.4.11. P2WI PMU MODE CONTROL REGISTER

Offset: 0x28			**Register Name: P2WI_PMCR** **Default Value: 0x003e3e68**
Bit	**R/W**	**Default**	**Description**
31	R/W	0	PMU_INIT_SEND 1 – Send Initial Sequence to PMU to switch PMU's bus mode from NTWI to P2WI. 0 – write ignore

			This bit will be self-cleared when initial sequence is sent onto the p2wi bus.
30:24	/	/	/
23:16	R/W	0x3e	PMU_INIT_DATA Value of PMU's initial data
15:8	R/W	0x3e	PMU MODE Control Register Address
7:0	R/W	0x68	PMU Device Address

8.4. SPI

8.4.1. OVERVIEW

The Serial Peripheral Interface (SPI) allows rapid data communication with fewer software interrupts. It contains one 128x8 receiver buffer (RXFIFO) and one 128x8 transmit buffer (TXFIFO), and can work in two modes: Master mode and Slave mode.

The SPI interface features:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Four chip selects to support multiple peripherals
- 8-bit wide by 128-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable
- Support dedicated DMA

8.4.2. SPI TIMING DIAGRAM

The serial peripheral interface master uses the SPI_SCLK signal to transfer data in and out of the shift register. Data is clocked using any one of four programmable clock phase and polarity combinations.

During Phase 0, Polarity 0 and Phase 1, Polarity 1 operations, output data changes on the falling clock edge and input data is shifted in on the rising edge.
During Phase 1, Polarity 0 and Phase 0, Polarity 1 operations, output data changes on the rising edges of the clock and is shifted in on falling edges.

The POL defines the signal polarity when SPI_SCLK is in idle state. The SPI_SCLK is high level when POL is ‘1’ and it is low level when POL is ‘0’. The PHA decides whether the leading edge of SPI_SCLK is used for

setup or sample data. The leading edge is used for setup data when PHA is '1' and for sample data when PHA is '0'. The four kind of modes are listed below:

SPI Mode	POL	PHA	Leading Edge	Trailing Edge
0	0	0	Rising, Sample	Falling, Setup
1	0	1	Rising, Setup	Falling, Sample
2	1	0	Falling, Sample	Rising, Setup
3	1	1	Failing, Setup	Rising, Sample

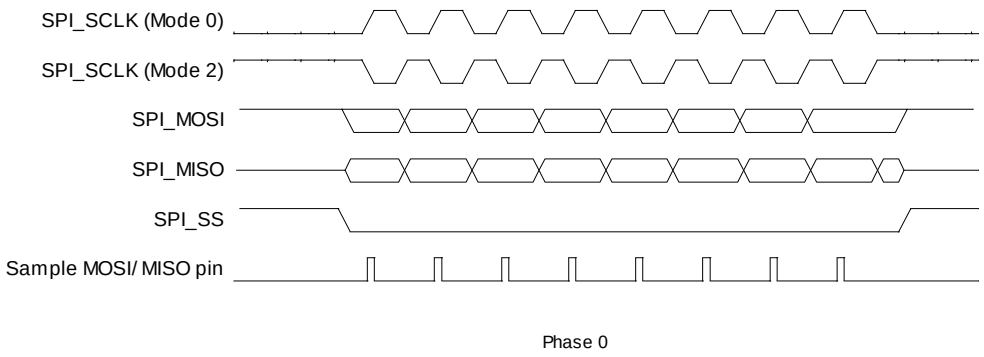


Figure 8-11 SPI Phase 0 Timing Diagram

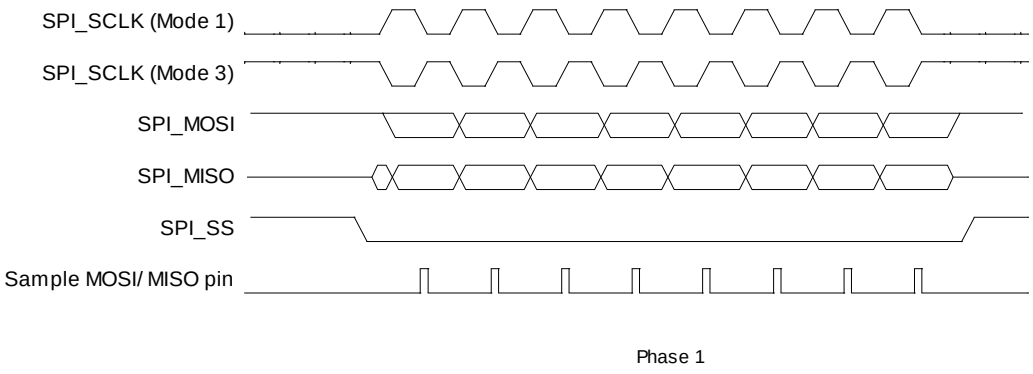


Figure 8-12 SPI Phase 1 Timing Diagram

8.4.3. SPI REGISTER LIST

Module Name	Base Address

SPI0	0x01C68000
SPI1	0x01C69000
SPI2	0x01C6A000
SPI3	0x01C6B000

Register Name	Offset	Description
SPI_VER	0x00	SPI Version Number Register
SPI_GCR	0x04	SPI Global Control Register
SPI_TCR	0x08	SPI Transfer Control register
/	0x0c	reserved
SPI_IER	0x10	SPI Interrupt Control register
SPI_ISR	0x14	SPI Interrupt Status register
SPI_FCR	0x18	SPI FIFO Control register
SPI_FSR	0x1C	SPI FIFO Status register
SPI_WCR	0x20	SPI Wait Clock Counter register
SPI_CCR	0x24	SPI Clock Rate Control register
/	0x28	reserved
/	0x2c	reserved
SPI_MBC	0x30	SPI Burst Counter register
SPI_MTC	0x34	SPI Transmit Counter Register
SPI_BCC	0x38	SPI Burst Control register
SPI_TXD	0x200	SPI TX Data register
SPI_RXD	0x300	SPI RX Data register

8.4.4. SPI REGISTER DESCRIPTION

8.4.4.1. SPI VERSION NUMBER REGISTER

Offset: 0x00	Register Name: SPI_VER

			Default Value: 0x0000_0080
Bit	**Read/Write**	**Default**	**Description**
31:16	R	0	VER_H
15:0	R	0	VER_L

8.4.4.2. SPI GLOBAL CONTROL REGISTER

Offset: 0x04			**Register Name: SPI_CTL** **Default Value: 0x0000_0080**
Bit	**Read/Write**	**Default**	**Description**
31	R/W	0	SRST Soft reset Write '1' to this bit will clear the SPI controller, and auto clear to '0' when reset operation completes Write '0' has no effect.
30:8	/	/	/
7	R/W	1	TP_EN Transmit Pause Enable In master mode, it is used to control transmit state machine to stop smart burst sending when RX FIFO is full. 1 – stop transmit data when RXFIFO full 0 – normal operation, ignore RXFIFO status Note: Can't be written when XCH=1
6:2	/	/	/
1	R/W	0	MODE SPI Function Mode Select 0: Slave Mode 1: Master Mode Note: Can't be written when XCH=1
0	R/W	0	EN

			SPI Module Enable Control 0: Disable 1: Enable

8.4.4.3. SPI TRANSFER CONTROL REGISTER

Offset: 0x08			Register Name: SPI_INTCTL Default Value: 0x0000_0087
Bit	**Read/Write**	**Default**	**Description**
31	R/W	0x0	XCH Exchange Burst In master mode it is used to start SPI burst 0: Idle 1: Initiates exchange. Write “1” to this bit will start the SPI burst, and will auto clear after finishing the bursts transfer specified by BC. Write “1” to SRST will also clear this bit. Write ‘0’ to this bit has no effect. Note：Can’t be written when XCH=1.
30:13	R	0x0	Reserved.
12	R/W	0x0	FBS First Transmit Bit Select 0: MSB first 1: LSB first Note：Can’t be written when XCH=1.
11	R/W	0x0	SDC Master Sample Data Control Set this bit to ‘1’ to make the internal read sample point with a delay of half cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave.

			0 – normal operation, do not delay internal read sample point 1 – delay internal read sample point Note：Can't be written when XCH=1.
10	R/W	0x0	RPSM Rapids mode select Select Rapids mode for high speed write. 0: normal write mode 1: rapids write mode Note：Can't be written when XCH=1.
9	R/W	0x0	DDB Dummy Burst Type 0: The bit value of dummy SPI burst is zero 1: The bit value of dummy SPI burst is one Note：Can't be written when XCH=1.
8	R/W	0x0	DHB Discard Hash Burst In master mode it controls whether discarding unused SPI bursts 0: Receiving all SPI bursts in BC period 1: Discard unused SPI bursts, only fetching the SPI bursts during dummy burst period. The bursts number is specified by TC. Note：Can't be written when XCH=1.
7	R/W	0x1	SS_LEVEL When control SS signal manually (SPI_CTRL_REG.SS_CTRL==1), set this bit to '1' or '0' to control the level of SS signal. 0: set SS to low 1: set SS to high Note：Can't be written when XCH=1.
6	R/W	0x0	SS_OWNER SS Output Owner Select

			Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software Note：Can't be written when XCH=1.
5:4	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted Note：Can't be written when XCH=1.
3	R/W	0x0	SSCTL In master mode, this bit selects the output wave form for the SPI_SSx signal. Only valid when SS_OWNER = 0. 0: SPI_SSx remains asserted between SPI bursts 1: Negate SPI_SSx between SPI bursts Note：Can't be written when XCH=1.
2	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) Note：Can't be written when XCH=1.
1	R/W	0x1	CPOL SPI Clock Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle)

			Note：Can’t be written when XCH=1.
0	R/W	0x1	CPHA SPI Clock/Data Phase Control 0: Phase 0 (Leading edge for sample data) 1: Phase 1 (Leading edge for setup data) Note：Can’t be written when XCH=1.

8.4.4.4. SPI INTERRUPT CONTROL REGISTER

Offset: 0x010			**Register Name: SPI_IER** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:14	R	0x0	Reserved.
13	R/W	0x0	SS_INT_EN SSI Interrupt Enable Chip Select Signal (SSx) from valid state to invalid state 0: Disable 1: Enable
12	R/W	0x0	TC_INT_EN Transfer Completed Interrupt Enable 0: Disable 1: Enable
11	R/W	0x0	TF_UDR_INT_EN TXFIFO under run Interrupt Enable 0: Disable 1: Enable
10	R/W	0x0	TF_OVF_INT_EN TX FIFO Overflow Interrupt Enable 0: Disable 1: Enable

9	R/W	0x0	RF_UDR_INT_EN RXFIFO under run Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	RF_OVF_INT_EN RX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
7	R	0x0	Reserved.
6	R/W	0x0	TF_FUL_INT_EN TX FIFO Full Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TX_EMP_INT_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	TX_ERQ_INT_EN TX FIFO Empty Request Interrupt Enable 0: Disable 1: Enable
3	R	0x0	Reserved
2	R/W	0x0	RF_FUL_INT_EN RX FIFO Full Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	RX_EMP_INT_EN RX FIFO Empty Interrupt Enable 0: Disable

			1: Enable
0	R/W	0x0	RF_RDY_INT_EN RX FIFO Ready Request Interrupt Enable 0: Disable 1: Enable

8.4.4.5. SPI INTERRUPT STATUS REGISTER

Offset: 0x14			**Register Name: SPI_INT_STA** **Default Value: 0x0000_0022**
Bit	**Read/Write**	**Default**	**Description**
31:14	/	0	/
13	R/W	0	SSI SS Invalid Interrupt When SSI is 1, it indicates that SS has changed from valid state to invalid state. Writing 1 to this bit clears it.
12	R/W	0	TC Transfer Completed In master mode, it indicates that all bursts specified by BC has been exchanged. In other condition, When set, this bit indicates that all the data in TXFIFO has been loaded in the Shift register, and the Shift register has shifted out all the bits. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed
11	R/W	0	TF_UDF TXFIFO under run This bit is set when if the TXFIFO is underrun. Writing 1 to this bit clears it. 0: TXFIFO is not underrun 1: TXFIFO is underrun

10	R/W	0	TF_OVF TXFIFO Overflow This bit is set when if the TXFIFO is overflow. Writing 1 to this bit clears it. 0: TXFIFO is not overflow 1: TXFIFO is overflowed
9	R/W	0	RX_UDF RXFIFO Underrun When set, this bit indicates that RXFIFO has underrun. Writing 1 to this bit clears it.
8	R/W	0	RX_OVF RXFIFO Overflow When set, this bit indicates that RXFIFO has overflowed. Writing 1 to this bit clears it. 0: RXFIFO is available. 1: RXFIFO has overflowed.
7	/	/	/
6	R/W	0	TX_FULL TXFIFO Full This bit is set when if the TXFIFO is full. Writing 1 to this bit clears it. 0: TXFIFO is not Full 1: TXFIFO is Full
5	R/W	1	TX_EMP TXFIFO Empty This bit is set if the TXFIFO is empty. Writing 1 to this bit clears it. 0: TXFIFO contains one or more words. 1: TXFIFO is empty
4	R/W	0	TX_READY TXFIFO Ready

			0: TX_WL > TX_TRIG_LEVEL 1: TX_WL <= TX_TRIG_LEVEL This bit is set any time if TX_WL <= TX_TRIG_LEVEL. Writing “1” to this bit clears it. Where TX_WL is the water level of RXFIFO
3	/	/	reserved
2	R/W	0	RX_FULL RXFIFO Full This bit is set when the RXFIFO is full. Writing 1 to this bit clears it. 0: Not Full 1: Full
1	R/W	1	RX_EMP RXFIFO Empty This bit is set when the RXFIFO is empty. Writing 1 to this bit clears it. 0: Not empty 1: empty
0	R/W	0	RX_RDY RXFIFO Ready 0: RX_WL < RX_TRIG_LEVEL 1: RX_WL >= RX_TRIG_LEVEL This bit is set any time if RX_WL >= RX_TRIG_LEVEL. Writing “1” to this bit clears it. Where RX_WL is the water level of RXFIFO.

8.4.4.6. SPI FIFO CONTROL REGISTER

Offset: 0x18			**Register Name: SPI_DMACTL** **Default Value: 0x0040_0001**
Bit	**Read/Write**	**Default**	**Description**
31	R/W	0	TX_FIFO_RST TX FIFO Reset Write ‘1’ to this bit will reset the control portion of the TX FIFO and

			auto clear to ‘0’ when completing reset operation, write to ‘0’ has no effect.
30	R/W	0	/
29:25	/	/	/
24	R/W	0x0	TF_ DRQ_EN TX FIFO DMA Request Enable 0: Disable 1: Enable
23:16	R/W	0x40	TX_TRIG_LEVEL TX FIFO Empty Request Trigger Level
15	W/R	0x0	RF_RST RXFIFO Reset Write ‘1’ to this bit will reset the control portion of the receiver FIFO, and auto clear to ‘0’ when completing reset operation, write ‘0’ to this bit has no effect.
14	W/R	0x0	/
13:10	R	0x0	Reserved
9	W/R	0x0	RX_DMA_MODE SPI RX DMA Mode Control 0: Normal DMA mode 1: Dedicate DMA mode
8	R/W	0x0	RF_ DRQ_EN RX FIFO DMA Request Enable 0: Disable 1: Enable
7:0	R/W	0x1	RX_TRIG_LEVEL RX FIFO Ready Request Trigger Level

8.4.4.7. SPI FIFO STATUS REGISTER

Offset: 0x1c			Register Name: SPI_FSR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31	R	0x0	TB_WR TX FIFO Write Buffer Write Enable
30:28	R	0x0	TB_CNT TX FIFO Write Buffer Counter These bits indicate the number of words in TX FIFO Write Buffer
27:24	R	0x0	Reserved
23:16	R	0x0	TF_CNT TX FIFO Counter These bits indicate the number of words in TX FIFO 0: 0 byte in TX FIFO 1: 1 byte in TX FIFO … 127: 127 bytes in TX FIFO
15	R	0x0	RB_WR RX FIFO Read Buffer Write Enable
14:12	R	0x0	RB_CNT RX FIFO Read Buffer Counter These bits indicate the number of words in RX FIFO Read Buffer
11:8	R	0x0	Reserved
7:0	R	0x0	RF_CNT RX FIFO Counter These bits indicate the number of words in RX FIFO 0: 0 byte in RX FIFO 1: 1 byte in RX FIFO …

			127: 127 bytes in RX FIFO

8.4.4.8. SPI WAIT CLOCK REGISTER

Offset: 0x20			Register Name: SPI_WAIT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:20	/	/	/
19:16	R/W	0x0	SWC Dual mode direction switch wait clock counter (for master mode only). 0: No wait states inserted n: n SPI_SCLK wait states inserted Note: These bits control the number of wait states to be inserted before start dual data transfer in dual SPI mode. The SPI module counts SPI_SCLK by SWC for delaying next word data transfer. Note：Can't be written when XCH=1.
15:0	R/W	0	WCC Wait Clock Counter (In Master mode) These bits control the number of wait states to be inserted in data transfers. The SPI module counts SPI_SCLK by WCC for delaying next word data transfer. 0: No wait states inserted N: N SPI_SCLK wait states inserted

8.4.4.9. SPI CLOCK CONTROL REGISTER

Offset: 0x24			Register Name: SPI_CCTL Default Value: 0x0000_0002
Bit	**Read/Write**	**Default**	**Description**
31:13	/	/	/

12	R/W	0	DRS Divide Rate Select (Master Mode Only) 0: Select Clock Divide Rate 1 1: Select Clock Divide Rate 2
11:8	R/W	0	CDR1 normal sample when SDC and CDR1 are 1 basic sample when CDR1=~(SDC|CPHA)
7:0	R/W	0x2	CDR2 Clock Divide Rate 2 (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = AHB_CLK / (2*(n + 1)).

8.4.4.10. SPI MASTER BURST COUNTER REGISTER

Offset: 0x30			**Register Name: SPI_BC** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
23:0	R/W	0	MBC Master Burst Counter In master mode, this field specifies the total burst number. 0: 0 burst 1: 1 burst … N: N bursts

8.4.4.11. SPI MASTER TRANSMIT COUNTER REGISTER

Offset: 0x34			**Register Name: SPI_TC** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**

31:24	/	/	/
23:0	R/W	0	MWTC Master Write Transmit Counter In master mode, this field specifies the burst number that should be sent to TXFIFO before automatically sending dummy burst.For saving bus bandwidth, the dummy burst (all zero bits or all one bits) is sent by SPI Controller automatically. 0: 0 burst 1: 1 burst … N: N bursts

8.4.4.12. SPI MASTER BURST CONTROL COUNTER REGISTER

Offset: 0x38			**Register Name: SPI_BCC** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:29	R	0x0	Reserved
28	R/W	0x0	DRM Master Dual Mode RX Enable 0: RX use single-bit mode 1: RX use dual mode Note：Can’t be written when XCH=1.
27:24	R/W	0x0	DBC Master Dummy Burst Counter In master mode, this field specifies the burst number that should be sent before receive in dual SPI mode. The data is don’t care by the device. 0: 0 burst 1: 1 burst

			… N: N bursts Note：Can’t be written when XCH=1.
23:0	R/W	0x0	STC Master Single Mode Transmit Counter In master mode, this field specifies the burst number that should be sent in single mode before automatically sending dummy burst. This is the first transmit counter in all bursts. 0: 0 burst 1: 1 burst … N: N bursts Note：Can’t be written when XCH=1.

8.4.4.13. SPI TX DATA REGISTER

Offset: 0x200			Register Name: SPI_TXD Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	W/R	0x0	TDATA Transmit Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are rooms in RXFIFO, one burst data is written to RXFIFO and the depth is increased by 1. In half-word accessing method, two SPI burst data are written and the TXFIFO depth is increase by 2. In word accessing method, four SPI burst data are written and the TXFIFO depth is increased by 4. Note: This address is writing-only if TF_TEST is ‘0’, and if TF_TEST is set to ‘1’, this address is readable and writable to test the TX FIFO through the AHB bus.

8.4.4.14. SPI RX DATA REGISTER

Offset: 0x300			Register Name: SPI_RXD Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R	0	RDATA Receive Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are data in RXFIFO, the top word is returned and the RXFIFO depth is decreased by 1. In half-word accessing method, two SPI bursts are returned and the RXFIFO depth is decrease by 2. In word accessing method, the four SPI bursts are returned and the RXFIFO depth is decreased by 4. Note: This address is read-only if RF_TEST is '0', and if RF_TEST is set to '1', this address is readable and writable to test the RX FIFO through the AHB bus.

8.4.5. SPI SPECIAL REQUIREMENT

8.4.5.1. SPI PIN LIST

The direction of SPI pin is different in two work modes: Master Mode and Slave Mode.

Port Name	Width	Direction(M)	Direction(S)	Description
SPI_SCLK	1	OUT	IN	SPI Clock
SPI_MOSI	1	OUT	IN	SPI Master Output Slave Input Data Signal
SPI_MISO	1	IN	OUT	SPI Master Input Slave Output Data Signal
SPI_SS[3:0]	4	OUT	IN	SPI Chip Select Signal

Notes:

SPI0 module has four chip select signals and SPI1 module has only one chip select signal for pin saving.

8.4.5.2. SPI MODULE CLOCK SOURCE AND FREQUENCY

The SPI module uses two clock sources: AHB_CLK and SPI_CLK. The SPI_SCLK ranges from 3KHz to 100 MHZ, and AHB_CLK >= 2xSPI_SCLK.

Clock Name	Description	Requirement
AHB_CLK	AHB bus clock, as the clock source of SPI module	AHB_CLK >= 2xSPI_SCLK
SPI_CLK	SPI serial input clock	

8.5. UART

8.5.1. OVERVIEW

The UART is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.

The UART contains registers to control the character length, baud rate, parity generation/checking, and interrupt generation. Although there is only one interrupt output signal from the UART, there are several prioritized interrupt types that can be responsible for its assertion. Each of the interrupt types can be separately enabled or disabled with the control registers.

The UART has 16450 and 16550 modes of operation, which are compatible with a range of standard software drivers. In 16550 mode, transmit and receive operations are both buffered by FIFOs. In 16450 mode, these FIFOs are disabled.

The UART supports word lengths from five to eight bits, an optional parity bit and 1, 1 ½ or 2 stop bits, and is fully programmable by an AMBA APB CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, together with separate transmit and receive FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided.

Interrupts can be generated for a range of TX Buffer/FIFO, RX Buffer/FIFO, Modem Status and Line Status conditions.

For integration in systems where Infrared SIR serial data format is required, the UART can be configured to have a software-programmable IrDA SIR Mode. If this mode is not selected, only the UART (RS232 standard) serial data format is available.

The UART includes the following features:

- Compliant with industry-standard 16450/16550 UARTs specification
- Support 1/1.5/2 stop bits

- Support fully AMBA APB CPU interface programmable operation
- Support 16-bit programmable baud rate and dynamic modification
- Support 2-wire serial communication
- Support 4-wire auto data flow communication
- Support 8-wire modem(data carrier equipment, DCE) or data set
- Separate transmit and receive FIFOs
- Eight modem control lines and a diagnostic loop-back mode

8.5.2. UART TIMING DIAGRAM

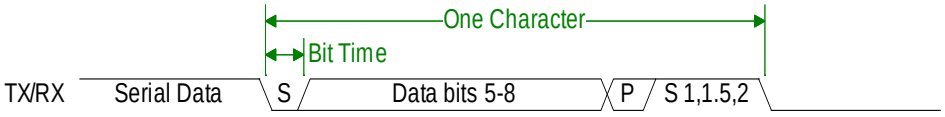


Figure 8-13 UART Serial Data Format

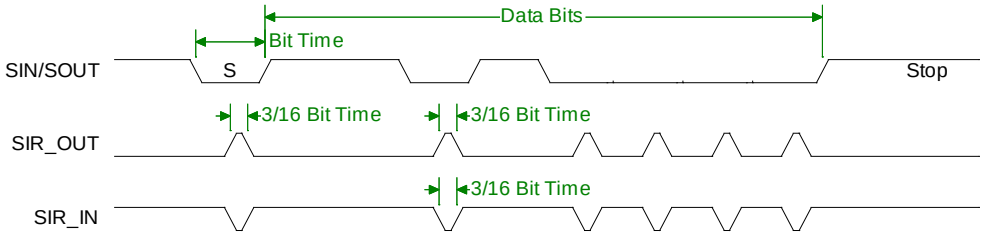


Figure 8-14 Serial IrDA Data Format

8.5.3. UART REGISTER LIST

There are 6 UART controllers in A31. UART1 has full modem control signals, including TX , RX ,RTS, CTS, DTR, DSR, DCD and RING signal. All UART controllers can be configured as Serial IrDA.

Module Name	Base Address
UART0	0x01C28000
UART1	0x01C28400

UART2	0x01C28800
UART3	0x01C28C00
UART4	0x01C29000
UART5	0x01C29400

Register Name	Offset	Description
UART_RBR	0x00	UART Receive Buffer Register
UART_THR	0x00	UART Transmit Holding Register
UART_DLL	0x00	UART Divisor Latch Low Register
UART_DLH	0x04	UART Divisor Latch High Register
UART_IER	0x04	UART Interrupt Enable Register
UART_IIR	0x08	UART Interrupt Identity Register
UART_FCR	0x08	UART FIFO Control Register
UART_LCR	0x0C	UART Line Control Register
UART_MCR	0x10	UART Modem Control Register
UART_LSR	0x14	UART Line Status Register
UART_MSR	0x18	UART Modem Status Register
UART_SCH	0x1C	UART Scratch Register
UART_USR	0x7C	UART Status Register
UART_TFL	0x80	UART Transmit FIFO Level
UART_RFL	0x84	UART_RFL
UART_HALT	0xA4	UART Halt TX Register

8.5.4. UART REGISTER DESCRIPTION

8.5.4.1. UART RECEIVER BUFFER REGISTER

Offset: 0x00	**Register Name: UART_RBR** **Default Value: 0x0000_0000**

Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R	0	RBR Receiver Buffer Register Data byte received on the serial input port (sin) in UART mode, or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set. If in FIFO mode and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an overrun error occurs.

8.5.4.2. UART TRANSMIT HOLDING REGISTER

Offset: 0x00			Register Name: UART_THR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7:0	W	0	THR Transmit Holding Register Data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in FIFO mode and FIFOs are enabled (FCR[0] = 1) and THRE is set, 16 number of characters of data may be written to the THR before the FIFO is full. Any attempt to write data when the FIFO is full results in the write data being lost.

8.5.4.3. UART DIVISOR LATCH LOW REGISTER

Offset: 0x00			Register Name: UART_DLL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7:0	R/W	0	DLL Divisor Latch Low Lower 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate equals to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

8.5.4.4. UART DIVISOR LATCH HIGH REGISTER

Offset: 0x04			Register Name: UART_DLH Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/

7:0	R/W	0	DLH Divisor Latch High Upper 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate equals to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

8.5.4.5. UART INTERRUPT ENABLE REGISTER

Offset: 0x04			**Register Name: UART_IER** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7	R/W		PTIME Programmable THRE Interrupt Mode Enable This is used to enable/disable the generation of THRE Interrupt. 0: Disable 1: Enable
6:4	/	/	/
3	R/W	0	EDSSI Enable Modem Status Interrupt This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority

			interrupt. 0: Disable 1: Enable
2	R/W	0	ELSI Enable Receiver Line Status Interrupt This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0: Disable 1: Enable
1	R/W	0	ETBEI Enable Transmit Holding Register Empty Interrupt This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0: Disable 1: Enable
0	R/W	0	ERBFI Enable Received Data Available Interrupt This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 0: Disable 1: Enable

8.5.4.6. UART INTERRUPT IDENTITY REGISTER

Offset: 0x08			**Register Name: UART_IIR** **Default Value: 0x0000_0001**
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/

7:6	R	0	FEFLAG FIFOs Enable Flag This is used to indicate whether the FIFOs are enabled or disabled. 00: Disable 11: Enable
5:4	/	/	/
3:0	R	0x1	IID Interrupt ID This indicates the highest priority pending interrupt which can be one of the following types: 0000: modem status 0001: no interrupt pending 0010: THR empty 0100: received data available 0110: receiver line status 0111: busy detect 1100: character timeout Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

Interrupt ID	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset
0001	-	None	None	-
0110	Highest	Receiver line status	Overrun/parity/ framing errors or break interrupt	Reading the line status register
0100	Second	Received data available	Receiver data available (non-FIFO mode or FIFOs disabled) or RCVR FIFO trigger level reached (FIFO	Reading the receiver buffer register (non-FIFO mode or FIFOs disabled) or the FIFO

			mode and FIFOs enabled)	drops below the trigger level (FIFO mode and FIFOs enabled)
1100	Second	Character timeout indication	No characters in or out of the RCVR FIFO during the last 4 character times and there is at least 1character in it during This time	Reading the receiver buffer register
0010	Third	Transmit holding register empty	Transmitter holding register empty (Program THRE Mode disabled) or XMIT FIFO at or below threshold (Program THRE Mode enabled)	Reading the IIR register (if source of interrupt); or, writing into THR (FIFOs or THRE Mode not selected or disabled) or XMIT FIFO above threshold (FIFOs and THRE Mode selected and enabled).
0000	Fourth	Modem status	Clear to send or data set ready or ring indicator or data carrier detect. Note that if auto flow control mode is enabled, a change in CTS (that is, DCTS set) does not cause an interrupt.	Reading the Modem status Register
0111	Fifth	Busy detect indication	UART_16550_COMPATIBLE = NO and master has tried to write to the Line Control Register while the UART is busy (USR[0] is set to one).	Reading the UART status register

8.5.4.7. UART FIFO CONTROL REGISTER

Offset: 0x08			Register Name: UART_FCR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**

31:8	/	/	/
7:6	W	0	RT RCVR Trigger This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. 00: 1 character in the FIFO 01: FIFO ¼ full 10: FIFO ½ full 11: FIFO-2 less than full
5:4	W	0	TFT TX Empty Trigger Writes have no effect when THRE_MODE_USER = Disabled. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. It also determines when the dma_tx_req_n signal is asserted when in certain modes of operation. 00: FIFO empty 01: 2 characters in the FIFO 10: FIFO ¼ full 11: FIFO ½ full
3	W	0	DMAM DMA Mode 0: Mode 0 1: Mode 1
2	W	0	XFIFOR XMIT FIFO Reset This resets the control portion of the transmit FIFO and treats the

			FIFO as empty. This also de-asserts the DMA TX request. It is 'self-clearing'. It is not necessary to clear this bit.
1	W	0	RFIFOR RCVR FIFO Reset This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request. It is 'self-clearing'. It is not necessary to clear this bit.
0	W	0	FIFOE Enable FIFOs This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset.

8.5.4.8. UART LINE CONTROL REGISTER

Offset: 0x0C			**Register Name: UART_LCR** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7	R/W	0	DLAB Divisor Latch Access Bit It is writeable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers. 0: Select RX Buffer Register (RBR) / TX Holding Register(THR) and Interrupt Enable Register (IER) 1: Select Divisor Latch LS Register (DLL) and Divisor Latch MS Register (DLM)

6	R/W	0	BC Break Control Bit This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE = Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5:4	R/W	0	EPS Even Parity Select It is writeable only when UART is not busy (USR[0] is zero) and always writable readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). Setting the LCR[5] is uset to reverse the LCR[4]. 00: Odd Parity 01: Even Parity 1X: Reverse LCR[4]
3	R/W	0	PEN Parity Enable It is writeable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0: parity disabled 1: parity enabled
2	R/W	0	STOP Number of stop bits

			It is writeable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 0: 1 stop bit 1: 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit
1:0	R/W	0	DLS Data Length Select It is writeable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits

8.5.4.9. UART MODEM CONTROL REGISTER

Offset: 0x10			**Register Name: UART_MCR** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:7	/	/	/
6	R/W	0	SIRE SIR Mode Enable 0: IrDA SIR Mode disabled

			1: IrDA SIR Mode enabled
5	R/W	0	AFCE Auto Flow Control Enable When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled. 0: Auto Flow Control Mode disabled 1: Auto Flow Control Mode enabled
4	R/W	0	/
3：2	/	/	/
1	R/W	0	RTS Request to Send This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high.In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. 0: rts_n de-asserted (logic 1) 1: rts_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	R/W	0	DTR Data Terminal Ready This is used to directly control the Data Terminal Ready (dtr_n) output.

			The value written to this location is inverted and driven out on dtr_n。 0：dtr_n de-asserted (logic 1) 1：dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.

8.5.4.10. UART LINE STATUS REGISTER

Offset: 0x14			**Register Name: UART_LSR** **Default Value: 0x0000_0060**
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7	R	0	FIFOERR RX Data Error in FIFO When FIFOs are disabled, this bit is always 0. When FIFOs are enabled, this bit is set to 1 when there is at least one PE, FE, or BI in the RX FIFO. It is cleared by a read from the LSR register provided there are no subsequent errors in the FIFO.
6	R	1	TEMT Transmitter Empty If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register and the TX Shift Register are empty. If the FIFOs are enabled, this bit is set whenever the TX FIFO and the TX Shift Register are empty. In both cases, this bit is cleared when a byte is written to the TX data channel.
5	R	1	THRE

			TX Holding Register Empty If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register is empty and ready to accept new data and it is cleared when the CPU writes to the TX Holding Register. If the FIFOs are enabled, this bit is set to "1" whenever the TX FIFO is empty and it is cleared when at least one byte is written to the TX FIFO.
4	R	0	BI Break Interrupt This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of *start time* + *data bits* + *parity* + *stop bits*. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of *start time* + *data bits* + *parity* + *stop bits*. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.
3	R	0	FE Framing Error This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid

			STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0: no framing error 1:framing error Reading the LSR clears the FE bit.
2	R	0	PE Parity Error This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0: no parity error 1: parity error Reading the LSR clears the PE bit.
1	R	0	OE Overrun Error This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was

			read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0: no overrun error 1: overrun error Reading the LSR clears the OE bit.
0	R	0	DR Data Ready This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 0: no data ready 1: data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

8.5.4.11. UART MODEM STATUS REGISTER

Offset: 0x18			**Register Name: UART_MSR** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7	R	0	DCD Line State of Data Carrier Detect This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. 0: dcd_n input is de-asserted (logic 1) 1: dcd_n input is asserted (logic 0)

6	R	0	RI Line State of Ring Indicator This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. 0: ri_n input is de-asserted (logic 1) 1: ri_n input is asserted (logic 0)
5	R	0	DSR Line State of Data Set Ready This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with UART. 0: dsr_n input is de-asserted (logic 1) 1: dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR).
4	R	0	CTS Line State of Clear To Send This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with UART. 0: cts_n input is de-asserted (logic 1) 1: cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS).
3	R	0	DDCD Delta Data Carrier Detect

			This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. 0: no change on dcd_n since last read of MSR 1: change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. Note: Ff the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted.
2	R	0	TERI Trailing Edge Ring Indicator This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. 0: no change on ri_n since last read of MSR 1: change on ri_n since last read of MSR Reading the MSR clears the TERI bit.
1	R	0	DDSR Delta Data Set Ready This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. 0: no change on dsr_n since last read of MSR 1: change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). Note: If the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted.
0	R	0	DCTS Delta Clear to Send

			This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 0: no change on ctsdsr_n since last read of MSR 1: change on ctsdsr_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). Note: If the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset isremoved if the cts_n signal remains asserted.

8.5.4.12. UART SCRATCH REGISTER

Offset: 0x1C			Register Name: UART_SCH Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7:0	R/W	0	SCRATCH_REG Scratch Register This register is for programmers to use as a temporary storage space. It has no defined purpose in the UART.

8.5.4.13. UART STATUS REGISTER

Offset: 0x7C			Register Name: UART_USR Default Value: 0x0000_0006
Bit	**Read/Write**	**Default**	**Description**
31:5	/	/	/
4	R	0	RFF Receive FIFO Full This is used to indicate that the receive FIFO is completely full. 0: Receive FIFO not full

			1: Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.
3	R	0	RFNE Receive FIFO Not Empty This is used to indicate that the receive FIFO contains one or more entries. 0: Receive FIFO is empty 1: Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.
2	R	1	TFE Transmit FIFO Empty This is used to indicate that the transmit FIFO is completely empty. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty.
1	R	1	TFNF Transmit FIFO Not Full This is used to indicate that the transmit FIFO in not full. 0: Transmit FIFO is full 1: Transmit FIFO is not full This bit is cleared when the TX FIFO is full.
0	R	0	BUSY UART Busy Bit 0: Idle or inactive 1: Busy

8.5.4.14. UART TRANSMIT FIFO LEVEL REGISTER

Offset: 0x80	**Register Name: UART_TFL** **Default Value: 0x0000_0000**

Bit	Read/Write	Default	Description
31:7	/	/	/
6:0	R	0	TFL Transmit FIFO Level This indicates the number of data entries in the transmit FIFO.

8.5.4.15. UART RECEIVE FIFO LEVEL REGISTER

Offset: 0x84			Register Name: UART_RFL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:7	/	/	/
6:0	R	0	RFL Receive FIFO Level This indicates the number of data entries in the receive FIFO.

8.5.4.16. UART HALT TX REGISTER

Offset: 0xA4			Register Name: UART_HALT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:6	/	/	/
5	R/W	0	SIR_RX_INVERT SIR Receiver Pulse Polarity Invert 0: Not invert receiver signal 1: Invert receiver signal
4	R/W	0	SIR_TX_INVERT SIR Transmit Pulse Polarity Invert 0: Not invert transmit pulse 1: Invert transmit pulse
3	/	/	/

2	R/W	0	CHANGE_UPDATE After the user using HALT[1] to change the baudrate or LCR configuration, write 1 to update the configuration and waiting this bit self clear to 0 to finish update process. Write 0 to this bit has no effect. 1: Update trigger, Self clear to 0 when finish update.
1	R/W	0	CHCFG_AT_BUSY This is an enable bit for the user to change LCR register configuration (except for the DLAB bit) and baudrate register (DLH and DLL) when the UART is busy (USB[0] is 1). 1: Enable change when busy
0	R/W	0	/

8.5.5. UART SPECIAL REQUIREMENT

8.5.5.1. UART PIN LIST

Port Name	Width	Direction	Description
UART0_TX	1	OUT	UART Serial Bit output
UART0_RX	1	IN	UART Serial Bit input
UART1_TX	1	OUT	UART Serial Bit output
UART1_RX	1	IN	UART Serial Bit input
UART1_RTS	1	OUT	UART Request To Send This active low output signal informs Modem that the UART is ready to send data
UART1_CTS	1	IN	UART Clear To End This active low signal is an input showing when Modem is ready to accept data
UART1_DTR	1	OUT	UART Data Terminal Ready This active low output signal informs Modem that the UART is ready to establish a communication link

UART1_DSR	1	IN	UART Data Set Ready This active low signal is an input indicating when Modem is ready to set up a link with the UART1
UART1_DCD	1	IN	UART Data Carrier Detect This active low signal is an input indicating when Modem has detected a carrier
UART1_RING	1	IN	UART Ring Indicator This active low signal is an input showing when Modem has sensed a ring signal on the telephone line
UART2_TX	1	OUT	UART Serial Bit output
UART2_RX	1	IN	UART Serial Bit input
UART2_RTS	1	OUT	UART Request To Send This active low output signal informs Modem that the UART is ready to send data
UART2_CTS	1	IN	UART Clear To End This active low signal is an input showing when Modem is ready to accept data
UART3_TX	1	OUT	UART Serial Bit output
UART3_RX	1	IN	UART Serial Bit input
UART3_RTS	1	OUT	UART Request To Send This active low output signal informs Modem that the UART is ready to send data
UART3_CTS	1	IN	UART Clear To End This active low signal is an input showing when Modem is ready to accept data
UART4_TX	1	OUT	UART Serial Bit output
UART4_RX	1	IN	UART Serial Bit input
UART5_TX	1	OUT	UART Serial Bit output
UART5_RX	1	IN	UART Serial Bit input

UART5_CTS	1	IN	UART Clear to End
UART5_RTS	1	OUT	UART Request to Send

8.5.5.2. IRDA INVERTED SIGNALS

When the UART is working in IrDA mode (MCR[6]='1'), if HALT[4] is set to '1', the signal is inverted before transferring to pin SOUT and if HALT[5] is set to '1', the signal is inverted after receiving from pin SIN

8.6. CIR

8.6.1. OVERVIEW

The CIR (Consumer IR) interface is used for remote control through infra-red light.

The CIR receiver samples the input signal on the programmable frequency and records these samples into RX FIFO when one CIR signal is found on the air. The CIR receiver uses Run-Length Code (RLC) to encode pulse width. The encoded data is buffered in a 64 levels and 8-bit width RX FIFO; the MSB bit is used to record the polarity of the receiving CIR signal. The high level is represented as '1' while the low level is represented as '0'. The rest 7 bits are used for the length of RLC. The maximum length is 128. If the duration of one level (high or low level) is more than 128, another byte is used.

Since there is always some noise in the air, a threshold can be set to filter the noise to reduce system loading and improve system stability.

The CIR interface features:

- Full physical layer implementation
- Support CIR for remote control or wireless keyboard
- 64x8bits FIFO for data buffer
- Programmable FIFO thresholds

8.6.2. CIR REGISTER LIST

Module Name	Base Address
CIR	0x01F02000

Register Name	Offset	Description
CIR_CTL	0x00	CIR Control Register
CIR_RXCTL	0x10	CIR Receiver Configure Register
CIR_RXFIFO	0x20	CIR Receiver FIFO Register
CIR_RXINT	0x2C	CIR Receiver Interrupt Control Register
CIR_RXSTA	0x30	CIR Receiver Status Register
CIR_CONFIG	0x34	CIR Configure Register

8.6.3. CIR REGISTER DESCRIPTION

8.6.3.1. CIR CONTROL REGISTER

Offset: 0x00			Register Name: CIR_CTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:6	/	/	/
5:4	R/W	0	CIR ENABLE 00~10: Reserved 11: CIR mode enable
3:2	/	/	/.
1	R/W	0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0	GEN Global Enable A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable

8.6.3.2. CIR RECEIVER CONFIGURE REGISTER

Offset: 0x10			Register Name: IR_RXCTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:3	/	/	/
2	R/W	1	RPPI Receiver Pulse Polarity Invert 0: Not invert receiver signal 1: Invert receiver signal
1:0	/	/	/

8.6.3.3. CIR RECEIVER FIFO REGISTER

Offset: 0x20			Register Name: IR_RXFIFO Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7:0	R	0	Receiver Byte FIFO

8.6.3.4. CIR RECEIVER INTERRUPT CONTROL REGISTER

Offset: 0x2C			Register Name: IR_RXINT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:14	/	/	/
13:8	R/W	0	RAL RX FIFO Available Received Byte Level for interrupt TRIGGER_LEVEL = RAL + 1
7:5	/	/	/
4	R/W	0	RAI_EN

			RX FIFO Available Interrupt Enable 0: Disable 1: Enable When set to '1', the Receiver FIFO IRQ is asserted if reaching RAL. The IRQ is de-asserted when condition fails.
3:2	/	/	/
1	R/W	0	RPEI_EN Receiver Packet End Interrupt Enable 0: Disable 1: Enable
0	R/W	0	ROI_EN Receiver FIFO Overrun Interrupt Enable 0: Disable 1: Enable

8.6.3.5. CIR RECEIVER STATUS REGISTER

Offset: 0x30			**Register Name: IR_RXSTA** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:14	/	/	/
13:8	R	0	RAC RX FIFO Available Counter 0: No available data in RX FIFO 1: 1 byte available data in RX FIFO 2: 2 byte available data in RX FIFO … 64: 64 byte available data in RX FIFO
7	R	0x0	STAT Status of CIR

			0x0 – Idle 0x1 – busy
6:5	/	/	/
4	R/W	0	RA RX FIFO Available 0: RX FIFO not available according its level 1: RX FIFO available according its level This bit is cleared by writing a ‘1’.
3:2	/	/	/
1	R/W	0	RPE Receiver Packet End Flag 0: STO was not detected. In CIR mode, one CIR symbol is receiving or not detected. 1: STO field or packet abort symbol (7’b0000,000 and 8’b0000,0000 for MIR and FIR) is detected. In CIR mode, one CIR symbol is received. This bit is cleared by writing a ‘1’.
0	R/W	0	ROI Receiver FIFO Overrun 0: Receiver FIFO not overrun 1: Receiver FIFO overrun This bit is cleared by writing a ‘1’.

8.6.3.6. CIR CONFIGURE REGISTER

Offset: 0x34			**Register Name: IR_CIR** **Default Value: 0x0000_1828**
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:25	/	/	/

24	R/W	0x0	SCS2 Bit2 of Sample Clock Select for CIR This bit is defined by SCS bits below.
23	R/W	0x0	ATHC Active Threshold Control for CIR 0x0 –ATHR in Unit of (Sample Clock) 0x1 –ATHR in Unit of (128*Sample Clocks)
22:16	R/W	0x0	ATHR Active Threshold for CIR These bits control the duration of CIR from Idle to Active State. The duration can be calculated by ((ATHR + 1)*(ATHC? Sample Clock: 128*Sample Clock)).
15:8	R/W	0x18	ITHR Idle Threshold for CIR The Receiver uses it to decide whether the CIR command has been received. If there is no CIR signal on the air, the receiver is staying in IDLE status. One active pulse will bring the receiver from IDLE status to Receiving status. After the CIR is end, the inputting signal will keep the specified level (high or low level) for a long time. The receiver can use this idle signal duration to decide that it has received the CIR command. The corresponding flag is asserted. If the corresponding interrupt is enable, the interrupt line is asserted to CPU. When the duration of signal keeps one status (high or low level) for the specified duration ((ITHR + 1)*128 sample_clk), this means that the previous CIR command has been finished.
7:2	R/W	0xa	NTHR Noise Threshold for CIR When the duration of signal pulse (high or low level) is less than NTHR, the pulse is taken as noise and should be discarded by

<table>
<tr><td></td><td></td><td></td><td>hardware.
0: all samples are recorded into RX FIFO
1: If the signal is only one sample duration, it is taken as noise and discarded.
2: If the signal is less than (<=) two sample duration, it is taken as noise and discarded.
…
61: if the signal is less than (<=) sixty-one sample duration, it is taken as noise and discarded.</td></tr>
<tr><td>1:0</td><td>R/W</td><td>0</td><td>SCS
Sample Clock Select for CIR
<table>
<tr><th>SCS2</th><th>SCS[1]</th><th>SCS[0]</th><th>Sample Clock</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>ir_clk/64</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>ir_clk/128</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ir_clk/256</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>ir_clk/512</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>ir_clk</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
</table>

8.7. USB DRD CONTROLLER

8.7.1. OVERVIEW

The USB DRD is a Dual-Role Device (DRD) controller, which can be configured as a Host-only or Device-only controller, fully compliant with the USB 2.0 Specification. It can support high-speed (HS, 480-Mbps), full-speed (FS, 12-Mbps), and low-speed (LS, 1.5-Mbps) transfers in Host mode, and support high-speed (HS, 480-Mbps), and full-speed (FS, 12-Mbps) in Device mode. Standard USB transceiver can be used through its UTMI+PHY Level3 interface. To save CPU bandwidth, USB DRD DMA interface can support one external DMA controller to take care of the data transfer between the memory and USB DRD FIFO. The USB DRD core also supports USB power saving functions.

The USB2.0 controller features:

- Complies with USB 2.0 Specification
- Supports High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps), and Low-Speed (LS, 1.5-Mbps) in Host mode and support High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps) in Device mode
- Supports the UTMI+ Level 3 interface, the 8-bit bidirectional data buses are used.
- 64-Byte Endpoint 0 buffer for Control Transfer (Endpoint0)
- Supports up to 10 User-Configurable Endpoints for Bulk , Isochronous, Control and Interrupt bi-directional transfers
- Supports up to 8128Byte FIFO for EPs (excluding EP0)
- Supports High-Bandwidth Isochronous & Interrupt transfers
- Automated splitting/combining of packets for Bulk transfers
- Supports point-to-point and point-to-multipoint transfer in both Host and Peripheral mode
- Includes automatic ping capabilities
- Soft connect/disconnect function
- Performs all transaction scheduling in hardware
- Power Optimization and Power Management capabilities

- Includes interface to an external Normal DMA controller; data is transferred between DRAM and FIFO via DMA

8.8. USB HOST CONTROLLER

8.8.1. OVERVIEW

USB Host Controller is fully compliant with the USB 2.0 specification, Enhanced Host Controller Interface (EHCI) Specification, Revision 1.0, and the Open Host Controller Interface (OHCI) Specification Release 1.0a. The controller supports high-speed, 480-Mbps transfers (40 times faster than USB 1.1 full-speed mode) using an EHCI Host controller, as well as full and low speeds through one or more integrated OHCI Host controllers.

The USB host controller includes following features:

- Support industry-standard AMBA High-Performance Bus (AHB) and it is fully compliant with the AMBA Specification, Revision 2.0. Supports bus.
- Support 32-bit Little Endian AMBA AHB Slave Bus for Register Access.
- Support 32-bit Little Endian AMBA AHB Master Bus for Memory Access.
- Include an internal DMA Controller for data transfer with memory.
- Comply with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.
- Support High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps), and Low-Speed (LS, 1.5-Mbps) Device.
- Support the UTMI+ Level 3 interface. The 8-bit bidirectional data buses are used.
- Support only 1 USB Root Port shared between EHCI and OHCI.
- The USB HOST system contains two HCI controllers and a single OHCI controller. The HCI controllers are composed of an EHCI controller and an OHCI companinon controller, while the OHCI controller is a single controller only.

8.8.2. USB HOST BLOCK DIAGRAM

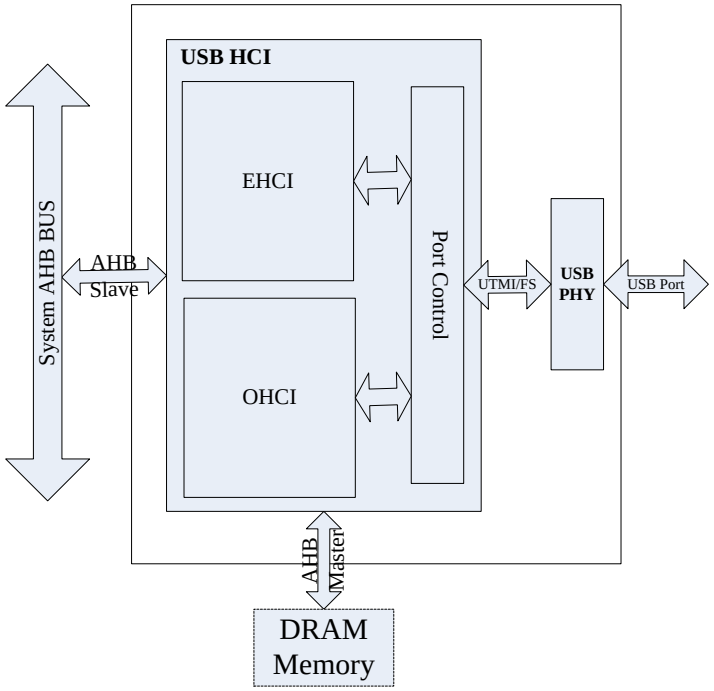


Figure 8-15 USB Host Block Diagram

8.8.3. USB HOST REGISTER LIST

Module Name	Base Address
USB_HCI0	0x01C1A000
USB_HCI1	0x01C1B000
USB_OHCI2	0x01C1C000

Register Name	Offset	Description
EHCI Capability Register		
E_CAPLENGTH	0x000	EHCI Capability register Length Register
E_HCIVERSION	0x002	EHCI Host Interface Version Number Register
E_HCSPARAMS	0x004	EHCI Host Control Structural Parameter Register
E_HCCPARAMS	0x008	EHCI Host Control Capability Parameter Register

E_HCSPPORTROUTE	0x00c	EHCI Companion Port Route Description
EHCI Operational Register		
E_USBCMD	0x010	EHCI USB Command Register
E_USBSTS	0x014	EHCI USB Status Register
E_USBINTR	0x018	EHCI USB Interrupt Enable Register
E_FRINDEX	0x01c	EHCI USB Frame Index Register
E_CTRLDSSEGMENT	0x020	EHCI 4G Segment Selector Register
E_PERIODICLISTBASE	0x024	EHCI Frame List Base Address Register
E_ASYNCLISTADDR	0x028	EHCI Next Asynchronous List Address Register
E_CONFIGFLAG	0x050	EHCI Configured Flag Register
E_PORTSC	0x054	EHCI Port Status/Control Register
OHCI Control and Status Partition Register		
O_HcRevision	0x400	OHCI Revision Register
O_HcControl	0x404	OHCI Control Register
O_HcCommandStatus	0x408	OHCI Command Status Register
O_HcInterruptStatus	0x40c	OHCI Interrupt Status Register
O_HcInterruptEnable	0x410	OHCI Interrupt Enable Register
O_HcInterruptDisable	0x414	OHCI Interrupt Disable Register
OHCI Memory Pointer Partition Register		
O_HcHCCA	0x418	OHCI HCCA Base
O_HcPeriodCurrentED	0x41c	OHCI Period Current ED Base
O_HcControlHeadED	0x420	OHCI Control Head ED Base
O_HcControlCurrentED	0x424	OHCI Control Current ED Base
O_HcBulkHeadED	0x428	OHCI Bulk Head ED Base
O_HcBulkCurrentED	0x42c	OHCI Bulk Current ED Base
O_HcDoneHead	0x430	OHCI Done Head Base
OHCI Frame Counter Partition Register		
O_HcFmInterval	0x434	OHCI Frame Interval Register
O_HcFmRemaining	0x438	OHCI Frame Remaining Register

O_HcFmNumber	0x43c	OHCI Frame Number Register
O_HcPerioddicStart	0x440	OHCI Periodic Start Register
O_HcLSThreshold	0x444	OHCI LS Threshold Register
OHCI Root Hub Partition Register		
O_HcRhDescriptorA	0x448	OHCI Root Hub Descriptor Register A
O_HcRhDesriptorB	0x44c	OHCI Root Hub Descriptor Register B
O_HcRhStatus	0x450	OHCI Root Hub Status Register
O_HcRhPortStatus	0x454	OHCI Root Hub Port Status Register

8.8.4. EHCI REGISTER DESCRIPTION

8.8.4.1. EHCI IDENTIFICATION REGISTER

Offset:0x00			**Register Name: CAPLENGTH** **Default Value: Implementation Dependent**
Bit	**Read/Write**	**Default**	**Description**
7:0	R	0x10	**CAPLENGTH** The value in these bits indicates an offset to add to register base to find the beginning of the Operational Register Space.

8.8.4.2. EHCI HOST INTERFACE VERSION NUMBER REGISTER

Offset: 0x02			**Register Name: HCIVERSION** **Default Value:0x0100**
Bit	**Read/Write**	**Default**	**Description**
15:0	R	0x0100	**HCIVERSION** This is a 16-bits register containing a BCD encoding of the EHCI revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision.

8.8.4.3. EHCI HOST CONTROL STRUCTURAL PARAMETER REGISTER

<table>
<tr><td colspan="3">Offset: 0x04</td><td>Register Name: HCSPARAMS
Default Value: Implementation Dependent</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default</td><td>Description</td></tr>
<tr><td>31:24</td><td>/</td><td>0</td><td>Reserved.
These bits are reserved and should be set to zero.</td></tr>
<tr><td>23:20</td><td>R</td><td>0</td><td>Reserved</td></tr>
<tr><td>19:16</td><td>/</td><td>0</td><td>Reserved.
These bits are reserved and should be set to zero.</td></tr>
<tr><td>15:12</td><td>R</td><td>0</td><td>Number of Companion Controller (N_CC)
This field indicates the number of companion controllers associated with this USB2.0 host controller. A zero in this field indicates there are no companion host controllers. And a value larger than zero in this field indicates there are companion USB1.1 host controller(s).
This field will always be ‘0’.</td></tr>
<tr><td>11:8</td><td>R</td><td>0</td><td>Number of Port per Companion Controller(N_PCC)
This field indicates the number of ports supported per companion host controller host controller. It is used to indicate the port routing configuration to system software.
This field will always fix with ‘0’.</td></tr>
<tr><td>7</td><td>R</td><td>0</td><td>Port Routing Rules
This field indicates the method used by this implementation for how all ports are mapped to companion controllers. The value of this field has the following interpretation:
<table>
<tr><td>Value</td><td>Meaning</td></tr>
<tr><td>0</td><td>The first N_PCC ports are routed to the lowest numbered function companion host controller, the next N_PCC port are routed to the next lowest function companion controller, and so on.</td></tr>
</table></td></tr>
</table>

			<table><tr><td>1</td><td>The port routing is explicitly enumerated by the first N_PORTS elements of the HCSP-PORTTOUTE array.</td></tr></table> This field will always be '0'.
6:4	/	0	**Reserved.** These bits are reserved and should be set to zero.
3:0	R	1	**N_PORTS** This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Valid values are in the range of 0x1 to 0x0f. This field is always 1.

8.8.4.4. EHCI HOST CONTROL CAPABILITY PARAMETER REGISTER

Offset: 0x08			Register Name: HCCPARAMS Default Value: Implementation Dependent
Bit	**Read/Write**	**Default**	**Description**
31:16	/	0	**Reserved** These bits are reserved and should be set to zero.
15:18	R	0	**EHCI Extended Capabilities Pointer (EECP)** This optional field indicates the existence of a capabilities list. A value of 00b indicates no extended capabilities are implemented. A non-zero value in this register indicates the offset in PCI configuration space of the first EHCI extended capabiliby. The pointer value must be 40h or greater if implemented to maintain to consistency of the PCI header defined for this calss of device. The value of this field is always '00b'.
7:4	R		**Isochronous Scheduling Threshold**

			This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. When bit[7] is zero, the value of the least significant 3 bits indicates the number of micro-frames a host controller can hold a set of isochronous data structures(one or more) before flushing the state. When bit[7] is a one, then host software assumes the host controller may cache an isochronous data structure for an entire frame.
3	R	0	**Reserved** These bits are reserved and should be set to zero.
2	R		**Asynchronous Schedule Park Capability** If this bit is set to a one, then the host controller supports the park feature for high-speed queue heads in the Asynchronous Schedule. The feature can be disabled or enabled and set to a specific level by using the Asynchronous Schedule Park Mode Enable and Asynchronous Schedule Park Mode Count fields in the USBCMD register.
1	R		**Programmable Frame List Flag** If this bit is set to a zero, then system software must use a frame list length of 1024 elements with this host controller.The USBCMD register Frame List Size field is a read-only register and should be set to zero. If set to 1,then system software can specify and use the frame list in the USBCMD register Frame List Size field to cofigure the host controller. The frame list must always aligned on a 4K page boundary.This requirement ensures that the frame list is always physically contiguous.

0	R	0	**Reserved** These bits are reserved for future use and should return a value of zero when read.

8.8.4.5. EHCI COMPANION PORT ROUTE DESCRIPTION

Offset: 0x0C			**Register Name: HCSP-PORTROUTE** **Default Value: UNDEFINED**
Bit	**Read/Write**	**Default**	**Description**
31:0	R		**HCSP-PORTROUTE** This optional field is valid only if Port Routing Rules field in HCSPARAMS register is set to a one. This field is used to allow a host controller implementation to explicitly describe to which companion host controller each implemented port is mapped. This field is a 15-element nibble array (each 4 bit is one array element). Each array location corresponds one-to-one with a physical port provided by the host controller (e.g. PORTROUTE [0] corresponds to the first PORTSC port, PORTROUTE [1] to the second PORTSC port, etc.). The value of each element indicates to which of the companion host controllers this port is routed. Only the first N_PORTS elements have valid information. A value of zero indicates that the port is routed to the lowest numbered function companion host controller. A value of one indicates that the port is routed to the next lowest numbered function companion host controller, and so on.

8.8.4.6. EHCI USB COMMAND REGISTER

Offset: 0x10	**Register Name: USBCMD** **Default Value: 0x00080000(0x00080B00 if Asynchronous Schedule Park Capability is a one)**

<table>
<tr><th>Bit</th><th>Read/Write</th><th>Default</th><th>Description</th></tr>
<tr><td>31:24</td><td>/</td><td>0</td><td>Reserved
These bits are reserved and should be set to zero.</td></tr>
<tr><td>23:16</td><td>R/W</td><td>0x08</td><td>Interrupt Threshold Control
The value in this field is used by system software to select the maximum rate at which the host controller will issue interrupts. The only valid values are defined below:
<table>
<tr><td>Value</td><td>Minimum Interrupt Interval</td></tr>
<tr><td>0x00</td><td>Reserved</td></tr>
<tr><td>0x01</td><td>1 micro-frame</td></tr>
<tr><td>0x02</td><td>2 micro-frame</td></tr>
<tr><td>0x04</td><td>4 micro-frame</td></tr>
<tr><td>0x08</td><td>8 micro-frame(default, equates to 1 ms)</td></tr>
<tr><td>0x10</td><td>16 micro-frame(2ms)</td></tr>
<tr><td>0x20</td><td>32 micro-frame(4ms)</td></tr>
<tr><td>0x40</td><td>64 micro-frame(8ms)</td></tr>
</table>
Any other value in this register yields undefined results.
The default value in this field is 0x08 .
Software modifications to this bit while HC Halted bit equals to zero results in undefined behavior.</td></tr>
<tr><td>15:12</td><td>/</td><td>0</td><td>Reserved
These bits are reserved and should be set to zero.</td></tr>
<tr><td>11</td><td>R/W or R</td><td>0</td><td>Asynchronous Schedule Park Mode Enable(OPTIONAL)
If the Asynchronous Park Capability bit in the HCCPARAMS register is a one, then this bit defaults to a 1 and is R/W. Otherwise the bit must be a zero and is Read Only. Software uses this bit to enable or disable Park mode. When this bit is one, Park mode is enabled. When this bit is zero, Park mode is disabled.</td></tr>
<tr><td>10</td><td>/</td><td>0</td><td>Reserved</td></tr>
</table>

			These bits are reserved and should be set to zero.
9:8	R/W or R	0	**Asynchronous Schedule Park Mode Count(OPTIONAL)** Asynchronous Park Capability bit in the HCCPARAMS register is a one, Then this field defaults to 0x3 and is W/R. Otherwise it defaults to zero and is R. It contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the Asynchronous schedule before continuing traversal of the Asynchronous schedule. Valid value are 0x1 to 0x3.Software must not write a zero to this bit when Park Mode Enable is a one as it will result in undefined behavior.
7	R/W	0	**Light Host Controller Reset(OPTIONAL)** This control bit is not required. If implemented, it allows the driver to reset the EHCI controller without affecting the state of the ports or relationship to the companion host controllers. For example, the PORSTC registers should not be reset to their default values and the CF bit setting should not go to zero (retaining port ownership relationships). An host software read of this bit as zero indicates the Light Host Controller Reset has completed and it si safe for software to re-initialize the host controller. A host software read of this bit as a one indicates the Light Host
6	R/W	0	**Interrupt on Async Advance Doorbell** This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Soft- Ware must write a 1 to this bit to ring the doorbell. When the host controller has evicted all appropriate cached schedule

<table>
<tr><td></td><td></td><td></td><td>state, it sets the Interrupt on Async Advance status bit in the USBSTS. if the Interrupt on Async Advance Enable bit in the USBINTR register is a one then the host controller will assert an interrupt at the next interrupt threshold.
The host controller sets this bit to a zero after it has set the Interrupt on Async Advance status bit in the USBSTS register to a one.
Software should not write a one to this bit when the asynchronous schedule is disabled. Doing so will yield undefined results.</td></tr>
<tr><td>5</td><td>R/W</td><td>0</td><td>Asynchronous Schedule Enable
This bit controls whether the host controller skips processing the Asynchronous Schedule. Values mean:<table><tr><td>Bit</td><td>Meaning</td></tr><tr><td>0</td><td>Do not process the Asynchronous Schedule.</td></tr><tr><td>1</td><td>Use the ASYNLISTADDR register to access the Asynchronous Schedule.</td></tr></table>The default value of this field is ‘0b’.</td></tr>
<tr><td>4</td><td>R/W</td><td>0</td><td>Periodic Schedule Enable
This bit controls whether the host controller skips processing the Periodic Schedule. Values mean:<table><tr><td>Bit</td><td>Meaning</td></tr><tr><td>0</td><td>Do not process the Periodic Schedule.</td></tr><tr><td>1</td><td>Use the PERIODICLISTBASE register to access the Periodic Schedule.</td></tr></table>The default value of this field is ‘0b’.</td></tr>
<tr><td>3:2</td><td>R/W or R</td><td>0</td><td>Frame List Size
This field is R/W only if Programmable Frame List Flag in the HCCPARAMS registers is set to a one. This field specifies the size of the
Frame list. The size the frame list controls which bits in the Frame</td></tr>
</table>

<table>
<tr>
<td></td>
<td></td>
<td></td>
<td>Index
Register should be used for the Frame List Current index. Values mean:
<table>
<tr><td>Bits</td><td>Meaning</td></tr>
<tr><td>00b</td><td>1024 elements(4096bytes)Default value</td></tr>
<tr><td>01b</td><td>512 elements(2048byts)</td></tr>
<tr><td>10b</td><td>256 elements(1024bytes)For resource-constrained condition</td></tr>
<tr><td>11b</td><td>reserved</td></tr>
</table>
The default value is ‘00b’.</td>
</tr>
<tr>
<td>1</td>
<td>R/W</td>
<td>0</td>
<td>Host Controller Reset
This control bit is used by software to reset the host controller. The effects of this on Root Hub registers are similar to a Chip Hardware Reset.
When software writes a one to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports.
All operational registers, including port registers and port state machines are set to their initial values. Port ownership reverts to the companion host controller(s). Software must reinitialize the host controller as described in Section 4.1 of the CHEI Specification in order to return the host controller to an operational state.
This bit is set to zero by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a zero to this register.
Software should not set this bit to a one when the HC Halted bit in the USBSTS register is a zero. Attempting to reset an actively running host controller will result in undefined behavior.</td>
</tr>
</table>

0	R/W	0	**Run/Stop** When set to a 1, the Host Controller proceeds with execution of the schedule. When set to 0, the Host Controller completes the current and any actively pipelined transactions on the USB and then halts. The Host Controller must halt within 16 micro-frames after software clears this bit. The HC Halted bit indicates when the Host Controller has finished its pending pipelined transactions and has entered the stopped state. Software must not write a one to this field unless the Host Controller is in the Halt State. The default value is 0x0.

8.8.4.7. EHCI USB STATUS REGISTER

Offset: 0x14			**Register Name: USBSTS** **Default Value: 0x00001000**
Bit	**Read/Write**	**Default**	**Description**
31:16	/	0	**Reserved** These bits are reserved and should be set to zero.
15	R	0	**Asynchronous Schedule Status** The bit reports the current real status of Asynchronous Schedule. If this bit is a zero then the status of the Asynchronous Schedule is disabled. If this bit is a one then the status of the Asynchronous Schedule is enabled. The Host Controller is not required to immediately disable or enable the Asynchronous Schedule when software transitions the Asynchronous Schedule Enable bit in the USBCMD register. When this bit and the Asynchronous Schedule Enable bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0).
14	R	0	**Periodic Schedule Status**

			The bit reports the current real status of the Periodic Schedule. If this bit is a zero then the status of the Periodic Schedule is disabled. If this bit is a one then the status of the Periodic Schedule is enabled. The Host Controller is not required to *immediately* disable or enable the Periodic Schedule when software transitions the *Periodic Schedule Enable* bit in the USBCMD register. When this bit and the *Periodic Schedule Enable* bit are the same value, the Periodic Schedule is either enabled (1) or disabled (0).
13	R	0	**Reclamation** This is a read-only status bit, which is used to detect an empty asynchronous schedule.
12	R	1	**HC Halted** This bit is a zero whenever the Run/Stop bit is a one. The Host Controller Sets this bit to one after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the Host Controller Hardware (e.g. internal error). The default value is '1'.
11:6	/	0	**Reserved** These bits are reserved and should be set to zero.
5	R/WC	0	**Interrupt on Async Advance** System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a one to the Interrupt on Async Advance Doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source.
4	R/WC	0	**Host System Error** The Host Controller set this bit to 1 when a serious error occurs during a host system access involving the Host Controller module. When this error occurs, the Host Controller clears the Run/Stop bit in

			the Command register to prevent further execution of the scheduled TDs.
3	R/WC	0	**Frame List Rollover** The Host Controller sets this bit to a one when the Frame List Index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size is 1024, the Frame Index Register rolls over every time FRINDEX [13] toggles. Similarly, if the size is 512, the Host Controller sets this bit to a one every time FRINDEX [12] toggles.
2	R/WC	0	**Port Change Detect** The Host Controller sets this bit to a one when any port for which the Port Owner bit is set to zero has a change bit transition from a zero to a one or a Force Port Resume bit transition from a zero to a one as a result of a J-K transition detected on a suspended port. This bit will also be set as a result of the Connect Status Chang being set to a one after system software has relinquished ownership of a connected port by writing a one to a port's Port Owner bit.
1	R/WC	0	**USB Error Interrupt(USBERRINT)** The Host Controller sets this bit to 1 when completion of USB transaction results in an error condition(e.g. error counter underflow).If the TD on which the error interrupt occurred also had its IOC bit set, both. This bit and USBINT bit are set.
0	R/WC	0	**USB Interrupt(USBINT)** The Host Controller sets this bit to a one on the completion of a USB transaction, which results in the retirement of a Transfer Descriptor that had its IOC bit set. The Host Controller also sets this bit to 1 when a short packet is detected

			(actual number of bytes received was less than the expected number of bytes)

8.8.4.8. EHCI USB INTERRUPT ENABLE REGISTER

Offset: 0x18			Register Name: USBINTR Default Value:0x00000000
Bit	**Read/Write**	**Default**	**Description**
31:6	/	0	**Reserved** These bits are reserved and should be zero.
5	R/W	0	**Interrupt on Async Advance Enable** When this bit is 1, and the Interrupt on Async Advance bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.
4	R/W	0	**Host System Error Enable** When this bit is 1, and the Host System Error Status bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit.
3	R/W	0	**Frame List Rollover Enable** When this bit is 1, and the Frame List Rollover bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.
2	R/W	0	**Port Change Interrupt Enable** When this bit is 1, and the Port Chang Detect bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Chang Detect bit.
1	R/W	0	**USB Error Interrupt Enable** When this bit is 1, and the USBERRINT bit in the USBSTS register is

			1,the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit.
0	R/W	0	**USB Interrupt Enable** When this bit is 1, and the USBINT bit in the USBSTS register is 1,the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit

8.8.4.9. EHCI FRAME INDEX REGISTER

Offset: 0x1c			**Register Name: FRINDEX** **Default Value: 0x00000000**
Bit	**Read/Write**	**Default**	**Description**
31:14	/	0	**Reserved** These bits are reserved and should be zero.
13:0	R/W	0	**Frame Index** The value in this register increment at the end of each time frame (e.g. micro-frame).Bits[N:3] are used for the Frame List current index. It Means that each location of the frame list is accessed 8 times(frames or Micro-frames) before moving to the next index. The following illustrates Values of N based on the value of the Frame List Size field in the USBCMD register.

USBCMD [Frame List Size]	Number Elements	N
00b	1024	12
01b	512	11

			10b	256	10	
			11b	Reserved		

Notes: This register must be written as a DWord. Byte writes produce undefined results.

8.8.4.10. EHCI PERIODIC FRAME LIST BASE ADDRESS REGISTER

Offset: 0x24			Register Name: PERIODICLISTBASE Default Value: Undefined
Bit	**Read/Write**	**Default**	**Description**
31:12	R/W		**Base Address** These bits correspond to memory address signals [31:12], respectively. This register contains the beginning address of the Periodic Frame List in the system memory. System software loads this register prior to starting the schedule execution by the Host Controller. The memory structure referenced by this physical memory pointer is assumed to be 4-K byte aligned. The contents of this register are combined with the Frame Index Register (FRINDEX) to enable the Host Controller to step through the Periodic Frame List in sequence.
11:0	/		**Reserved** Must be written as 0x0 during runtime, the values of these bits are undefined.

Notes: Writes must be Dword Writes.

8.8.4.11. EHCI CURRENT ASYNCHRONOUS LIST ADDRESS REGISTER

Offset: 0x28			Register Name: ASYNCLISTADDR Default Value: Undefined
Bit	**Read/Write**	**Default**	**Description**
31:5	R/W		**Link Pointer (LP)**

			This field contains the address of the next asynchronous queue head to be executed. These bits correspond to memory address signals [31:5], respectively.
4:0	/	/	**Reserved** These bits are reserved and their value has no effect on operation. Bits in this field cannot be modified by system software and will always return a zero when read.

Notes: Write must be DWord Writes.

8.8.4.12. EHCI CONFIGURE FLAG REGISTER

Offset: 0x50			**Register Name: CONFIGFLAG** **Default Value: 0x00000000**
Bit	**Read/Write**	**Default**	**Description**
31:1	/	0	**Reserved** These bits are reserved and should be set to zero.
0	R/W	0	**Configure Flag(CF)** Host software sets this bit as the last action in its process of configuring the Host Controller. This bit controls the default port-routing control logic as follow: Value: 0 — Port routing control logic default-routs each port to an implementation dependent classic host controller. Value: 1 — Port routing control logic default-routs all ports to this host controller. The default value of this field is '0'.

Notes: This register is not use in the normal implementation.

8.8.4.13. EHCI PORT STATUS AND CONTROL REGISTER

Offset: 0x54			Register Name: PORTSC Default Value: 0x00002000(w/PPC set to one);0x00003000(w/PPC set to a zero)
Bit	**Read/Write**	**Default**	**Description**
31:22	/	0	**Reserved** These bits are reserved for future use and should return a value of zero when read.
21	R/W	0	**Wake on Disconnect Enable(WKDSCNNT_E)** Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. This field is zero if Port Power is zero. The default value in this field is '0'.
20	R/W	0	**Wake on Connect Enable(WKCNNT_E)** Writing this bit to a one enable the port to be sensitive to device connects as wake-up events. This field is zero if Port Power is zero. The default value in this field is '0'.
19:16	R/W	0	**/**
15:14	R/W	0	**Reserved** These bits are reserved for future use and should return a value of zero when read.
13	R/W	1	**Port Owner** This bit unconditionally goes to a 0b when the Configured bit in the CONFIGFLAG register makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configured bit is zero. System software uses this field to release ownership of the port to selected host controller (in the event that the attached device is not a high-speed device).Software writes a one to this bit when the

<table>
<tr><td></td><td></td><td></td><td>attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port.
Default Value = 1b.</td></tr>
<tr><td>12</td><td>/</td><td>0</td><td>Reserved
These bits are reserved for future use and should return a value of zero when read.</td></tr>
<tr><td>11:10</td><td>R</td><td>0</td><td>Line Status
These bits reflect the current logical levels of the D+ (bit11) and D-(bit10) signal lines. These bits are used for detection of low-speed USB devices prior to port reset and enable sequence. This read only field is valid only when the port enable bit is zero and the current connect status bit is set to a one.
The encoding of the bits are:
<table>
<tr><td>Bit[11:10]</td><td>USB State</td><td>Interpretation</td></tr>
<tr><td>00b</td><td>SE0</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
<tr><td>10b</td><td>J-state</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
<tr><td>01b</td><td>K-state</td><td>Low-speed device, release ownership of port.</td></tr>
<tr><td>11b</td><td>Undefined</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
</table>
This value of this field is undefined if Port Power is zero.</td></tr>
<tr><td>9</td><td>/</td><td>0</td><td>Reserved
This bit is reserved for future use, and should return a value of zero when read.</td></tr>
<tr><td>8</td><td>R/W</td><td>0</td><td>Port Reset
1=Port is in Reset. 0=Port is not in Reset. Default value = 0.
When software writes a one to this bit (from a zero), the bus reset</td></tr>
</table>

<table>
<tr><td></td><td></td><td></td><td>sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to ensure the reset sequence, as specified in the USB Specification Revision 2.0, completes. Notes: when software writes this bit to a one , it must also write a zero to the Port Enable bit.
Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detects that the attached device is high-speed during reset, then the host controller must have the port in the enabled state with 2ms of software writing this bit to a zero.
The HC Halted bit in the USBSTS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HC Halted bit is a one.
This field is zero if Port Power is zero.</td></tr>
<tr><td>7</td><td>R/W</td><td>0</td><td>Suspend
Port Enabled Bit and Suspend bit of this register define the port states as follows:
<table>
<tr><td>Bits[Port Enables, Suspend]</td><td>Port State</td></tr>
<tr><td>0x</td><td>Disable</td></tr>
<tr><td>10</td><td>Enable</td></tr>
<tr><td>11</td><td>Suspend</td></tr>
</table>
When in suspend state, downstream propagation of data is blocked</td></tr>
</table>

			on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Not that the bit status does not change until the port is suspend and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when: ① Software sets the Force Port Resume bit to a zero(from a one). ② Software sets the Port Reset bit to a one(from a zero). If host software sets this bit to a one when the port is not enabled(i.e. Port enabled bit is a zero), the results are undefined. This field is zero if Port Power is zero. The default value in this field is '0'.
6	R/W	0	**Force Port Resume** 1 = Resume detected/driven on port. 0 = No resume (K-state) detected/ driven on port. Default value = 0. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspend and software transitions this bit to a one, then the effects on the bus are undefined. Software sets this bit to a 1 drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB

			Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero. This field is zero if Port Power is zero.
5	R/WC	0	**Over-current Change** Default = 0. This bit gets set to a one when there is a change to Over-current Active. Software clears this bit by writing a one to this bit position.
4	R	0	**Over-current Active** 0 = This port does not have an over-current condition. 1 = This port currently has an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed. The default value of this bit is '0'.
3	R/WC	0	**Port Enable/Disable Change** Default = 0. 1 = Port enabled/disabled status has changed. 0 = No change. For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a Port Error). Software clears this bit by writing a 1 to it. This field is zero if Port Power is zero.
2	R/W	0	**Port Enabled/Disabled**

			1=Enable, 0=Disable. Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field. The host controller will only set this bit to a one when the reset sequence determines that the attached device is a high-speed device. Ports can be disabled by either a fault condition(disconnect event or other fault condition) or by host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. When the port is disabled, downstream propagation of data is blocked on this port except for reset. The default value of this field is '0'. This field is zero if Port Power is zero.
1	R/WC	0	**Connect Status Change** 1=Change in Current Connect Status, 0=No change, Default=0. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be "setting" an already-set bit. Software sets this bit to 0 by writing a 1 to it. This field is zero if Port Power is zero.
0	R	0	**Current Connect Status** Device is present on port when the value of this field is a one, and no device is present on port when the value of this field is a zero. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change(Bit 1) to

			be set. This field is zero if Port Power zero.

Notes: This register is only reset by hardware or in response to a host controller reset.

8.8.5. OHCI REGISTER DESCRIPTION

8.8.5.1. HCREVISION REGISTER

Offset: 0x400				**Register Name: HcRevision** **Default Value:0x10**
Bit	**Read/Write**		**Default**	**Description**
	HCD	**HC**		
31:8	/	/	0x00	**Reserved**
7:0	R	R	0x10	**Revision** This read-only field contains the BCD representation of the version of the HCI specification that is implemented by this HC. For example, a value of 0x11 corresponds to version 1.1. All of the HC implementations that are compliant with this specification will have a value of 0x10.

8.8.5.2. HCCONTROL REGISTER

Offset: 0x404				**Register Name: HcRevision** **Default Value:0x0**
Bit	**Read/Write**		**Default**	**Description**
	HCD	**HC**		
31:11	/	/	0x00	**Reserved**
10	R/W	R	0x0	**RemoteWakeupEnable** This bit is used by HCD to enable or disable the remote wakeup feature upon the detection of upstream resume signaling. When this bit is set and the **ResumeDetected** bit in ***HcInterruptStatus***

<table>
<tr><td></td><td></td><td></td><td></td><td>is set, a remote wakeup is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt.</td></tr>
<tr><td>9</td><td>R/W</td><td>R/W</td><td>0x0</td><td>RemoteWakeupConnected
This bit indicates whether HC supports remote wakeup signaling. If remote wakeup is supported and used by the system, it is the responsibility of system firmware to set this bit during POST. HC clear the bit upon a hardware reset but does not alter it upon a software reset. Remote wakeup signaling of the host system is host-bus-specific and is not described in this specification.</td></tr>
<tr><td>8</td><td>R/W</td><td>R</td><td>0x0</td><td>InterruptRouting
This bit determines the routing of interrupts generated by events registered in HcInterruptStatus. If clear, all interrupt are routed to the normal host bus interrupt mechanism. If set interrupts are routed to the System Management Interrupt. HCD clears this bit upon a hardware reset, but it does not alter this bit upon a software reset. HCD uses this bit as a tag to indicate the ownership of HC.</td></tr>
<tr><td>7:6</td><td>R/W</td><td>R/W</td><td>0x0</td><td>HostControllerFunctionalState for USB
<table><tr><td>00b</td><td>USBReset</td></tr><tr><td>01b</td><td>USBResume</td></tr><tr><td>10b</td><td>USBOperational</td></tr><tr><td>11b</td><td>USBSuspend</td></tr></table>A transition to USBOperational from another state causes SOF generation to begin 1 ms later. HCD may determine whether HC has begun sending SOFs by reading the StartoFrame field of HcInterruptStatus.
This field may be changed by HC only when in the USBSUSPEND state. HC may move from the USBSUSPEND state to the USBRESUME state after detecting the resume signaling from a downstream port.</td></tr>
</table>

				HC enters USBSUSPEND after a software reset, whereas it enters USBRESET after a hardware reset. The latter also resets the Root Hub and asserts subsequent reset signaling to downstream ports.
5	R/W	R	0x0	**BulkListEnable** This bit is set to enable the processing of the Bulk list in the next Frame. If cleared by HCD, processing of the Bulk list does not occur after the next SOF. HC checks this bit whenever it determines to process the list. When disabled, HCD may modify the list. If *HcBulkCurrentED* is pointing to an ED to be removed, HCD must advance the pointer by updating *HcBulkCurrentED* before re-enabling processing of the list.
4	R/W	R	0x0	**ControlListEnable** This bit is set to enable the processing of the Control list in the next Frame. If cleared by HCD, processing of the Control list does not occur after the next SOF. HC must check this bit whenever it determines to process the list. When disabled, HCD may modify the list. If *HcControlCurrentED* is pointing to an ED to be removed, HCD must advance the pointer by updating *HcControlCurrentED* before re-enabling processing of the list.
3	R/W	R	0x0	**IsochronousEnable** This bit is used by HCD to enable/disable processing of isochronous EDs. While processing the periodic list in a Frame, HC checks the status of this bit when it finds an Isochronous ED (F=1). If set (enabled), HC continues processing the EDs. If cleared (disabled), HC halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists. Setting this bit is guaranteed to take effect in the next Frame (not

				the current Frame).
2	R/W	R	0x0	**PeriodicListEnable** This bit is set to enable the processing of periodic list in the next Frame. If cleared by HCD, processing of the periodic list does not occur after the next SOF. HC must check this bit before it starts processing the list.
1:0	R/W	R	0x0	**ControlBulkServiceRatio** This specifies the service ratio between Control and Bulk EDs. Before processing any of the nonperiodic lists, HC must compare the ratio specified with its internal count on how many nonempty Control EDs have been processed, in determining whether to continue serving another Control ED or switching to Bulk EDs. The internal count will be retained when crossing the frame boundary. In case of reset, HCD is responsible for restoring this value. CBSR: No. of Control EDs Over Bulk EDs Served 0: 1:1 1: 2:1 2: 3:1 3: 4:1 The default value is 0x0.

8.8.5.3. HCCOMMANDSTATUS REGISTER

Offset: 0x408				Register Name: HcCommandStatus Default Value:0x0
Bit	**Read/Write**		**Default**	**Description**
	HCD	**HC**		
31:18	/	/	0x0	**Reserved**
17:16	R	R/W	0x0	**SchedulingOverrunCount** These bits are incremented on each scheduling overrun error. It is

				initialized to 00b and wraps around at 11b. This will be incremented when a scheduling overrun is detected even if **SchedulingOverrun** in *HcInterruptStatus* has already been set. This is used by HCD to monitor any persistent scheduling problem.
15:4	/	/	0x0	**Reserved**
3	R/W	R/W	0x0	**OwershipChangeRequest** This bit is set by an OS HCD to request a change of control of the HC. When set HC will set the **OwnershipChange** field in *HcInterruptStatus*. After the changeover, this bit is cleared and remains so until the next request from OS HCD.
2	R/W	R/W	0x0	**BulklListFilled** This bit is used to indicate whether there are any TDs on the Bulk list. It is set by HCD whenever it adds a TD to an ED in the Bulk list. When HC begins to process the head of the Bulk list, it checks BLF. As long as **BulkListFilled** is 0, HC will not start processing the Bulk list. If **BulkListFilled** is 1, HC will start processing the Bulk list and will set BF to 0. If HC finds a TD on the list, then HC will set **BulkListFilled** to 1 causing the Bulk list processing to continue. If no TD is found on the Bulk list, and if HCD does not set **BulkListFilled**, then **BulkListFilled** will still be 0 when HC completes processing the Bulk list and Bulk list processing will stop.
1	R/W	R/W	0x0	**ControlListFilled** This bit is used to indicate whether there are any TDs on the Control list. It is set by HCD whenever it adds a TD to an ED in the Control list. When HC begins to process the head of the Control list, it checks CLF. As long as **ControlListFilled** is 0, HC will not start

				processing the Control list. If CF is 1, HC will start processing the Control list and will set **ControlListFilled** to 0. If HC finds a TD on the list, then HC will set **ControlListFilled** to 1 causing the Control list processing to continue. If no TD is found on the Control list, and if the HCD does not set **ControlListFilled**, then **ControlListFilled** will still be 0 when HC completes processing the Control list and Control list processing will stop.
0	R/W	R/E	0x0	**HostControllerReset** This bit is by HCD to initiate a software reset of HC. Regardless of the functional state of HC, it moves to the USBSuspend state in which most of the operational registers are reset except those stated otherwise; e.g, the InteruptRouting field of HcControl, and no Host bus accesses are allowed. This bit is cleared by HC upon the completion of the reset operation. The reset operation must be completed within 10 ms. This bit, when set, should not cause a reset to the Root Hub and no subsequent reset signaling should be asserted to its downstream ports.

8.8.5.4. HCINTERRUPTSTATUS REGISTER

Offset: 0x40c				**Register Name: HcInterruptStatus** **Default Value:0x00**
Bit	**Read/Write**		**Default**	**Description**
	HCD	**HC**		
31:7	/	/	0x0	**Reserved**
6	R/W	R/W	0x0 0x1？	**RootHubStatusChange** This bit is set when the content of *HcRhStatus* or the content of any of *HcRhPortStatus*[**NumberofDownstreamPort**] has changed.

5	R/W	R/W	0x0	**FrameNumberOverflow** This bit is set when the MSb of *HcFmNumber* (bit 15) changes value, from 0 to 1 or from 1 to 0, and after *HccaFrameNumber* has been updated.
4	R/W	R/W	0x0	**UnrecoverableError** This bit is set when HC detects a system error not related to USB. HC should not proceed with any processing nor signaling before the system error has been corrected. HCD clears this bit after HC has been reset.
3	R/W	R/W	0x0	**ResumeDetected** This bit is set when HC detects that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling causing this bit to be set. This bit is not set when HCD sets the USBRseume state.
2	R/W	R/W	0x0	**StartofFrame** This bit is set by HC at each start of frame and after the update of HccaFrameNumber. HC also generates a SOF token at the same time.
1	R/W	R/W	0x0	**WritebackDoneHead** This bit is set immediately after HC has written *HcDoneHead* to *HccaDoneHead*. Further updates of the *HccaDoneHead* will not occur until this bit has been cleared. HCD should only clear this bit after it has saved the content of *HccaDoneHead*.
0	R/W	R/W	0x0	**SchedulingOverrun** This bit is set when the USB schedule for the current Frame overruns and after the update of *HccaFrameNumber*. A scheduling overrun will also cause the **SchedulingOverrunCount** of *HcCommandStatus* to be Incremented.

8.8.5.5. HCINTERRUPTENABLE REGISTER

Offset: 0x410			Register Name: HcInterruptEnable Register Default Value: 0x0
Bit	Read/Write	Default	Description
	HCD / HC		
31	R/W / R	0x0	**MasterInterruptEnable** A '0' writtern to this field is ignored by HC. A '1' written to this field enables interrupt generation due to events specified in the other bits of this register. This is used by HCD as Master Interrupt Enable.
30:7	/ / /	0x0	**Reserved**
6	R/W / R	0x0	**RootHubStatusChange Interrupt Enable** 0 Ignore; 1 Enable interrupt generation due to Root Hub Status Change;
5	R/W / R	0x0	**FrameNumberOverflow Interrupt Enable** 0 Ignore; 1 Enable interrupt generation due to Frame Number Over Flow;
4	R/W / R	0x0	**UnrecoverableError Interrupt Enable** 0 Ignore; 1 Enable interrupt generation due to Unrecoverable Error;
3	R/W / R	0x0	**ResumeDetected Interrupt Enable** 0 Ignore; 1 Enable interrupt generation due to Resume Detected;
2	R/W / R	0x0	**StartofFrame Interrupt Enable** 0 Ignore; 1 Enable interrupt generation due to Start of Flame;
1	R/W / R	0x0	**WritebackDoneHead Interrupt Enable**

				0 Ignore; 1 Enable interrupt generation due to Write back Done Head;
0	R/W	R	0x0	**SchedulingOverrun Interrupt Enable** 0 Ignore; 1 Enable interrupt generation due to Scheduling Overrun;

8.8.5.6. HCINTERRUPTDISABLE REGISTER

Offset: 0x414				**Register Name: HcInterruptDisable Register** **Default Value: 0x0**
Bit	**Read/Write**		**Default**	**Description**
	HCD	**HC**		
31	R/W	R	0x0	**MasterInterruptEnable** A written '0' to this field is ignored by HC. A '1' written to this field disables interrupt generation due events specified in the other bits of this register. This field is set after a hardware or software reset.
30:7	/	/	0x00	**Reserved**
6	R/W	R	0x0	**RootHubStatusChange Interrupt Disable** 0 Ignore; 1 Disable interrupt generation due to Root Hub Status Change;
5	R/W	R	0x0	**FrameNumberOverflow Interrupt Disable** 0 Ignore; 1 Disable interrupt generation due to Frame Number Over Flow;
4	R/W	R	0x0	**UnrecoverableError Interrupt Disable** 0 Ignore; 1 Disable interrupt generation due to Unrecoverable Error;
3	R/W	R	0x0	**ResumeDetected Interrupt Disable**

				0 Ignore; 1 Disable interrupt generation due to Resume Detected;
2	R/W	R	0x0	**StartofFrame Interrupt Disable** 0 Ignore; 1 Disable interrupt generation due to Start of Flame;
1	R/W	R	0x0	**WritebackDoneHead Interrupt Disable** 0 Ignore; 1 Disable interrupt generation due to Write back Done Head;
0	R/w	R	0x0	**SchedulingOverrun Interrupt Disable** 0 Ignore; 1 Disable interrupt generation due to Scheduling Overrun;

8.8.5.7. HCHCCA REGISTER

Offset: 0x418				**Register Name: HcHCCA** **Default Value:0x0**
Bit	**Read/Write**		**Default**	**Description**
	HCD	**HC**		
31:8	R/W	R	0x0	**HCCA[31:8]** This is the base address of the Host Controller Communication Area. This area is used to hold the control structures and the Interrupt table that are accessed by both the Host Controller and the Host Controller Driver.
7:0	R	R	0x0	**HCCA[7:0]** The alignment restriction in HcHCCA register is evaluated by examining the number of zeros in the lower order bits. The minimum alignment is 256 bytes, therefore, bits 0 through 7 must always return 0 when read.

8.8.5.8. HCPERIODCURRENTED REGISTER

Offset: 0x41c			Register Name: HcPeriodCurrentED(PCED) Default Value: 0x0
Bit	Read/Write	Default	Description
	HCD HC		
31:4	R R/W	0x0	**PCED[31:4]** This is used by HC to point to the head of one of the Periodec list which will be processed in the current Frame. The content of this register is updated by HC after a periodic ED has been processed. HCD may read the content in determining which ED is currently being processed at the time of reading.
3:0	R R	0x0	**PCED[3:0]** Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.8.5.9. HCCONTROLHEADED REGISTER

Offset: 0x420			Register Name: HcControlHeadED[CHED] Default Value: 0x0
Bit	Read/Write	Default	Description
	HCD HC		
31:4	R/W R	0x0	**EHCD[31:4]** The HcControlHeadED register contains the physical address of the first Endpoint Descriptor of the Control list. HC traverse the Control list starting with the HcControlHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0	R R	0x0	**EHCD[3:0]** Because the general TD length is 16 bytes, the memory structure for

				the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.8.5.10. HCCONTROLCURRENTED REGISTER

Offset: 0x424				Register Name: HcControlCurrentED[CCED] Default Value: 0x0
Bit	Read/Write		Default	Description
	HCD	HC		
31:4	R/W	R/W	0x0	**CCED[31:4]** The pointer is advanced to the next ED after serving the present one. HC will continue processing the list from where it left off in the last Frame. When it reaches the end of the Control list, HC checks the ControlListFilled of in HcCommandStatus. If set, it copies the content of HcControlHeadED to HcControlCurrentED and clears the bit. If not set, it does nothing. HCD is allowed to modify this register only when the ControlListEnable of HcControl is cleared. When set, HCD only reads the instantaneous value of this register. Initially, this is set to zero to indicate the end of the Control list.
3:0	R	R	0x0	**CCED[3:0]** Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.8.5.11. HCBULKHEADED REGISTER

Offset: 0x428				Register Name: HcBulkHeadED[BHED] Default Value: 0x0
Bit	Read/Write		Default	Description
	HCD	HC		

31:4	R/W	R	0x0	**BHED[31:4]** The HcBulkHeadED register contains the physical address of the first Endpoint Descriptor of the Bulk list. HC traverses the Bulk list starting with the HcBulkHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0	R	R	0x0	**BHED[3:0]** Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.8.5.12. HCBULKCURRENTED REGISTER

Offset: 0x42c			**Register Name: HcBulkCurrentED [BCED]** **Default Value: 0x00**
Bit	**Read/Write**	**Default**	**Description**
	HCD **HC**		
31:4	R/W R/W	0x0	**BulkCurrentED[31:4]** This is advanced to the next ED after the HC has served the present one. HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, HC checks the **ControlListFilled** of HcControl. If set, it copies the content of *HcBulkHeadED* to *HcBulkCurrentED* and clears the bit. If it is not set, it does nothing. HCD is only allowed to modify this register when the **BulkListEnable** of *HcControl* is cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to zero to indicate the end of the Bulk list.
3:0	R R	0x0	**BulkCurrentED [3:0]** Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.8.5.13. HCDONEHEAD REGISTER

Offset: 0x430			Register Name: HcDoneHead Default Value: 0x00
Bit	Read/Write	Default	Description
	HCD HC		
31:4	R R/W	0x0	**HcDoneHead[31:4]** When a TD is completed, HC writes the content of *HcDoneHead* to the NextTD field of the TD. HC then overwrites the content of *HcDoneHead* with the address of this TD. This is set to zero whenever HC writes the content of this register to HCCA. It also sets the **WritebackDoneHead** of *HcInterruptStatus*.
3:0	R R	0x0	**HcDoneHead[3:0]** Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.8.5.14. HCFMINTERVAL REGISTER

Offset: 0x434			Register Name: HcFmInterval Register Default Value: 0x2EDF
Bit	Read/Write	Default	Description
	HCD HC		
31	R/W R	0x0	**FrameIntervalToggler** HCD toggles this bit whenever it loads a new value to **FrameInterval**.
30:16	R/W R	0x0	**FSLargestDataPacket** This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or

				received by the HC in a single transaction at any given time without causing scheduling overrun. The field value is calculated by the HCD.
15:14	/	/	0x0	**Reserved**
13:0	R/W	R	0x2edf	**FrameInterval** This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to be 11,999. HCD should store the current value of this field before resetting HC. By setting the **HostControllerReset** field of *HcCommandStatus* as this will cause the HC to reset this field to its nominal value. HCD may choose to restore the stored value upon the completion of the Reset sequence.

8.8.5.15. HCFMREMAINING REGISTER

Offset: 0x438				Register Name: HcFmRemaining Default Value: 0x0
Bit	**Read/Write**		**Default**	**Description**
	HCD	**HC**		
31	R	R/W	0x0	**FrameRemaining Toggle** This bit is loaded from the **FrameIntervalToggle** field of *HcFmInterval* whenever **FrameRemaining** reaches 0. This bit is used by HCD for the synchronization between **FrameInterval** and **FrameRemaining**.
30:14	/	/	0x0	**Reserved**
13:0	R	RW	0x0	**FramRemaining** This counter is decremented at each bit time. When it reaches zero, it is reset by loading the FrameInterval value specified in *HcFmInterval* at the next bit time boundary. When entering the USBOPERATIONAL state, HC re-loads the content with the

				FrameInterval of *HcFmInterval* and uses the updated value from the next SOF.

8.8.5.16. HCFMNUMBER REGISTER

Offset: 0x43c				Register Name: HcFmNumber Default Value:0x0
Bit	**Read/Write**		**Default**	**Description**
	HCD	**HC**		
31:16				**Reserved**
15:0	R	R/W	0x0	**FrameNumber** This is incremented when *HcFmRemaining* is re-loaded. It will be rolled over to 0x0 after 0x0ffff. When entering the USBOPERATIONAL state, this will be incremented automatically. The content will be written to HCCA after HC has incremented the **FrameNumber** at each frame boundary and sent a SOF but before HC reads the first ED in that Frame. After writing to HCCA, HC will set the **StartofFrame** in *HcInterruptStatus.*

8.8.5.17. HCPERIODICSTART REGISTER

Offset: 0x440				Register Name: HcPeriodicStatus Default Value: 0x0
Bit	**Read/Write**		**Default**	**Description**
	HCD	**HC**		
31:14				**Reserved**
13:0	R/W	R	0x0	**PeriodicStart** After a hardware reset, this field is cleared. This is then set by HCD during the HC initialization. The value is calculated roughly as 10% off from *HcFmInterval*. A typical value will be 0x2A3F (0x3e67??). When *HcFmRemaining* reaches the value specified, processing of

				the periodic lists will have priority over Control/Bulk processing. HC will therefore start processing the Interrupt list after completing the current Control or Bulk transaction that is in progress.

8.8.5.18. HCLSTHRESHOLD REGISTER

Offset: 0x444				Register Name: HcLSThreshold Default Value: 0x0628
Bit	**Read/Write**		**Default**	**Description**
	HCD	**HC**		
31:12				**Reserved**
11:0	R/W	R	0x0628	**LSThreshold** This field contains a value which is compared to the **FrameRemaining** field prior to initiating a Low Speed transaction. The transaction is started only if **FrameRemaining** ³ this field. The value is calculated by HCD with the consideration of transmission and setup overhead.

8.8.5.19. HCRHDESCRIPTORA REGISTER

Offset: 0x448				Register Name: HcRhDescriptorA Default Value:
Bit	**Read/Write**		**Default**	**Description**
	HCD	**HC**		
31:24	R/W	R	0x2	**PowerOnToPowerGoodTime[POTPGT]** This byte specifies the duration HCD has to wait before accessing a powered-on port of the Root Hub. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as POTPGT * 2ms.
23:13				**Reserved**
12	R/W	R	1	**NoOverCurrentProtection** This bit describes how the overcurrent status for the Root Hub ports

<table>
<tr><td></td><td></td><td></td><td></td><td>are reported. When this bit is cleared, the OverCurrentProtectionMode field specifies global or per-port reporting.<table><tr><td>0</td><td>Over-current status is reported collectively for all downstream ports.</td></tr><tr><td>1</td><td>No overcurrent protection supported.</td></tr></table></td></tr>
<tr><td>11</td><td>R/W</td><td>R</td><td>0</td><td>OverCurrentProtectionMode
This bit describes how the overcurrent status for the Root Hub ports are reported. At reset, these fields should reflect the same mode as PowerSwitchingMode. This field is valid only if the NoOverCurrentProtection field is cleared.<table><tr><td>0</td><td>Over-current status is reported collectively for all downstream ports.</td></tr><tr><td>1</td><td>Over-current status is reported on per-port basis.</td></tr></table></td></tr>
<tr><td>10</td><td>R</td><td>R</td><td>0x0</td><td>Device Type
This bit specifies that the Root Hub is not a compound device. The Root Hub is not permitted to be a compound device. This field should always read/write 0.</td></tr>
<tr><td>9</td><td>R/W</td><td>R</td><td>1</td><td>PowerSwitchingMode
This bit is used to specify how the power switching of the Root Hub ports is controlled. It is implementation-specific. This field is only valid if the NoPowerSwitching field is cleared.<table><tr><td>0</td><td>All ports are powered at the same time.</td></tr><tr><td>1</td><td>Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port
switching. If the PortPowerControlMask bit is set, the port responds only to port power commands (Set/ClearPortPower). If the port mask is cleared, then</td></tr></table></td></tr>
</table>

				the port is controlled only by the global power switch (**Set/ClearGlobalPower**).
8	R/W	R	0	**NoPowerSwithcing** These bits are used to specify whether power switching is supported or ports are always powered. It is implementation-specific. When this bit is cleared, the **PowerSwitchingMode** specifies global or per-port switching. **0** Ports are power switched. **1** Ports are always powered on when the HC is powered on.
7:0	R	R	0x01	**NumberDownstreamPorts** These bits specify the number of downstream ports supported by the Root Hub. It is implementation-specific. The minimum number of ports is 1. The maximum number of ports supported.

8.8.5.20. HCRHDESCRIPTORB REGISTER

Offset: 0x44c				**Register Name: HcRhDescriptorB Register** **Default Value:**
Bit	**Read/Write**		**Default**	**Description**
	HCD	**HC**		
31:16	R/W	R	0x0	**PortPowerControlMask** Each bit indicates if a port is affected by a global power control command when **PowerSwitchingMode** is set. When set, the port's power state is only affected by per-port power control (**Set/ClearPortPower**). When cleared, the port is controlled by the global power switch (**Set/ClearGlobalPower**). If the device is configured to global switching mode (**PowerSwitchingMode** = 0), this field is not valid. Bit0 Reserved

				Bit1 Ganged-power mask on Port #1. Bit2 Ganged-power mask on Port #2. … Bit15 Ganged-power mask on Port #15.
15:0	R/W	R	0x0	**DeviceRemovable** Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable. Bit0 Reserved Bit1 Device attached to Port #1. Bit2 Device attached to Port #2. … Bit15 Device attached to Port #15.

8.8.5.21. HCRHSTATUS REGISTER

Offset: 0x450			**Register Name: HcRhStatus Register** **Default Value:**
Bit	**Read/Write**	**Default**	**Description**
	HCD **HC**		
31	W R	0	**(write)ClearRemoteWakeupEnable** Write a ‘1’ clears **DeviceRemoteWakeupEnable.** Write a ‘0’ has no effect.
30:18	/ /	0x0	**Reserved**
17	R/W R	0	**OverCurrentIndicatorChang** This bit is set by hardware when a change has occurred to the **OverCurrentIndicator** field of this register. The HCD clears this bit by writing a ‘1’.Writing a ‘0’ has no effect.
16	R/W R	0x0	**(read)LocalPowerStartusChange** The Root Hub does not support the local power status features,

<table>
<tr><td></td><td></td><td></td><td></td><td>thus, this bit is always read as ‘0’.
(write)SetGlobalPower
In global power mode (PowerSwitchingMode=0), This bit is written to ‘1’ to turn on power to all ports (clear PortPowerStatus). In per-port power mode, it sets PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a ‘0’ has no effect.</td></tr>
<tr><td>15</td><td>R/W</td><td>R</td><td>0x0</td><td>(read)DeviceRemoteWakeupEnable
This bit enables a ConnectStatusChange bit as a resume event, causing a USBSUSPEND to USBRESUME state transition and setting the ResumeDetected interrupt.
<table>
<tr><td>0</td><td>ConnectStatusChange is not a remote wakeup event.</td></tr>
<tr><td>1</td><td>ConnectStatusChange is a remote wakeup event.</td></tr>
</table>
(write)SetRemoteWakeupEnable
Writing a ‘1’ sets DeviceRemoveWakeupEnable. Writing a ‘0’ has no effect.</td></tr>
<tr><td>14:2</td><td></td><td></td><td></td><td>Reserved</td></tr>
<tr><td>1</td><td>R</td><td>R/W</td><td>0x0</td><td>OverCurrentIndicator
This bit reports overcurrent conditions when the global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal.
If per-port overcurrent protection is implemented this bit is always ‘0’</td></tr>
<tr><td>0</td><td>R/W</td><td>R</td><td>0x0</td><td>(Read)LocalPowerStatus
When read, this bit returns the LocalPowerStatus of the Root Hub. The Root Hub does not support the local power status feature; thus, this bit is always read as ‘0’.
(Write)ClearGlobalPower</td></tr>
</table>

				When write, this bit is operated as the ClearGlobalPower. In global power mode (**PowerSwitchingMode**=0), This bit is written to '1' to turn off power to all ports (clear **PortPowerStatus**). In per-port power mode, it clears **PortPowerStatus** only on ports whose **PortPowerControlMask** bit is not set. Writing a '0' has no effect.

8.8.5.22. HCRHPORTSTATUS REGISTER

Offset: 0x454				**Register Name: HcRhPortStatus** **Default Value: 0x100**
Bit	**Read/Write**		**Default**	**Description**
	HCD	**HC**		
31:21	/	/	0x0	**Reserved**
20	R/W	R/W	0x0	**PortResetStatusChange** This bit is set at the end of the 10-ms port reset signal. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 – port reset is not complete 1 – port reset is complete
19	R/W	R/W	0x0	**PortOverCurrentIndicatorChange** This bit is valid only if overcurrent conditions are reported on a per-port basis. This bit is set when Root Hub changes the **PortOverCurrentIndicator** bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 – no change in **PortOverCurrentIndicator** 1 – **PortOverCurrentIndicator** has changed
18	R/W	R/W	0x0	**PortSuspendStatusChange** This bit is set when the full resume sequence has been completed. This sequence includes the 20-s resume pulse, LS EOP, and 3-ms resychronization delay. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. This bit is also cleared when

<table>
<tr><td></td><td></td><td></td><td></td><td>ResetStatusChange is set.<table><tr><td>0</td><td>resume is not completed</td></tr><tr><td>1</td><td>resume completed</td></tr></table></td></tr>
<tr><td>17</td><td>R/W</td><td>R/W</td><td>0x0</td><td>PortEnableStatusChange
This bit is set when hardware events cause the PortEnableStatus bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a ‘1’ to clear this bit. Writing a ‘0’ has no effect.<table><tr><td>0</td><td>no change in PortEnableStatus</td></tr><tr><td>1</td><td>change in PortEnableStatus</td></tr></table></td></tr>
<tr><td>16</td><td>R/W</td><td>R/W</td><td>0x0</td><td>ConnectStatusChange
This bit is set whenever a connect or disconnect event occurs. The HCD writes a ‘1’ to clear this bit. Writing a ‘0’ has no effect. If CurrentConnectStatus is cleared when a SetPortReset,SetPortEnable, or SetPortSuspend write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected.<table><tr><td>0</td><td>no change in PortEnableStatus</td></tr><tr><td>1</td><td>change in PortEnableStatus</td></tr></table>Notes:
If the DeviceRemovable[NDP] bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.</td></tr>
<tr><td>15:10</td><td>/</td><td>/</td><td>0x0</td><td>Reserved</td></tr>
<tr><td>9</td><td>R/W</td><td>R/W</td><td>-</td><td>(read)LowSpeedDeviceAttached
This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid</td></tr>
</table>

<table>
<tr><td></td><td></td><td></td><td></td><td>only when the CurrentConnectStatus is set.
<table><tr><td>0</td><td>full speed device attached</td></tr><tr><td>1</td><td>low speed device attached</td></tr></table>
(write)ClearPortPower
The HCD clears the PortPowerStatus bit by writing a ‘1’ to this bit. Writing a ‘0’ has no effect.</td></tr>
<tr><td>8</td><td>R/W</td><td>R/W</td><td>0x1</td><td>(read)PortPowerStatus
This bit reflects the port’s power status, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. HCD sets this bit by writing SetPortPower or SetGlobalPower. HCD clears this bit by writing ClearPortPower or ClearGlobalPower. Which power control switches are enabled is determined by PowerSwitchingMode and PortPortControlMask[NumberDownstreamPort]. In global switching mode(PowerSwitchingMode=0), only Set/ClearGlobalPower controls
this bit. In per-port power switching (PowerSwitchingMode=1), if the PortPowerControlMask[NDP] bit for the port is set, only Set/ClearPortPower commands are enabled. If the mask is not set, only Set/ClearGlobalPower commands are enabled. When port power is disabled, CurrentConnectStatus, PortEnableStatus, PortSuspendStatus, and PortResetStatus should be reset.
<table><tr><td>0</td><td>port power is off</td></tr><tr><td>1</td><td>port power is on</td></tr></table>
(write)SetPortPower
The HCD writes a ‘1’ to set the PortPowerStatus bit. Writing a ‘0’</td></tr>
</table>

<table>
<tr><td></td><td></td><td></td><td></td><td>has no effect.

Notes:
This bit is always reads ‘1b’ if power switching is not supported.</td></tr>
<tr><td>7:5</td><td>/</td><td>/</td><td>0x0</td><td>Reserved</td></tr>
<tr><td>4</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortResetStatus
When this bit is set by a write to SetPortReset, port reset signaling is asserted. When reset is completed, this bit is cleared when PortResetStatusChange is set. This bit cannot be set if CurrentConnectStatus is cleared.
<table><tr><td>0</td><td>port reset signal is not active</td></tr><tr><td>1</td><td>port reset signal is active</td></tr></table>
(write)SetPortReset
The HCD sets the port reset signaling by writing a ‘1’ to this bit. Writing a ‘0’ has no effect. If CurrentConnectStatus is cleared, this write does not set PortResetStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to reset a disconnected port.</td></tr>
<tr><td>3</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortOverCurrentIndicator
This bit is only valid when the Root Hub is configured in such a way that overcurrent conditions are reported on a per-port basis. If per-port overcurrent reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. This bit always reflects the overcurrent input signal.
<table><tr><td>0</td><td>no overcurrent condition.</td></tr><tr><td>1</td><td>overcurrent condition detected.</td></tr></table></td></tr>
</table>

<table>
<tr><td></td><td></td><td></td><td></td><td>(write)ClearSuspendStatus
The HCD writes a ‘1’ to initiate a resume. Writing a ‘0’ has no effect. A resume is initiated only if PortSuspendStatus is set.</td></tr>
<tr><td>2</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortSuspendStatus
This bit indicates the port is suspended or in the resume sequence. It is set by a SetSuspendState write and cleared when PortSuspendStatusChange is set at the end of the resume interval. This bit cannot be set if CurrentConnectStatus is cleared. This bit is also cleared when PortResetStatusChange is set at the end of the port reset or when the HC is placed in the USBRESUME state. If an upstream resume is in progress, it should propagate to the HC.
<table>
<tr><td>0</td><td>port is not suspended</td></tr>
<tr><td>1</td><td>port is suspended</td></tr>
</table>
(write)SetPortSuspend
The HCD sets the PortSuspendStatus bit by writing a ‘1’ to this bit. Writing a ‘0’ has no effect. If CurrentConnectStatus is cleared, this write does not set PortSuspendStatus; instead it sets ConnectStatusChange. This informs the driver that it attempted to suspend a disconnected port.</td></tr>
<tr><td>1</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortEnableStatus
This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes PortEnabledStatusChange to be set. HCD sets this bit by writing SetPortEnable and clears it by writing ClearPortEnable. This bit cannot be set when CurrentConnectStatus is cleared. This bit is</td></tr>
</table>

<table>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>also set, if not already, at the completion of a port reset when ResetStatusChange is set or port suspend when SuspendStatusChange is set.
<table>
<tr><td>0</td><td>port is disabled</td></tr>
<tr><td>1</td><td>port is enabled</td></tr>
</table>
(write)SetPortEnable
The HCD sets PortEnableStatus by writing a ‘1’. Writing a ‘0’ has no effect. If CurrentConnectStatus is cleared, this write does not set PortEnableStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to enable a disconnected Port.</td>
</tr>
<tr>
<td>0</td>
<td>R/W</td>
<td>R/W</td>
<td>0x0</td>
<td>(read)CurrentConnectStatus
This bit reflects the current state of the downstream port.
<table>
<tr><td>0</td><td>No device connected</td></tr>
<tr><td>1</td><td>Device connected</td></tr>
</table>
(write)ClearPortEnable
The HCD writes a ‘1’ to clear the PortEnableStatus bit. Writing ‘0’ has no effect. The CurrentConnectStatus is not affected by any write.

Notes:
This bit is always read ‘1’ when the attached device is nonremovable (Device Removable [NumberDownstreamPort]).</td>
</tr>
</table>

8.9. DIGITAL AUDIO INTERFACE

8.9.1. OVERVIEW

The Digital Audio Interface can be configured as I2S interface or PCM interface by software. When configured as I2S interface, it can support the industry standard format for I2S, left-justified, or right-justified. PCM is a standard method used to digital audio for transmission over digital communication channels. It supports linear 13 or 16-bits linear, or 8-bit u-law or A-law companded sample formats at 8K samples/s and can receive and transmit on any selection of four of the first four slots following PCM_SYNC.

It includes the following features:

- Comply with industry standard I2S/PCM specification
- 2 sets of I2S/PCM Interfaces for Baseband and Bluetooth

I2S interface:

- Support 16/20/24 data resolution
- Support full-duplex synchronous serial interface
- Support master/slave mode operation configured by software
- Support audio sample rate from 8KHz to 192KHz
- Support standard I2S, Left Justified and Right Justified
- Support 8-channel output and 2-channel input

PCM interface:

- Support 8/16-bit linear sample, 8-bit u-law and a-law companded sample
- Support full-duplex synchronous serial interface
- Support master/slave mode operation configured by software
- Support audio sample rate from 8KHz to 192KHz
- Support any start selection of 4 slots(8/16-bit width) following SYNC signal
- Support MCLK output for CODEC chips whether controller in slave or master mode
- Support codec, Baseband or Bluetooth communication

- Separate transmit and receive FIFOs for buffered read or write operations

8.9.2. DIGITAL AUDIO BLOCK DIAGRAM

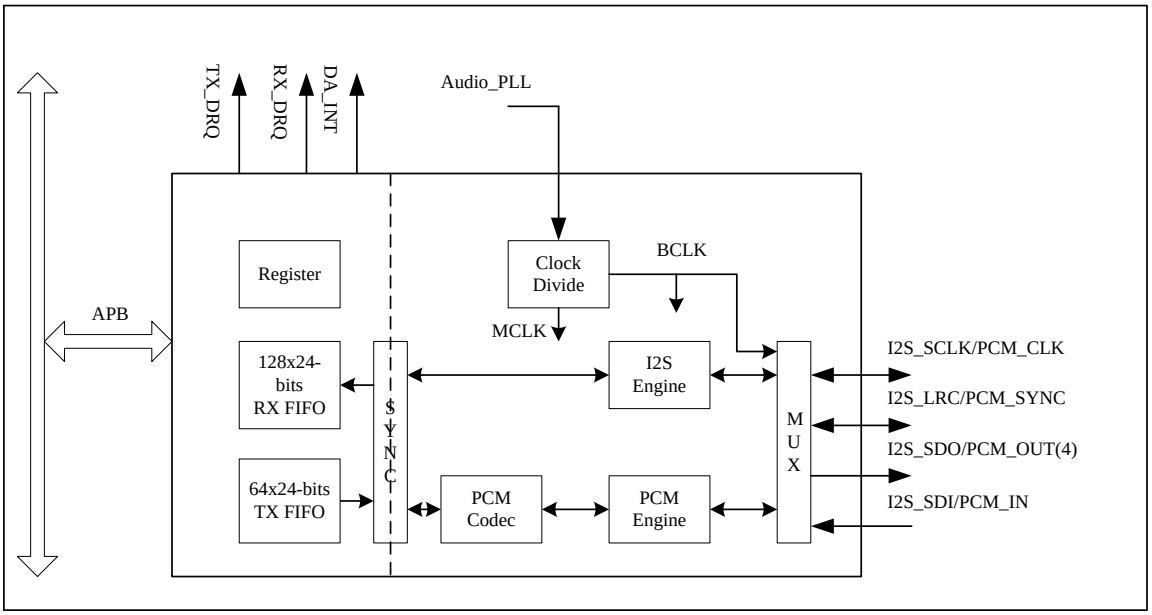


Figure 8-16 Digital Audio Block Diagram

8.9.3. DIGITAL AUDIO INTERFACE TIMING DIAGRAM

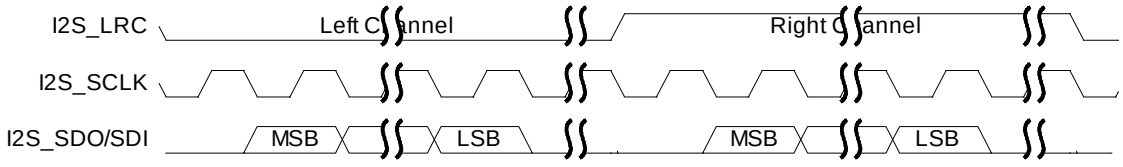


Figure 8-17 I2S Timing Diagram

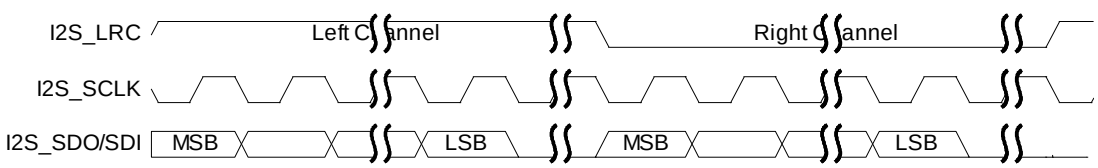


Figure 8-18 I2S Left-justified Timing Diagram

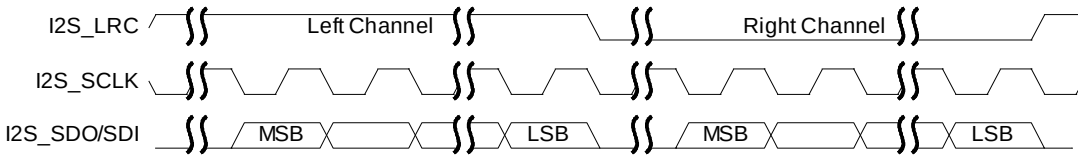


Figure 8-19 I2S Right-justified Timing Diagram

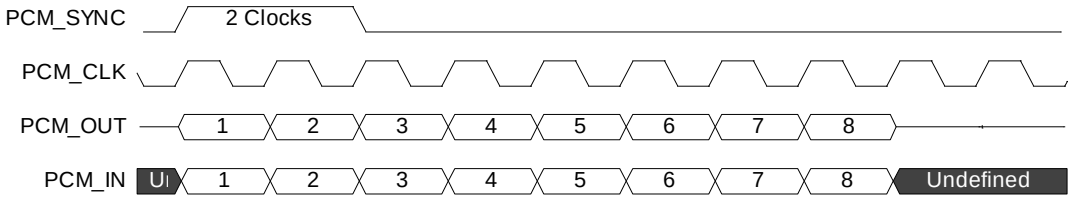


Figure 8-20 PCM Long Frame SYNC Timing Diagram

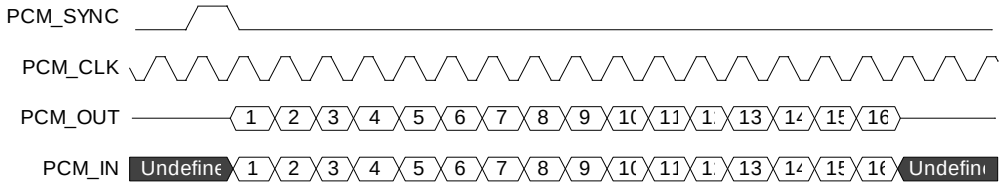


Figure 8-21 PCM Short Frame SYNC Timing Diagram

8.9.4. DIGITAL AUDIO INTERFACE REGISTER LIST

Module Name	Base Address
DA0	0x01C22000
DA1	0x01C22400

Register Name	Offset	Description

DA_CTL	0x00	Digital Audio Control Register
DA_FAT0	0x04	Digital Audio Format Register 0
DA_FAT1	0x08	Digital Audio Format Register 1
DA_TXFIFO	0x0C	Digital Audio TX FIFO Register
DA_RXFIFO	0x10	Digital Audio RX FIFO Register
DA_FCTL	0x14	Digital Audio FIFO Control Register
DA_FSTA	0x18	Digital Audio FIFO Status Register
DA_INT	0x1C	Digital Audio Interrupt Control Register
DA_ISTA	0x20	Digital Audio Interrupt Status Register
DA_CLKD	0x24	Digital Audio Clock Divide Register
DA_TXCNT	0x28	Digital Audio RX Sample Counter Register
DA_RXCNT	0x2C	Digital Audio TX Sample Counter Register
DA_TXCHSEL	0x30	Digital Audio TX Channel Select register
DA_TXCHMAP	0x34	Digital Audio TX Channel Mapping Register

8.9.5. DIGITAL AUDIO INTERFACE REGISTER DESCRIPTION

8.9.5.1. DIGITAL AUDIO CONTROL REGISTER

Offset: 0x00			**Register Name: DA_CTL** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:12	/	/	/
11	R/W	0	SDO3_EN 0: Disable 1: Enable
10	R/W	0	SDO2_EN 0: Disable 1: Enable

9	R/W	0	SDO1_EN 0: Disable 1: Enable
8	R/W	0	SDO0_EN 0: Disable 1: Enable
7	/	/	/
6	R/W	0	ASS Audio sample select when TX FIFO under run 0: Sending zero 1: Sending last audio sample
5	R/W	0	MS Master Slave Select 0: Master 1: Slave
4	R/W	0	PCM 0: I2S Interface 1: PCM Interface
3	R/W	0	/
2	R/W	0	TXEN Transmitter Block Enable 0: Disable 1: Enable
1	R/W	0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0	GEN Globe Enable

			A disable on this bit overrides any other block or channel enables. 0: Disable 1: Enable

8.9.5.2. DIGITAL AUDIO FORMAT REGISTER 0

Offset: 0x04			Register Name: DA_FAT0 Default Value: 0x0000_000C
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7	R/W	0	LRCP Left/ Right Clock Parity 0: Normal 1: Inverted In DSP/ PCM mode 0: MSB is available on 2nd BCLK rising edge after LRC rising edge 1: MSB is available on 1st BCLK rising edge after LRC rising edge
6	R/W	0	BCP BCLK Parity 0: Normal 1: Inverted
5:4	R/W	0	SR Sample Resolution 00: 16-bits 01: 20-bits 10: 24-bits 11: Reserved
3:2	R/W	0x3	WSS Word Select Size 00: 16 BCLK

			01: 20 BCLK 10: 24 BCLK 11: 32 BCLK
1:0	R/W	0	FMT Serial Data Format 00: Standard I2S Format 01: Left Justified Format 10: Right Justified Format 11: Reserved

8.9.5.3. DIGITAL AUDIO FORMAT REGISTER 1

Offset: 0x08			**Register Name: DA_FAT1** **Default Value: 0x0000_4020**
Bit	**Read/Write**	**Default**	**Description**
31:15	/	/	/
14:12	R/W	0x4	PCM_SYNC_PERIOD PCM SYNC Period Clock Number 000: 16 BCLK period 001: 32 BCLK period 010: 64 BCLK period 011: 128 BCLK period 100: 256 BCLK period Others : Reserved
11	R/W	0	PCM_SYNC_OUT PCM Sync Out 0: Enable PCM_SYNC output in Master mode 1: Suppress PCM_SYNC whilst keeping PCM_CLK running. Some Codec utilize this to enter a low power state.
10	R/W	0	PCM Out Mute

			Write 1 force PCM_OUT to 0
9	R/W	0	MLS MSB / LSB First Select 0: MSB First 1: LSB First
8	R/W	0	SEXT Sign Extend (only for 16 bits slot) 0: Zeros or audio gain padding at LSB position 1: Sign extension at MSB position When writing the bit is 0, the unused bits are audio gain for 13-bit linear sample and zeros padding for 8-bit companding sample. When writing the bit is 1, the unused bits are both sign extension.
7:6	R/W	0	SI Slot Index 00: the 1st slot 01: the 2nd slot 10: the 3rd slot 11: the 4th slot
5	R/W	1	SW Slot Width 0: 8 clocks width 1: 16 clocks width Notes: For A-law or u-law PCM sample, if this bit is set to 1, eight zero bits are following with PCM sample.
4	R/W	0	SSYNC Short Sync Select 0: Long Frame Sync 1: Short Frame Sync It should be set ‘1’ for 8 clocks width slot.

3:2	R/W	0	RX_PDM PCM Data Mode 00: 16-bits Linear PCM 01: 8-bits Linear PCM 10: 8-bits u-law 11: 8-bits A-law
1:0	R/W	0	TX_PDM PCM Data Mode 00: 16-bits Linear PCM 01: 8-bits Linear PCM 10: 8-bits u-law 11: 8-bits A-law

8.9.5.4. DIGITAL AUDIO TX FIFO REGISTER

Offset: 0x0C			**Register Name: DA_TXFIFO** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:0	W	0	TX_DATA TX Sample Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.

8.9.5.5. DIGITAL AUDIO RX FIFO REGISTER

Offset: 0x10			**Register Name: DA_RXFIFO** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:0	R	0	RX_DATA RX Sample

			Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

8.9.5.6. DIGITAL AUDIO FIFO CONTROL REGISTER

Offset: 0x14			Register Name: DA_FCTL Default Value: 0x0004_00F0
Bit	**Read/Write**	**Default**	**Description**
31	R/W	0	FIFOSRC TX FIFO source select 0: APB bus 1: Analog Audio CODEC
30:26	/	/	/
25	R/W	0	FTX Write ‘1’ to flush TX FIFO, self clear to ‘0’.
24	R/W	0	FRX Write ‘1’ to flush RX FIFO, self clear to ‘0’.
23:19	/	/	/
18:12	R/W	0x40	TXTL TX FIFO Empty Trigger Level Interrupt and DMA request trigger level for TXFIFO normal condition Trigger Level = TXTL
11:10	/	/	/
9:4	R/W	0xF	RXTL RX FIFO Trigger Level Interrupt and DMA request trigger level for RXFIFO normal condition Trigger Level = RXTL + 1
3	/	/	/
2	R/W	0	TXIM TX FIFO Input Mode (Mode 0, 1)

			0: Valid data at the MSB of TXFIFO register 1: Valid data at the LSB of TXFIFO register Example for 20-bits transmitted audio sample: Mode 0: FIFO_I[23:0] = {4'h0, TXFIFO[31:12]} Mode 1: FIFO_I[23:0] = {4'h0, TXFIFO[19:0]}
1:0	R/W	0	RXOM RX FIFO Output Mode (Mode 0, 1, 2, 3) 00: Expanding '0' at LSB of DA_RXFIFO register. 01: Expanding received sample sign bit at MSB of DA_RXFIFO register. 10: Truncating received samples at high half-word of DA_RXFIFO register and low half-word of DA_RXFIFO register is filled by '0'. 11: Truncating received samples at low half-word of DA_RXFIFO register and high half-word of DA_RXFIFO register is expanded by its sign bit. Example for 20-bits received audio sample: Mode 0: RXFIFO[31:0] = {FIFO_O[19:0], 12'h0} Mode 1: RXFIFO[31:0] = {12{FIFO_O[19]}, FIFO_O[19:0]} Mode 2: RXFIFO[31:0] = {FIFO_O[19:4], 16'h0} Mode 3: RXFIFO[31:0] = {16{FIFO_O[19], FIFO_O[19:4]}

8.9.5.7. DIGITAL AUDIO FIFO STATUS REGISTER

Offset: 0x18			**Register Name: DA_FSTA** **Default Value: 0x1080_0000**
Bit	**Read/Write**	**Default**	**Description**
31:29	/	/	/
28	R	1	TXE TX FIFO Empty 0: No room for new sample in TX FIFO

			1: More than one room for new sample in TX FIFO (>= 1 word)
27:24	/	/	/
23:16	R	0x80	TXE_CNT TX FIFO Empty Space Word Counter
15:9	/	/	/
8	R	0	RXA RX FIFO Available 0: No available data in RX FIFO 1: More than one sample in RX FIFO (>= 1 word)
7	/	/	/
6:0	R	0	RXA_CNT RX FIFO Available Sample Word Counter

8.9.5.8. DIGITAL AUDIO DMA & INTERRUPT CONTROL REGISTER

Offset: 0x1C			**Register Name: DA_INT** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7	R/W	0	TX_DRQ TX FIFO Empty DRQ Enable 0: Disable 1: Enable
6	R/W	0	TXUI_EN TX FIFO Under run Interrupt Enable 0: Disable 1: Enable
5	R/W	0	TXOI_EN TX FIFO Overrun Interrupt Enable 0: Disable

			1: Enable When set to '1', an interrupt happens when writing new audio data if TX FIFO is full.
4	R/W	0	TXEI_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
3	R/W	0	RX_DRQ RX FIFO Data Available DRQ Enable 0: Disable 1: Enable When set to '1', RXFIFO DMA Request line is asserted if Data is available in RX FIFO.
2	R/W	0	RXUI_EN RX FIFO Under run Interrupt Enable 0: Disable 1: Enable
1	R/W	0	RXOI_EN RX FIFO Overrun Interrupt Enable 0: Disable 1: Enable
0	R/W	0	RXAI_EN RX FIFO Data Available Interrupt Enable 0: Disable 1: Enable

8.9.5.9. DIGITAL AUDIO INTERRUPT STATUS REGISTER

Offset: 0x20	**Register Name: DA_ISTA** **Default Value: 0x0000_0010**

Bit	Read/Write	Default	Description
31:7	/	/	/
6	R/W	0	TXU_INT TX FIFO Under run Pending Interrupt 0: No Pending Interrupt 1: FIFO Under run Pending Interrupt
5	R/W	0	TXO_INT TX FIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Overrun Pending Interrupt Write ‘1’ to clear this interrupt
4	R/W	1	TXE_INT TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt Write ‘1’ to clear this interrupt or automatic clear if interrupt condition fails.
3:2	/	/	/
2	R/W	0	RXU_INT RX FIFO Under run Pending Interrupt 0: No Pending Interrupt 1:FIFO Under run Pending Interrupt Write 1 to clear this interrupt
1	R/W	0	RXO_INT RX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write ‘1’ to clear this interrupt
0	R/W	0	RXA_INT

			RX FIFO Data Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.

8.9.5.10. DIGITAL AUDIO CLOCK DIVIDE REGISTER

Offset: 0x24			Register Name: DA_CLKD Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/
7	R/W	0	MCLKO_EN 0: Disable MCLK Output 1: Enable MCLK Output Notes: Whether in Slave or Master mode, when this bit is set to 1, MCLK should be output.
6:4	R/W	0	BCLKDIV BCLK Divide Ratio from MCLK 000: Divide by 2 (BCLK = MCLK/2) 001: Divide by 4 010: Divide by 6 011: Divide by 8 100: Divide by 12 101: Divide by 16 110: Divide by 32 111: Divide by 64
3:0	R/W	0	MCLKDIV MCLK Divide Ratio from Audio PLL Output 0000: Divide by 1

			0001: Divide by 2 0010: Divide by 4 0011: Divide by 6 0100: Divide by 8 0101: Divide by 12 0110: Divide by 16 0111: Divide by 24 1000: Divide by 32 1001: Divide by 48 1010: Divide by 64 Others : Reserved

8.9.5.11. DIGITAL AUDIO TX COUNTER REGISTER

Offset: 0x28			Register Name: DA_TXCNT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value.

8.9.5.12. DIGITAL AUDIO RX COUNTER REGISTER

Offset: 0x2C			Register Name: DA_RXCNT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0	RX_CNT

			RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value.

8.9.5.13. DIGITAL AUDIO TX CHANNEL SELECT REGISTER

Offset: 0x30			Register Name: DA_TXCHSEL Default Value: 0x0000_0001
Bit	**Read/Write**	**Default**	**Description**
31:3	/	/	/
2:0	R/W	1	TX_CHSEL TX Channel Select 0: 1-ch 1: 2-ch 2: 3-ch 3: 4-ch 4: 5-ch 5: 6-ch 6: 7-ch 7: 8-ch

8.9.5.14. DIGITAL AUDIO TX CHANNEL MAPPING REGISTER

Offset: 0x34			Register Name: DA_TXCHMAP Default Value: 0x7654_3210
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:28	R/W	7	TX_CH7_MAP

			TX Channel7 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample
27	/	/	/
26:24	R/W	6	TX_CH6_MAP TX Channel6 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample
23	/	/	/
22:20	R/W	5	TX_CH5_MAP TX Channel5 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample

			110: 7th sample 111: 8th sample
19	/	/	/
18:16	R/W	4	TX_CH4_MAP TX Channel4 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample
15	/	/	/
14:12	R/W	3	TX_CH3_MAP TX Channel3 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample
11	/	/	/
10:8	R/W	2	TX_CH2_MAP TX Channel2 Mapping 000: 1st sample 001: 2nd sample

			010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample
7	/	/	/
6:4	R/W	1	TX_CH1_MAP TX Channel1 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample
3	/	/	/
2:0	R/W	0	TX_CH0_MAP TX Channel0 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample 100: 5th sample 101: 6th sample 110: 7th sample 111: 8th sample

8.9.5.15. DIGITAL AUDIO RX CHANNEL SELECT REGISTER

Offset: 0x38			Register Name: DA_RXCHSEL Default Value: 0x0000_0001
Bit	**Read/Write**	**Default**	**Description**
31:3	/	/	**/**
2:0	R/W	1	RX_CHSEL RX Channel Select 0: 1-ch 1: 2-ch 2: 3-ch 3: 4-ch Others: Reserved

8.9.5.16. DIGITAL AUDIO RX CHANNEL MAPPING REGISTER

Offset: 0x3C			Register Name: DA_RXCHMAP Default Value: 0x0000_3210
Bit	**Read/Write**	**Default**	**Description**
31:15	/	/	/
14:12	R/W	3	RX_CH3_MAP RX Channel3 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample Others: Reserved
11	/	/	/
10:8	R/W	2	RX_CH2_MAP RX Channel2 Mapping 000: 1st sample

			001: 2nd sample 010: 3rd sample 011: 4th sample Others: Reserved
7	/	/	/
6:4	R/W	1	RX_CH1_MAP RX Channel1 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample Others: Reserved
3	/	/	/
2:0	R/W	0	RX_CH0_MAP RX Channel0 Mapping 000: 1st sample 001: 2nd sample 010: 3rd sample 011: 4th sample Others: Reserved

8.9.6. DIGITAL AUDIO INTERFACE SPECIAL REQUIREMENT

8.9.6.1. DIGITAL AUDIO INTERFACE PIN LIST

Port Name	Width	Direction(M)	Description
DA_BCLK	1	IN/OUT	Digital Audio Serial Clock
DA_LRC	1	IN/OUT	Digital Audio Sample Rate Clock/ Sync
DA_SDO	1	OUT	Digital Audio Serial Data Output
DA_SDI	1	IN	Digital Audio Serial Data Input

DA_MCLK	1	OUT	Digital Audio MCLK Output

8.9.6.2. DIGITAL AUDIO INTERFACE MCLK AND BCLK

The Digital Audio Interface can support sampling rates from 128fs to 768fs, where fs is the audio sampling frequency that typicals 32KHz, 44.1KHz, 48KHz or 96KHz. For different sampling frequencies, the tables list the coefficient value of MCLKDIV and BCLKDIV.

Sampling Rate (kHz)	128fs	192fs	256fs	384fs	512fs	768fs
8	24	16	12	8	6	4
16	12	8	6	4	X	2
32	6	4	X	2	X	1
64	X	2	X	1	X	X
128	X	1	X	X	X	X
12	16	X	8	X	4	X
24	8	X	4	X	2	X
48	4	X	2	X	1	X
96	2	X	1	X	X	X
192	1	X	X	X	X	X

Table 8-1 MCLKDIV value for 24.576MHz Audio Serial Frequency

Sampling Rate (kHz)	128fs	192fs	256fs	384fs	512fs	768fs
11.025	16	X	8	X	4	X
22.05	8	X	4	X	2	X
44.1	4	X	2	X	1	X
88.2	2	X	1	X	X	X
176.4	1	X	X	X	X	X

Table 8-2 MCLKDIV value for 22.5792 MHz Audio Serial Frequency

Word Select Size	128fs	192fs	256fs	384fs	512fs	768fs
16	4	6	8	12	16	X
24	X	4	X	8	X	16
32	2	X	4	6	8	12

Table 8-3 BCLKDIV value for Different Word Select Size

8.9.6.3. DIGITAL AUDIO INTERFACE CLOCK SOURCE AND FREQUENCY

There are two clock sources for Digital Audio Interface: One is from APB bus and the other is from Audio PLL.

Name	Description
Audio_PLL	24.576Mhz or 22.528Mhz generated by Audio PLL
APB_CLK	APB bus system clock. In I2S mode, it is requested >= 0.25 BCLK. In PCM mode, it is requested >= 0.5 BCLK.

8.10. TRANSPORT STREAM CONTROLLER

8.10.1. OVERVIEW

The transport stream controller is responsible for de-multiplexing and pre-processing the inputting multimedia data defined in ISO/IEC 13818-1.

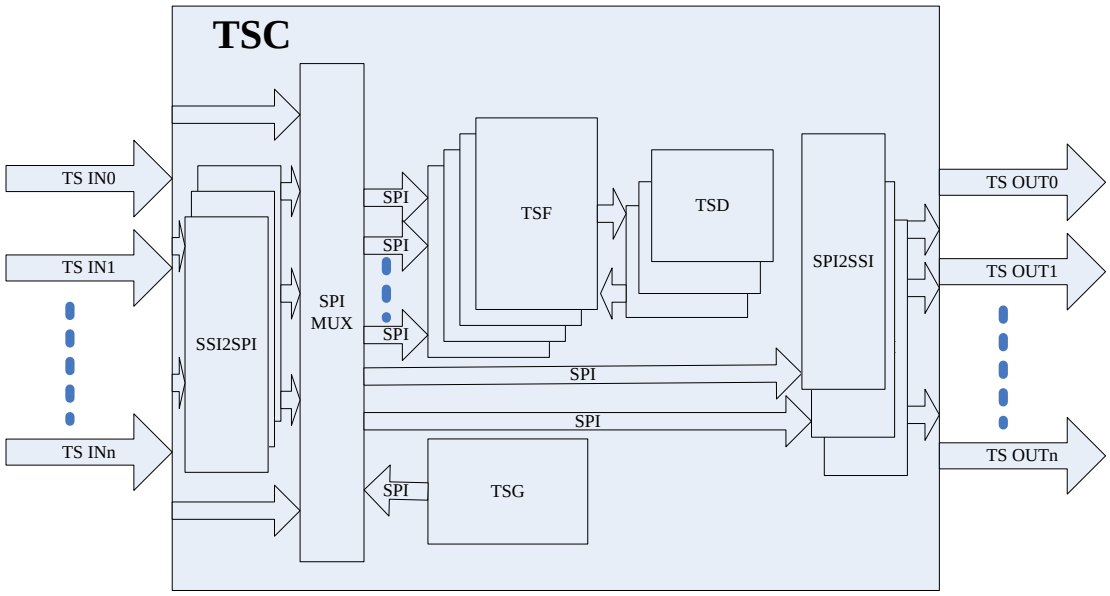
The transport stream controller receives multimedia data stream from SSI (Synchronous Serial Port)/SPI (Synchronous Parallel Port) inputs and de-multiplexing the data into Packets by PID (Packet Identify). Before the Packet is stored to memory by DMA, it can be pre-processing by the Transport Stream Descrambler.

The transport stream controller can be used for almost all multi-media application cases, example: DVB Set top Box, IPTV, Streaming-media Box, multi-media players and so on.

The Transport Stream Controller features:

- One external Synchronous Parallel Interface (SPI) or one external Synchronous Serial Interface (SSI)
- 32 channels PID filter
- Multiple transport stream packet (188, 192, 204) format support
- SPI and SSI timing parameters are configurable
- Hardware packet synchronous byte error detecting
- Hardware PCR packet detecting
- Configurable SPI transport stream generator for streams in DRAM memory
- DMA is supported for transferring data
- Support DVB-CSA V1.1 Descrambler

8.10.2. TSC BLOCK DIAGRAM



TSC – TS Controller; TSF – TS Filter; TSD – TS Descrambler; TSG – TS Generator

Figure 8-22 Transport Stream Controller Block Diagram

8.10.3. TSC REGISTER LIST

Module Name	Base Address
TSC_BASE	0x01C04000
TSG OFFSET	0x00000040
TSF0 OFFSET	0x00000080
TSF1 OFFSET	0x00000100

Register Name	Offset	Description
TSC_CTLR	TSC + 0x00	TSC Control Register
TSC_STAR	TSC + 0x04	TSC Status Register
TSC_PCTLR	TSC + 0x10	TSC Port Control Register
TSC_PPARR	TSC + 0x14	TSC Port Parameter Register

TSC_TSFMUXR	TSC + 0x20	TSC TSF Input Multiplex Control Register
TSC_OUTMUXR	TSC + 0x28	TSC Port Output Multiplex Control Register
TSG_CTLR	TSG + 0x00	TSG Control Register
TSG_PPR	TSG + 0x04	TSG Packet Parameter Register
TSG_STAR	TSG + 0x08	TSG Status Register
TSG_CCR	TSG + 0x0c	TSG Clock Control Register
TSG_BBAR	TSG + 0x10	TSG Buffer Base Address Register
TSG_BSZR	TSG + 0x14	TSG Buffer Size Register
TSG_BPR	TSG + 0x18	TSG Buffer Pointer Register
TSF_CTLR	TSF + 0x00	TSF Control Register
TSF_PPR	TSF + 0x04	TSF Packet Parameter Register
TSF_STAR	TSF + 0x08	TSF Status Register
TSF_DIER	TSF + 0x10	TSF DMA Interrupt Enable Register
TSF_OIER	TSF + 0x14	TSF Overlap Interrupt Enable Register
TSF_DISR	TSF + 0x18	TSF DMA Interrupt Status Register
TSF_OISR	TSF + 0x1c	TSF Overlap Interrupt Status Register
TSF_PCRCR	TSF + 0x20	TSF PCR Control Register
TSF_PCRDR	TSF + 0x24	TSF PCR Data Register
TSF_CENR	TSF + 0x30	TSF Channel Enable Register
TSF_CPER	TSF + 0x34	TSF Channel PES Enable Register
TSF_CDER	TSF + 0x38	TSF Channel Descramble Enable Register
TSF_CINDR	TSF + 0x3c	TSF Channel Index Register
TSF_CCTLR	TSF + 0x40	TSF Channel Control Register
TSF_CSTAR	TSF + 0x44	TSF Channel Status Register
TSF_CCWIR	TSF + 0x48	TSF Channel CW Index Register
TSF_CPIDR	TSF + 0x4c	TSF Channel PID Register
TSF_CBBAR	TSF + 0x50	TSF Channel Buffer Base Address Register
TSF_CBSZR	TSF + 0x54	TSF Channel Buffer Size Register
TSF_CBWPR	TSF + 0x58	TSF Channel Buffer Write Pointer Register

TSF_CBRPR	TSF + 0x5c	TSF Channel Buffer Read Pointer Register

8.10.4. TSC REGISTER DESCRIPTION

8.10.4.1. TSC CONTROL REGISTER

Offset: 0x00			Register Name: TSC_CTLR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

8.10.4.2. TSC STATUS REGISTER

Offset: 0x04			Register Name: TSC_STAR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

8.10.4.3. TSC PORT CONTROL REGISTER

Offset: 0x10			Register Name: TSC_PCTLR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:1	/	/	/
0	R/W	0	TS Input Port0 Control 0 – SPI 1 – SSI

8.10.4.4. TSC PORT PARAMETER REGISTER

Offset: 0x14	Register Name: TSC_PPARR Default Value: 0x0000_0000

<table>
<tr><th>Bit</th><th>Read/Write</th><th>Default</th><th>Description</th></tr>
<tr><td>31:8</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>7:0</td><td>R/W</td><td>0x00</td><td>TS Input Port0 Parameters
<table>
<tr><th>Bit</th><th>Definition</th></tr>
<tr><td>7:5</td><td>Reserved</td></tr>
<tr><td>4</td><td>SSI data order
0: MSB first for one byte data
1: LSB first for one byte data</td></tr>
<tr><td>3</td><td>CLOCK signal polarity
0 : Rise edge capturing
1: Fall edge capturing</td></tr>
<tr><td>2</td><td>ERROR signal polarity
0: High level active
1: Low level active</td></tr>
<tr><td>1</td><td>DVALID signal polarity
0: High level active
1: Low level active</td></tr>
<tr><td>0</td><td>PSYNC signal polarity
0: High level active
1: Low level active</td></tr>
</table></td></tr>
</table>

8.10.4.5. TSC TSF INPUT MULTIPLEX CONTROL REGISTER

<table>
<tr><th colspan="3">Offset: 0x20</th><th>Register Name: TSC_TSFMUXR
Default Value: 0x0000_0000</th></tr>
<tr><th>Bit</th><th>Read/Write</th><th>Default</th><th>Description</th></tr>
<tr><td>31:4</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>3:0</td><td>R/W</td><td>0x0</td><td>TSF0 Input Multiplex Control
0x0 –Data from TSG
0x1 –Data from TS IN Port0</td></tr>
</table>

			Others – Reserved

8.10.4.6. TSC PORT OUTPUT MULTIPLEX CONTROL REGISTER

Offset: 0x28			Register Name: TSC_TSFMUXR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

8.10.4.7. TSG CONTROL AND STATUS REGISTER

Offset: TSG+0x00			Register Name: TSG_CSR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:26	/	/	/
25:24	R	0	Status for TS Generator 0: IDLE state 1: Running state 2: PAUSE state Others: Reserved
23:10	/	/	/
9	R/W	0	Loop Buffer Mode When set to ‘1’, the TSG external buffer is in loop mode.
8	R/W	0	Sync Byte Check Enable Enable/ Disable check SYNC byte fro receiving new packet 0: Disable 1: Enable If enable check SYNC byte and an error SYNC byte is receiver, TS Generator would come into PAUSE state. If the correspond interrupt is enable, the interrupt would happen.
7:3	/	/	/

2	R/W	0	Pause Bit for TS Generator Write '1' to pause TS Generator. TS Generator would stop fetch new data from DRAM. After finishing this operation, this bit will clear to zero by hardware. In PAUSE state, write '1' to resume this state.
1	R/W	0	Stop Bit for TS Generator Write '1' to stop TS Generator. TS Generator would stop fetch new data from DRAM. The data already in its FIFO should be sent to TS filter. After finishing this operation, this bit will clear to zero by hardware.
0	R/W	0	Start Bit for TS Generator Write '1' to start TS Generator. TS Generator would fetch data from DRAM and generate SPI stream to TS filter. This bit will clear to zero by hardware after TS Generator is running.

8.10.4.8. TSG PACKET PARAMETER REGISTER

Offset: TSG+0x04			**Register Name: TSG_PPR** **Default Value: 0x0047_0000**
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
23:16	R/W	0x47	Sync Byte Value This is the value of sync byte used in the TS Packet.
15:8	/	/	/
7	R/W	0	Sync Byte Position 0: the 1st byte position 1: the 5th byte position Notes: This bit is only used for 192 bytes packet size.
6:2	/	/	/
1:0	R/W	0	Packet Size Byte Size for one TS packet

			0: 188 bytes 1: 192 bytes 2: 204 bytes 3: Reserved

8.10.4.9. TSG INTERRUPT ENABLE AND STATUS REGISTER

Offset: TSG+0x08			Register Name: TSG_IESR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:20	/	/	/
19	R/W	0	TS Generator (TSG) End Interrupt Enable 0: Disable 1: Enable If set this bit, the interrupt would assert to CPU when all data in external DRAM are sent to TS PID filter.
18	R/W	0	TS Generator (TSG) Full Finish Interrupt Enable 0: Disable 1: Enable
17	R/W	0	TS Generator (TSG) Half Finish Interrupt Enable 0: Disable 1: Enable
16	R/W	0	TS Generator (TSG) Error Sync Byte Interrupt Enable 0: Disable 1: Enable
15:4	/	/	/
3	R/W	0	TS Generator (TSG) End Status Write ‘1’ to clear.
2	R/W	0	TS Generator (TSG) Full Finish Status Write ‘1’ to clear.

1	R/W	0	TS Generator (TSG) Half Finish Status Write '1' to clear.
0	R/W	0	TS Generator (TSG) Error Sync Byte Status Write '1' to clear.

8.10.4.10. TSG CLOCK CONTROL REGISTER

Offset: TSG+0x0c			Register Name: TSG_CCR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:16	R/W	0x0	TSG Clock Divide Factor (N) The Numerator part of TSG Clock Divisor Factor.
15:0	R/W	0x0	TSG Clock Divide Factor (D) The Denominator part of TSG Clock Divisor Factor. Frequency of output clock: Fo = (Fi*(N+1))/(8*(D+1)). Fi is the input special clock of TSC, and D must not less than N.

8.10.4.11. TSG BUFFER BASE ADDRESS REGISTER

Offset: TSG+0x10			Register Name: TSG_BBAR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:28	/	/	/
27:0	RW	0x0	Buffer Base Address This value is a start address of TSG buffer. Note: This value should be 4-word (16Bytes) align, and the lowest 4-bit of this value should be zero.

8.10.4.12. TSG BUFFER SIZE REGISTER

Offset: TSG+0x14	Register Name: TSG_BSZR

			Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
23:0	R/W	0	Data Buffer Size for TS Generator It is in byte unit. The size should be 4-word (16Bytes) align, and the lowest 4 bits should be zero.

8.10.4.13. TSG BUFFER POINTER REGISTER

Offset: TSG+0x18			**Register Name: TSG_BPR** **Default Value: 0x1fff_0000**
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
23:0	R	0	Data Buffer Pointer for TS Generator Current TS generator data buffer read pointer (in byte unit)

8.10.4.14. TSF CONTROL AND STATUS REGISTER

Offset: TSF+0x00			**Register Name: TSF_CSR** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:3	/	/	/
2	R/W	0	TSFEN 0: Disable TSF Input 1: Enable TSF Input
1	/	/	/
0	R/W	0	TSF Global Soft Reset A software writing ‘1’ will reset all status and state machine of TSF. And it’s cleared by hardware after finish reset. A software writing ‘0’ has no effect.

8.10.4.15. TSF PACKET PARAMETER REGISTER

Offset: TSF+0x04			Register Name: TSF_PPR Default Value: 0x0047_0000
Bit	**Read/Write**	**Default**	**Description**
31:28	R/W	0	Lost Sync Packet Threshold It is used for packet sync lost by checking the value of sync byte.
27:24	R/W	0	Sync Packet Threshold It is used for packet sync by checking the value of sync byte.
23:16	R/W	0x47	Sync Byte Value This is the value of sync byte used in the TS Packet.
15:10	/	/	/
9:8	R/W	0	Packet Sync Method 0: By PSYNC signal 1: By sync byte 2: By both PSYNC and Sync Byte 3: Reserved
7	R/W	0	Sync Byte Position 0: the 1st byte position 1: the 5th byte position Notes: This bit is only used for 192 bytes packet size.
6:2	/	/	/
1:0	R/W	0	Packet Size Byte Size for one TS packet 0: 188 bytes 1: 192 bytes 2: 204 bytes 3: Reserved

8.10.4.16. TSF INTERRUPT ENABLE AND STATUS REGISTER

Offset: TSF+0x08			Register Name: TSF_IESR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:20	/	/	/
19	R/W	0	TS PID Filter (TSF) Internal FIFO Overrun Interrupt Enable 0: Disable 1: Enable
18	R/W	0	TS PCR Packet Detect Interrupt Enable 0: Disable 1: Enable
17	R/W	0	TS PID Filter (TSF) Channel Overlap Interrupt Global Enable 0: Disable 1: Enable
16	R/W	0	TS PID Filter (TSF) Channel DMA Interrupt Global Enable 0: Disable 1: Enable
15:4	/	/	/
3	R/W	0	TS PID Filter (TSF) Internal FIFO Overrun Status Write ‘1’ to clear.
2	R/W	0	TS PCR Packet Found Status When it is ‘1’, one TS PCR Packet is found. Write ‘1’ to clear.
1	R	0	TS PID Filter (TSF) Channel Overlap Status It is global status for 16 channel. It would clear to zero after all channels status bits are clear.
0	R	0	TS PID Filter (TSF) Channel DMA status It is global status for 16 channel. It would clear to zero after all channels status bits are clear.

8.10.4.17. TSF DMA INTERRUPT ENABLE REGISTER

Offset: TSF+0x10			Register Name: TSF_DIER Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0x0	DMA Interrupt Enable DMA interrupt enable bits for channel 0~31.

8.10.4.18. TSF OVERLAP INTERRUPT ENABLE REGISTER

Offset: TSF+0x14			Register Name: TSF_OIER Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0x0	Overlap Interrupt Enable Overlap interrupt enable bits for channel 0~31.

8.10.4.19. TSF DMA INTERRUPT STATUS REGISTER

Offset: TSF+0x18			Register Name: TSF_DISR Default Value: 0x3FFF_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0x0	DMA Interrupt Status DMA interrupt Status bits for channel 0~31. Set by hardware, and can be cleared by software writing '1'. When both these bits and the corresponding DMA Interrupt Enable bits set, the TSF interrupt will generate.

8.10.4.20. TSF OVERLAP INTERRUPT STATUS REGISTER

Offset: TSF+0x1c			Register Name: TSF_OISR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0x0	Overlap Interrupt Status

			Overlap interrupt Status bits for channel 0~31. Set by hardware, and can be cleared by software writing '1'. When both these bits and the corresponding Overlap Interrupt Enable bits set, the TSF interrupt will generate.

8.10.4.21. TSF PCR CONTROL REGISTER

Offset: TSF+0x20			Register Name: TSF_PCRCR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:17	/	/	/
16	R/W	0	PCR Detecting Enable 0: Disable 1: Enable
15:13	/	/	/
12:8	R/W	0	Channel Index m for Detecting PCR packet (m from 0 to 31)
7:1	/	/	/
0	R	0	PCR Contest LSB 1 bit PCR[0]

8.10.4.22. TSF PCR DATA REGISTER

Offset: TSF+0x24			Register Name: TSF_PCRDR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R	0	PCR Data High 32 bits PCR[32:1]

8.10.4.23. TSF CHANNEL ENABLE REGISTER

Offset: TSF+0x30	Register Name: TSF_CENR Default Value: 0x0000_0000

Bit	Read/Write	Default	Description
31:0	R/W	0x0	Filter Enable for Channel 0~31 0: Disable 1: Enable From Disable to Enable, internal status of the corresponding filter channel will be reset.

8.10.4.24. TSF CHANNEL PES ENABLE REGISTER

Offset: TSF+0x34			Register Name: TSF_CPER Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0x0	PES Packet Enable for Channel 0~31 0: Disable 1: Enable These bits should not be changed during the corresponding channel enable.

8.10.4.25. TSF CHANNEL DESCRAMBLE ENABLE REGISTER

Offset: TSF+0x38			Register Name: TSF_CDER Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

8.10.4.26. TSF CHANNEL INDEX REGISTER

Offset: TSF+0x3c			Register Name: TSF_CINDR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:5	/	/	/
4:0	R/W	0x0	Channel Index

			This value is the channel index for channel private registers access. Range is from 0x00 to 0x1f. Address range of channel private registers is 0x40~0x7f.

8.10.4.27. TSF CHANNEL CONTROL REGISTER

Offset: TSF+0x40			Register Name: TSF_CCTLR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

8.10.4.28. TSF CHANNEL STATUS REGISTER

Offset: TSF+0x44			Register Name: TSF_CSTAR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

8.10.4.29. TSF CHANNEL CW INDEX REGISTER

Offset: TSF+0x48			Register Name: TSF_CCWIR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	/	/	/

8.10.4.30. TSF CHANNEL PID REGISTER

Offset: TSF+0x4c			Register Name: TSF_CPIDR Default Value: 0x1fff_0000
Bit	**Read/Write**	**Default**	**Description**
31:16	R/W	0x1fff	Filter PID Mask for Channel
15:0	R/W	0x0	Filter PID value for Channel Filter Fit: Input PID & PID Mask == PID Value

8.10.4.31. TSF CHANNEL BUFFER BASE ADDRESS REGISTER

Offset: TSF+0x50			Register Name: TSF_CBBAR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0	Data Buffer Base Address for Channel It is 4-word (16Bytes) align address. The LSB four bits should be zero.

8.10.4.32. TSF CHANNEL BUFFER SIZE REGISTER

Offset: TSF+0x54			Register Name: TSF_CBSZR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:26	/	/	/
25:24	R/W	0	DMA Interrupt Threshold for Channel m (m from 1 to 15) The unit is TS packet size. When received packet (has also stored in DRAM) size is beyond (>=) threshold value, the corresponding channel interrupt is generated to CPU. TSC should count the new received packet again, when exceed the specified threshold value, one new interrupt is generated again. 0: 1/2 data buffer packet size 1: 1/4 data buffer packet size 2: 1/8 data buffer packet size 3: 1/16 data buffer packet size
23:21	/	/	/
20:0	R/W	0	Data Buffer Packet Size for Channel The exact buffer size of buffer is N+1 bytes. The maximum buffer size is 2MB. This size should be 4-word (16Bytes) aligned. The LSB four bits should be zero.

8.10.4.33. TSF CHANNEL BUFFER WRITE POINTER REGISTER

Offset: TSF+0x58			Register Name: TSF_CBWPR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:21	/	/	/
20:0	R/W	0	Data Buffer Write Pointer (in Bytes) This value is changed by hardware, when data is filled into buffer, this pointer is increased. And this pointer can be set by software, but it should not be changed by software during the corresponding channel is enable.

8.10.4.34. TSF CHANNEL BUFFER READ POINTER REGISTER

Offset: TSF+0x5c			Register Name: TSF_CBRPR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:21	/	/	/
20:0	R/W	0	Data Buffer Read Pointer (in Bytes) This pointer should be changed by software after the data of buffer is read.

8.10.5. TS CLOCK REQUIREMENT

Clock Name	Description	Requirement
HCLK	AHB bus clock	
TS_CLK	Clock of TS Stream in SPI mode	
TSC_CLK	TS serial clock from CCU	TSC_CLK >=8*TS_CLK

8.11. EMAC

8.11.1. OVERVIEW

The EMAC controller enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2002 standard. It supports 10M/100M/1000M external PHY with MII/GMII/RGMII interface in both full and half duplex mode. The EMAC-DMA is designed for packet-oriented data transfers based on a linked list of descriptors. 4K Byte TXFIFO and 16K Byte RXFIFO are provided to keep continuous transmission and reception. Flow Control, CRC Pad & Stripping, and address filtering are also supported in this module.

The EMAC Controller features:

- Comply with the IEEE 802.3-2002 standard
- Support both full-duplex and half-duplex operation
- Automatic CRC and pad generation controllable on a per-frame basis
- Options for Automatic Pad/CRC Stripping on receive frames
- Programmable frame length to support Standard or Jumbo Ethernet frames with size up to 16KB
- Support a variety of flexible address filtering modes
- Support 10/100/1000-Mbps data transfer rates IEEE 802.3-compiant GMII/MII interface to communicate with an external Gigabit/Fast Ethernet PHY
- Support 10/100/1000-Mbps data transfer rates RGMII interface to communicate with an external Gigabit PHY
- Optimization for packet-oriented DMA transfers with frame delimiters
- DMA's Descriptor architecture (ring or chained), allowing large blocks of data transfer with minimum CPU intervention
- 4KB transmit FIFO for transmission packets and 16KB receive FIFO for reception packet

8.12. ONE WIRE INTERFACE

8.12.1. OVERVIEW

The One Wire Interface implements the hardware protocol of the 1-Wire protocol, which use a single wire for communication between the Master (1-Wire controller) and the Slaves (1-Wire external compliant devices).

The One Wire interface is implemented as an open-drain output at the device level, therefore, an external pullup is required, and protocols use the return-to-1 mechanism (that is, after any command by any of the connected devices, the line is pulled to a logical high level).

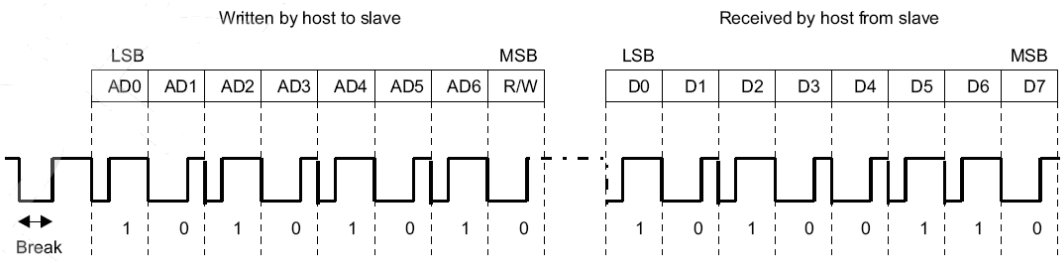
8.12.2. ONE WIRE INTERFACE WORK MODES

The One Wire Interface can work at Simple mode or Standard mode at one time.

Simple Mode

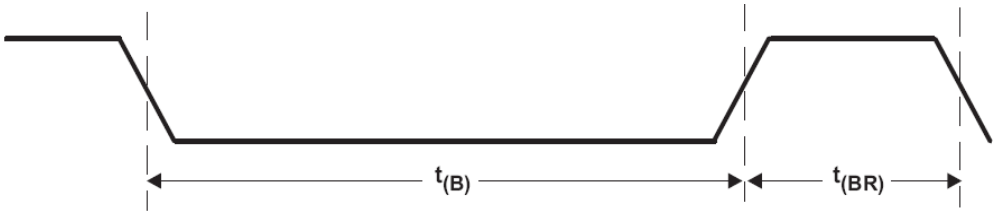
The bus of Simple Mode is a master-slave bus system using a simple one-wire, asynchronous, bi-directional, serial interface with a maximum bit-rate of about 5-Kbit/s.

It is a command-based protocol in which the host sends a command byte to the slave. The command directs the slave either to store the next eight bits of data received to a register specified by the command byte (Write command), or to output the eight bits of data from a register specified by the command byte (Read command). Command and data bytes consist of a stream of bits where the least-significant bit of a command or data byte is transmitted first. The first 7 bits of the command word are the register address and the last command bit transmitted is the read/write (R/W) bit. The following figure illustrates a typical HDQ read cycle.



In the figure, the 1 of the R/W bit indicates a write command where the 0 indicates the read command.

In Simple mode, the slave can be reset by using the break pulse. If the host does not get an expected response from the slave or if the host needs to restart a communication before it is complete, the host can hold the line low and generate a break to reset the communication engine. The Break timing is illustrated as below.

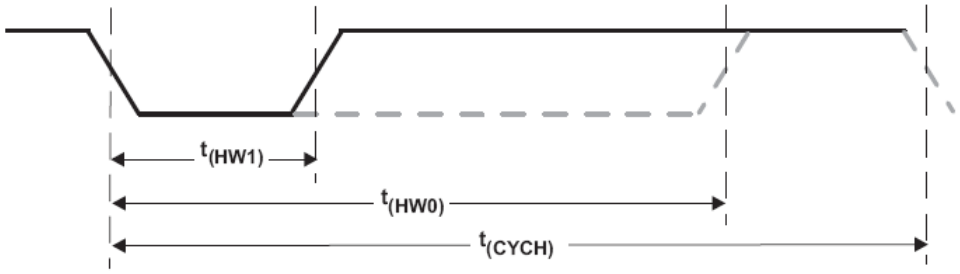


Timing Parameter	For Device	Minimum	Maximum
t(B)	All	190us	
t(BR)	All	40us	

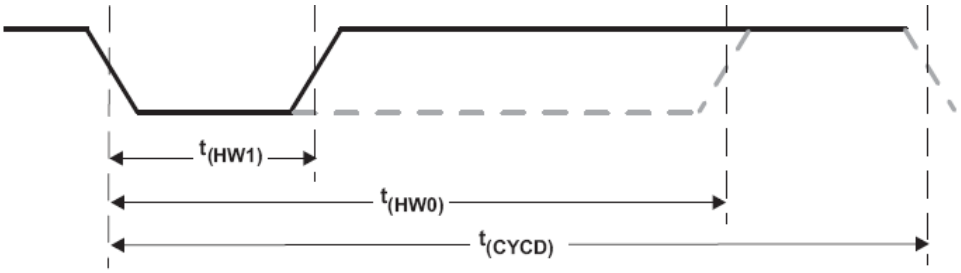
It is not required, but it is recommended to precede each communication with a break for the reliable communication.

After a successful break pulse (if have), the host and slave are ready for bit transmission. Each bit to transmit (either from the host to the slave or from the slave to the host) is preceded by a low-going edge on the line.

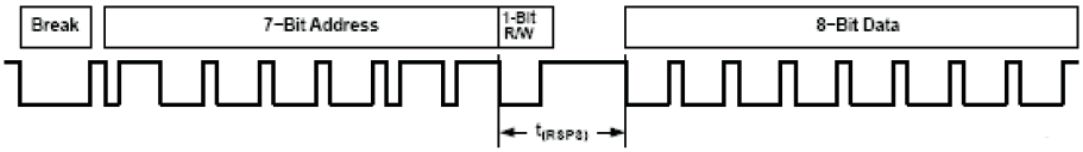
The host transmitted bit timing is showed as follow.



And the slave transmitted bit timing is showed as follow.



After the last bit of address is sent on a read cycle, the slave starts outputting the data after the specified response time, t(RSPS). The response time is measured from the fall time of the command R/W bit to the fall time of the first data bit returned by the slave and therefore includes the entire bit time for the R/W bit. Because the minimum response time equals to the minimum bit cycle time, this means that the first data bit may begin as soon as the command R/W bit time ends. The timing is show as follow.



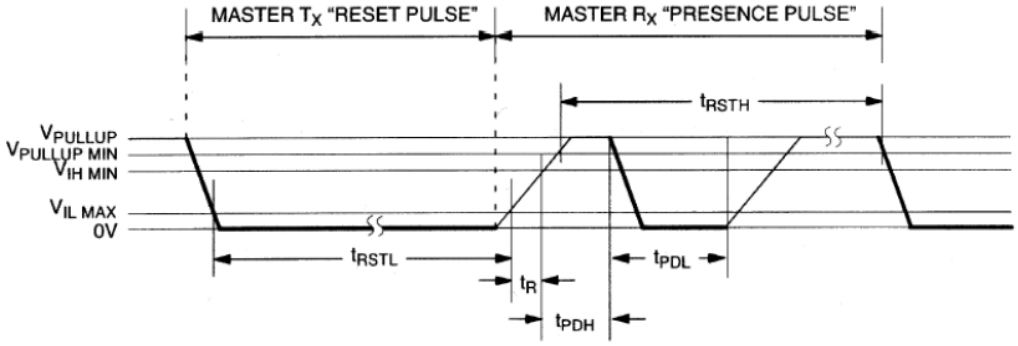
Timing Parameter	For Device	Minimum	Maximum
t(RSPS)	All	190us	320us

Also, to avoid short noise spike coupled onto the line, some filtering may be prudent.

Standard Mode

The Standard Mode consists of 4 types of signaling on the data line, which are Initialization Sequence, Write Zero, Write One and Read Data.

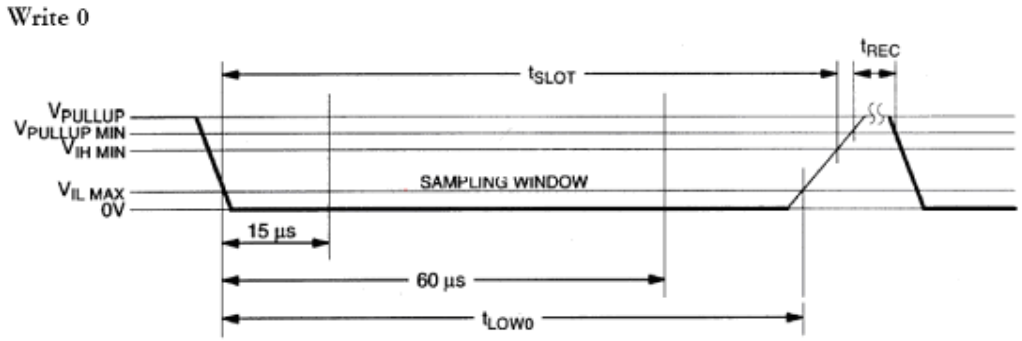
The host first sends an initialization pulse and then waits for the slave to respond with a presence pulse before enabling any communication sequence. The initialization pulse and presence pulse are showed as follow.



Timing Parameter	Minimum	Maximum
t(RSTL)	480us	
t(RSTH)	480us	
t(PDH)	15us	60us
t(PDL)	60us	240us

The other two types of signaling are Writing Zero and Writing One. The both write time slots must be a minimum of 60us in duration with a minimum of a 1us recovery time between individual write cycles. The slave device sample the data line in a window of 15us to 60us after the data line falls. If the line is high, a Write One occurs. If the line is low, a Write Zero occurs.

The Write Zero time slot is showed below.

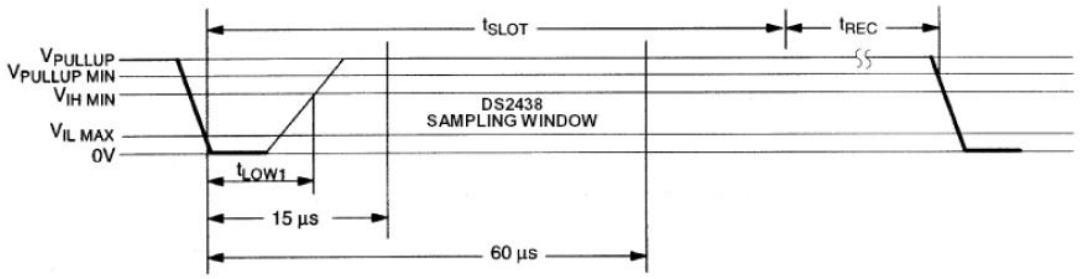


Timing Parameter	Minimum	Maximum
T(LOW0)	60us	t(SLOT)
t(SLOT)	T(LOW0)	120 us
t(REC)	1us	

When Write One occurs, the data line must be pulled to a logic low level and then released, allowing the data

line to pull up to a high level within 15us after the start of the write time slot. The Write One time slot is showed as follow.

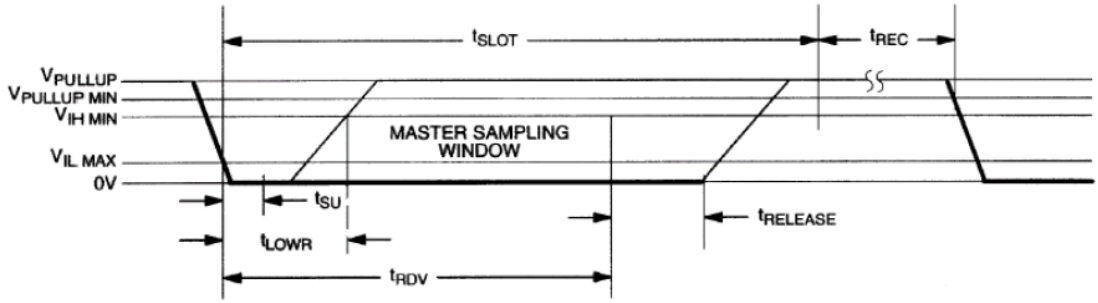
Write 1



Timing Parameter	Minimum	Maximum
t(SLOT)	60us	120 us
t(LOW1)	1us	15us
t(REC)	1us	

The last signaling type is Read Data. A read time slot is initiated when the bus master pulls the data line from a logic high level to logic low level. The data line must remain at a low logic level for a minimum of 1 us; output data from the slave is then valid within the next 14 us maximum.

The bus master therefore must stop driving the data line low in order to read its state 15 us from the start of the read slot. All read time slots must be a minimum of 60us in duration with a minimum of a 1 us recovery time between individual read slots. The Read Data slot is showed as follow.



Timing Parameter	Minimum	Maximum
t(SU)		1us
t(LOWR)	1us	15us

t(RDV)	(= 15us)	
t(RELEASE)	0us	45us
t(SLOT)	60 us	120 us
t(REC)	1us	

Cyclic Redundancy Check (CRC) is used by One Wire devices to ensure data integrity. Two different CRC are commonly found in 1-Wire devices. One 8 bit CRC and one 16 bit CRC. CRC8 is used in the ROM section of all devices. CRC8 is also in some devices used to verify other data, like commands issued on the bus. CRC16 is used by some devices to check for errors on larger data sets.

8.12.3. ONE WIRE INTERFACE REGISTER LIST

Module Name	Base Address
HDQ/One Wire	0x01F03000

Register Name	Offset	Description
OW_DATA	0x00	One Wire Data Register
OW_CTL	0x04	One Wire Control Register
OW_SMSC	0x08	One Wire Standard Mode Special Control Register
OW_SMCRC	0x0c	One Wire Standard Mode CRC Register
OW_INT_STATUS	0x10	One Wire Interrupt Status Register
OW_INT_MASK	0x14	One Wire Interrupt Mask Register
OW_FCLK	0x18	One Wire Function Clock Register
OW_LC	0x1C	One Wire Line Control Register
SM_WR_RD_TCTL	0x20	Standard Mode Write Read Timing Control Register
SM_RST_PRESENCE_TCTL	0x24	Standard Mode Reset Presence Timing Control Register

SP_WR_RD_TCTL	0x28	Simple Mode Timing Control Register
SP_BR_TCTL	0x2c	Simple Mode Break Timing Control Register

8.12.4. ONE WIRE INTERFACE REGISTER DESCRIPTION

8.12.4.1. ONE WIRE DATA REGISTER

Offset: 0x00			**Register Name: OW_DATA** **Default Value: 0x00000000**
Bit	**Read/Write**	**Default**	**Description**
24:31	/	/	/
23:16	R/W	0	**SM_DATA** These fields are for Simple Mode data send or receive in a one wire transmission. After this byte data transfer finishes, a transmission complete interrupt will generate.
15:8	/	0	/
7:0	R/W	0	**OW_DATA** Data byte for transmitting or received In Simple mode, these fields are for the command byte transmission. When GO bit is set (the INITIALIZATION/BREAK bit is not set at the same time), these fields will be sent as the address and command for a Simple Mode transfer. After the command byte transmission finished, the controller in Simple Mode will send next 8 bit data from SM_DATA when the DIR bit is 1 or receive one byte data to SM_DATA when the DIR bit is 0. In Standard Mode, if the INITIALIZATION/BREAK bit is not set, the controller samples/sends data to/from these fields determining by the DIR bit when the Go bit is set. When the ONE_WIRE_SINGLE_BIT is enabled, only the first bit of these fields is available.

8.12.4.2. ONE WIRE CONTROL REGISTER

Offset: 0x04			Register Name: OW_CTL Default Value: 0x00030000
Bit	**Read/Write**	**Default**	**Description**
31:20	/	/	/
19:16	R/W	0x3	SAMPLE_TIME These fields determine the sample times in digital circuit.
15:10	/	/	/
9	R/W	0	INNER_PULL_UP_ENABLE(50K~150K) When this bit is set, the inner pull up for one wire bus is determined by inner output (pull up is off when bus is drive 0) 0: inner pull up is on 1: inner pull up is off when bus is drive 0
8	R/W	0	**AUTOIDLE** Auto Idle 0: Module clock is free-running; 1: Module clock is in power saving mode, the function clock is running only when module is accessed or inside logic is in function to process events.
7	/	/	/
6	R	0	**PRESENCEDETECT** Slave Presence Indicator This read-only flag is only used in Standard mode. The value of this field indicates whether there is Presence Pulse responding to the host initialization pulse. The flag is updated when the **OW_INT_STATUS[0]** Presence Detect Interrupt Flag is set.
5	R/W	0	**STANDARD_MODE_SINGLE_BIT** The single-bit mode is only supported for Standard Mode (Simple

			mode does not support bit transfer mode). After the bit is transferred, Tx-complete or Rx-complete interrupt will generate for corresponding transfer operation. 0: Disabled 1: Enabled
4	R/W	0	**Go** Go Bit Write 1 to start the appropriate operation. If the INITIALIZATION/BREAK bit is set, the controller generates the initialization or break pulse. If the INITIALIZATION/BREAK bit is not set, the controller in Standard Mode samples/sends data to/from the **OW_DATA** fields determining by the DIR bit, or the controller in Simple Mode begins a transfer sequence with the command byte in **OW_DATA**. Bit returns to 0 after the operation is complete.
3	R/W	0	**INITIALIZATION/BREAK** Initialization/Break Bit Write 1 to send initialization pulse for the Standard Mode or break pulse for the Simple Mode. The **OW_DATA** register will be flushed when initialization or the break situation is generating. Bit returns to 0 after pulse is sent. The pulse generates after the **Go** bit is set.
2	R/W	0	**DIR** Direction Bit In Standard Mode, this field determines if next operation (byte operation or bit operation) is read or write. In Simple Mode, this field determines if the current transfer sequence is read or write. 0 = read

			1 = write The operation starts after the Go bit is set.
1	R/W	0	**MS** Mode Selection Bit 0: Standard Mode 1: Simple mode When the controller is working in Simle Mode, it is compliance with the HDQ protocol. Else, it implements as a standard one wire controller.
0	R/W	0	**GEN** Global Enable This field is used to enable or disable the One Wire Controller. A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable

8.12.4.3. ONE WIRE STANDARD MODE SPECIAL CONTROL REGISTER

Offset: 0x08			**Register Name: OW_SMSC** **Default Value: 0x00000000**
Bit	**Read/Write**	**Default**	**Description**
31:6	/	/	**/**
5	R/W	0	**CRC_ERROR_STATUS** These fields indicate the result of the CRC compareing. 0: CRC compareing right 1: CRC compareing wrong
4	/	/	**/**
3	R/W	0	**MEM_CRC_COMPARE** This field is only used in Standard mode. When this field is

			set, the controller will compare the value in the CRC_RECEV field with the data read from the CRC_CALC_INDICATE field, and then returns corresponding result in the CRC_ERROR_STATUS field and generates CRC finish interrupt. The CRC shift register and CRC_CALC_INDICATE field will be cleaned to 0 then. This field will be automatically cleaned when the CRC compare is finish.
2	R/W	0	**CRC_16BIT_EN** This field is only used in Standard mode and is set to 1 to select 16bit CRC, else the 8bit CRC is select. 0: CRC_8BIT_EN 1: CRC_16BIT_EN
1	R/W	0	**WR_MEM_CRC_REQ** This field is only used in Standard mode. When this bit is set, the bit send to the device will be took into calculate the CRC value (CRC8 or CRC16). The calculation will stop when this bit is cleaned. The value will be preserved in the corresponding CRC (CRC8 or CRC16) shift register then.
0	R/W	0	**RD_MEM_CRC_REQ** This field is only used in Standard mode. When this bit is set, the bit received from the device will be took into calculate the CRC value (CRC8 or CRC16). The calculation will stop when this bit is cleaned. The value will be preserved in the corresponding CRC (CRC8 or CRC16) shift register then.

8.12.4.4. ONE WIRE STANDARD MODE CRC REGISTER

Offset: 0x0c	**Register Name: OW_SMCRC** **Default Value: 0x00000000**

Bit	Read/Write	Default	Description
31:16	R	0	**CRC_CALC_INDICATE** This field indicates the CRC value calculated by the CRC shift register.
15:0	R/W	0	**CRC_RECEV** The data CRC value (CRC8 or CRC16) will be written to these fields by software for CRC comparing.

8.12.4.5. ONE WIRE INTERRUPT STATUS REGISTER

Offset: 0x10			Register Name: OW_INT_STATUS Default Value: 0x00000000
Bit	**Read/Write**	**Default**	**Description**
31:6	/	/	/
5	R/W	0	**Deglitch Detected Interrupt Flag** This flag indicates a deglitch in the bus. The controller looks for any glitch in the sample window for at least 1us. If the Deglitch Interrupt is enabled, an interrupt will issues when any deglitch occurs in the bus. The interrupt condition is cleared by writing “1” to this field.
4	R/W	0	**CRC Compareing Complete Interrupt Flag** This flag is used in Standard mode, and is used to indicate the CRC compareing has finished. The interrupt condition is cleared by writing “1” to this field.
3	R/W	0	**Transmission Complete Interrupt Flag** In the Standard mode, the flag is set when a write operation of one byte or one bit in single-bit mode was completed. The interrupt is generated then. In the Simple Mode, the flag is set when a write operation of one byte was completed. The interrupt is also generated.

			The interrupt condition is cleared by writing “1” to this field.
2	R/W	0	**Read Complete Interrupt Flag** In the Standard mode, the flag is set when a byte or a bit in single-bit mode has been successfully read. The interrupt is generated then. In the Simple, the flag is set when a byte has been successfully read. The interrupt is also generated then. The interrupt condition is cleared by writing “1” to this field.
1	R/W	0	**Time-out Interrupt Flag** This flag is only used in Simple Mode. The flag is set when two event happened. The one event is that after a read command initiated by the host, the slave did not pull the line low within the specified time (512 us). The other event is that another bit transfer does not begin after a specified time (512 us) from the pre-bit beginning. When the above situation occurs, the interrupt generates and the value of this field is set. The interrupt condition is cleared by writing “1” to this field.
0	R/W	0	**Presence Detect Interrupt Flag** In the Standard mode, this interrupt status is set when the Initialization Pulse is completed. The interrupt is generated then and the PRESENCEDETECT bit is update. In the Simple Mode, the flag is set when the successful completion of a break pulse. The interrupt is also generated then. The interrupt condition is cleared by writing “1” to this field.

8.12.4.6. HDQ/ONE WIRE INTERRUPT MASKING REGISTER

Offset: 0x14			**Register Name: OW_INT_MASK** **Default Value: 0x00000000**
Bit	**Read/Write**	**Default**	**Description**
31:6	/	/	/

5	R/W	0	**Deglitch Detected Interrupt Enable** 0 = Disable 1 = Enable
4	R/W	0	**CRC Compareing Complete Interrupt Enable** 0 = Disable 1 = Enable
3	R/W	0	**Transmission Complete Interrupt Enable** 0 = Disable 1 = Enable
2	R/W	0	**Read Complete Interrupt Enable** 0 = Disable 1 = Enable
1	R/W	0	**Time-out Interrupt Enable** 0 = Disable 1 = Enable
0	R/W	0	**Presence Detect Interrupt Enable** 0 = Disable 1 = Enable

8.12.4.7. ONE WIRE FUNCTION CLOCK REGISTER

Offset: 0x18			**Register Name: OW_FCLK** **Default Value: 0x00000000**
Bit	**Read/Write**	**Default**	**Description**
31:21	/	/	/
20:16	R/W	0	OW_FCLK (n) A n MHz clock is needed to use as a time reference by the machine. Transitions between the states of the state machine as well a actions triggered at precise time deadlines are expressed using the n – MHz clock.

15:8	/	/	/
7:0	R/W	0	OW_FCLK_D OW_FCLK = SOURCE_CLK/OW_FCLK_D

8.12.4.8. ONE WIRE LINE CONTROL REGISTER

Offset: 0x1c			Register Name: OW_LC Default Value: 0x00000000
Bit	**Read/Write**	**Default**	**Description**
31:3	/	/	/
2	R	1	**Current state of One Wire Line** 0: low 1: high
1	R/W	0	**One Wire line state control bit** When the line control mode is enabled (bit [0] set), value of this bit decides the output level of the One Wire line. 0: output low level 1: output high level
0	R/W	0	**One Wire line state control enable** When this bit is set, the state of One Wire line is control by the value of bit [1]. 0: disable line control mode 1: enable line control mode

8.12.4.9. STANDARD MODE WRITE READ TIMING CONTROL REGISTER

Offset: 0x20			Register Name: OW_SMSC Default Value: 0x213de0bc
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:29	R/W	0x1	TSU

			Read Data Setup. In standard speed, range: t(SU) < 1 00: 0.5us 01: 1us 10: 2us 11: 4us
28	/	/	/
27:24	R/W	1	REC Recovery Time, t(recovery) = N us. In standard speed, range:: 1us <= t(recovery)
23	/	/	/
22:18	R/W	0xf	TRDV Read data valid time, t(rdv) = N us. In standard speed, range: Exactly 15
17:11	R/W	0x3c	TLOW0 Write Zero time Low, Tlow0 = N us. The range setting for TLOW0 is from 0x3c to 0x77. In standard mode, range:60<= t(low0) < t(tslot) <120
10:7	R/W	1	TLOW1 Write One time Low, or TLOWR both are same. t(low1) = N us. The range setting for TLOW1 and TLOWR here is from 0x1 to 0xf. In standard speed, range:1 <= t(low1) < 15. t(lowR) = N owr clks. In standard speed, rang = 1 <= t(lowR) <15
6:0	R/W	0x3c	TSLOT Active time slot for write and read data, t(slot) = N us. The range settting for TSLOT is from 0x3c to 0x78. In standard mode, range:60 <= t(slot) <120

8.12.4.10. STANDARD MODE RESET PRESENCE TIMING CONTROL REGISTER

Offset: 0x24	Register Name: SM_RST_PRESENCE_TCTL Default Value:

			0x3c3fc1e0
Bit	**Read/Write**	**Default**	**Description**
31:24	R/W	0x3c	TPDL PRESENCE_DETECT_LOW t(pdl) = N us. The range setting for TPDL in these fields is from 0 to 0xf0. In standard speed, Range: 60 <= t(pdl) <240.
23:18	R/W	0xf	TPDH PRESENCE_DETECT_HIGH t(pdh) = N us. The range setting for TPDH in these fields is from 0xf to 0x3c. In standard speed, range: 15 <= t(pdh) < 60 .
17:9	R/W	0x1e0	TRSTL RESET_TIME_LOW t(rstl) = N us. The range setting for TRSTL in these fields is from 0 to 0xff. In standard speed , Range: 480 <= t(rstl) < infinity
8:0	R/W	0x1e0	TRSTH RESET_TIME_HIGH, t(rsth) = N us. The range setting for TRSTH in these fields is from 0 to 0xff. In standard speed , Range : 480 <= t(rsth) < infinity

8.12.4.11. SIMPLE MODE TIMING CONTROL REGISTER

Offset: 0x28			**Register Name: SP_WR_RD_TCTL** **Default Value: 0x0a0158be**
Bit	**Read/Write**	**Default**	**Description**
31:28	R/W	0	RD_SAMPLE_POINT When controller of the Simple Mode read, the default sample point is at the middle of the THW1 point and the THW0 point, named S(middle). When these fields are set, the corresponding new sample point will be determined.

0000	S(middle)		1000	S(middle)-30us

			0001	S(middle)+5us		1001	S(middle)+40us
			0010	S(middle)-5us		1010	S(middle)-40us
			0011	S(middle)+10us		1011	S(middle)+50us
			0100	S(middle)-10us		1100	S(middle)-50us
			0101	S(middle)+20us		1101	S(middle)+60us
			0110	S(middle)-20us		1110	S(middle)-60us
			0111	S(middle)+30us		1111	reserve
27:22	R/W	0x28	THW1_INT t(HW1_INT) = N us. The range setting for THW1_INT in these fields is from 0 to 0x3f, which is the integer part of the THW1. In HDQ mode, Range: t(HW0) <= 50 us.				
21:18	R/W	0	THW1_DEC THW1_DEC is the decimal part of the THW1. t(HW1_DEC) = N ow_clks. The value for the THW1 = THW1_INT + THW1_DEC.				
17:10	R/W	0x56	THW0 t(HW0) = N us. The range setting for THW0 in these fields is from 0 to 0xff. In HDQ mode, Range: t(HW0) <= 145 us.				
9:0	R/W	0xbe	TCYCH t(CYCH) = N us. The range setting for TCYCH in these fields is from 0 to 0x3ff. In HDQ mode, Rang: 190 us <= t(CYCH) <= infinity.				

8.12.4.12. SIMPLE MODE BREAK TIMING CONTROL REGISTER

Offset: 0x2c			**Register Name: SP_BR_TCTL** **Default Value: 0x0be0028**
Bit	**Read/Write**	**Default**	**Description**
31:26	/	/	/
25:16	R/W	0xbe	TB t(B) = N us. The range setting for TB in these fields is from 0 to 0x 3ff.

			In HDQ mode, Rang: 190 us <= t(B) <= infinity.
15:10	/	/	/
9:0	R/W	0x28	TBR t(BR) = N us. The range setting for TBR in these fields is from 0 to 0xff. In HDQ mode, Rang: 40 us <= t(BR) <= infinity.

APPENDIX ABBREVIATIONS

A

AES	Advanced Encryption Standard	A specification for the encryption of electronic data established by the U.S. National Institute of Standards and Technology (NIST) in 2001
AGC	Automatic Gain Control	An adaptive system found in electronic devices that automatically controls the gain of a signal: the average output signal level is fed back to adjust the gain to an appropriate level for a range of input signal levels.
AHB	AMBA High-speed Bus	A bus protocol introduced in Advanced Microcontroller Bus Architecture version 2 published by ARM Ltd company
APB	Advanced Peripheral Bus	APB is designed for low bandwidth control accesses, which has an address and data phase similar to AHB, but a much reduced, low complexity signal list (for example no bursts).
AVS	Audio Video Standard	A compression standard for digital audio and video

C

CIR	Consumer IR	The CIR (Consumer IR) interface is used for remote control through infra-red light
CRC	Cyclic Redundancy Check	A type of hash function used to produce a checksum in order to detect errors in data storage or transmission
CSI	CMOS Sensor Interface	The hardware block that interfaces with different image sensor interfaces and provides a standard output that can be used for subsequent image processing

D

DES	Data Encryption Standard	A previously predominant algorithm for the encryption of electronic data
DEU	Detail Enhancement Unit	A unit used for display engine frontend data post-processing
DLL	Delay-Locked Loop	A digital circuit similar to a phase-locked loop (PLL), with the main difference being the absence of an internal voltage-controlled oscillator, replaced by a delay line
DRC	Dynamic Range Compression	It reduces the volume of loud sounds or amplifies quiet sounds by narrowing or "compressing" an audio signal's dynamic range.
DVFS	Dynamic Voltage and Frequency Scaling	Dynamic voltage scaling is a power management technique where the voltage used in a component is increased or decreased, depending on

		circumstances. Dynamic frequency scaling is a technique whereby the frequency of a microprocessor can be automatically adjusted on the fly so that the power consumption or heat generated by the chip can be reduced. These two are often used together to save power in mobile devices.

E

EHCI	Enhanced Host Controller Interface	The register-level interface for a Host Controller for the USB Revision 2.0.
eMMC	Embedded Multi-Media Card	An architecture consisting of an embedded storage solution with MMC interface, flash memory and controller, all in a small BGA package

F

FBGA	Fine Ball Grid Array	FBGA is based on BGA technology, but comes with thinner contacts and is mainly used in SoC design

G

GIC	Generic Interrupt Controller	A centralized resource for supporting and managing interrupts in a system that includes at least one processor

H

HDMI	High-Definition Multimedia Interface	A compact audio/video interface for transmitting uncompressed digital data

I

IEP	Image Enhancement Processor	A unit used for the improvement of digital image quality, including DEU, DRC, CMU.
I2S	IIS	An electrical serial bus interface standard used for connecting digital audio devices together

L

LSB	Least Significant Bit	The bit position in a binary integer giving the units value, that is, determining whether the number is even or odd. It is sometimes referred to as the right-most bit, due to the convention in positional notation of writing less significant digits further to the right.
LRADC	Low Resolution Analog to Digital Converter	A module which can transfer analog signals to digital signals

M

MAC	Media Access Control	A sublayer of the data link layer, which provides addressing and channel access control mechanisms that make it possible for several terminals or network nodes to communicate within a multiple access network that incorporates a shared medium, e.g. Ethernet.

MII	Media Independent Interface	An interface originally designed to connect a fast Ethernet MAC-block to a PHY chip, which now has been extended to support reduced signals and increased speeds
MIPI	Mobile Industry Processor Interface	MIPI alliance is an open membership organization that includes leading companies in the mobile industry that share the objective of defining and promoting open specifications for interfaces inside mobile terminals.
MIPI DSI	MIPI Display Serial Interface	A specification by the Mobile Industry Processor Interface (MIPI) Alliance aimed at reducing the cost of display sub-systems in a mobile device
MSB	Most Significant Bit	The bit position in a binary number having the greatest value, which is sometimes referred to as the left-most bit due to the convention in positional notation of writing more significant digits further to the left

N

NTSC	National Television System Committee	An analog television system that is used in most of North America, and many other countries

O

OHCI	Open Host Controller Interface	A register-level interface that enables a host controller for USB or FireWire hardware to communicate with a host controller driver in software
OSD	On-Screen Display	A feature of visual devices like VCRs and DVD players that displays program, position, and setting data on a connected TV or computer display

P

PAL	Phase Alternating Line	An analogue television color encoding system used in broadcast television systems in many countries
PCM	Pulse Code Modulation	A method used to digitally represent sampled analog signals
PID	Packet Identifier	Each table or elementary stream in a transport stream is identified by a 13-bit packet ID (PID). A demultiplexer extracts elementary streams from the transport stream in part by looking for packets identified by the same PID.

S

SPI	Synchronous Peripheral Interface	A synchronous serial data link standard named by Motorola that operates in full duplex mode. Devices communicate in master/slave mode where the master device initiates the data frame

T

TP	Touch Panel	A human-machine interactive interface
TS	Transport Stream	A data stream defined by ISO13818-1, which consists of one or more programs with video and audio data.

U

USB DRD	Universal Serial Bus Dual-Role Device	A dual-role controller, which supports both Host and Device functions and is fully compliant with the On-The-Go Supplement to the USB 2.0 Specification, Revision 1.0a